Fault Isolation and Failure Analysis Approaches for Advanced Packaging

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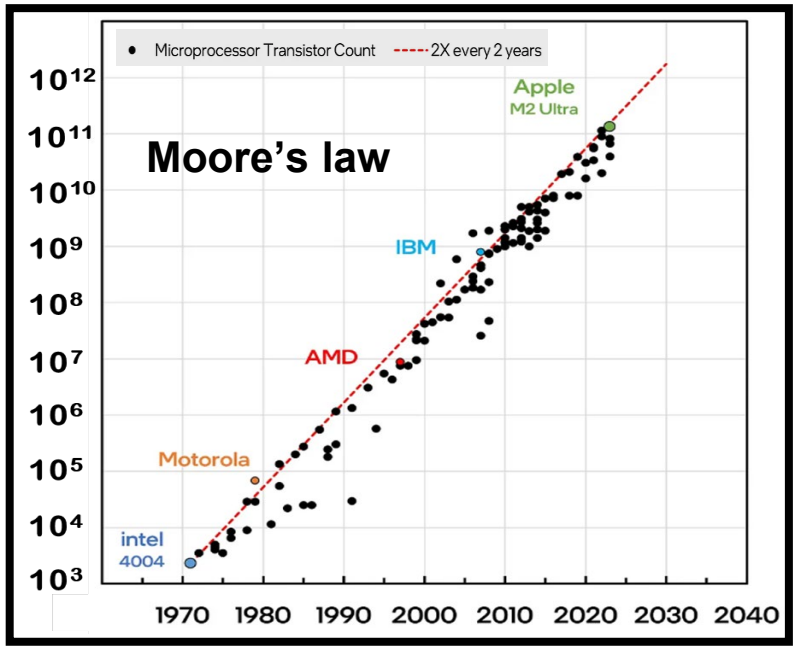
SAMSUNG

Outline

- Introduction
- Fault Isolation and Failure Analysis Challenges
- Fault Isolation and Failure Analysis Approaches
- Future Development Trends
- Conclusions

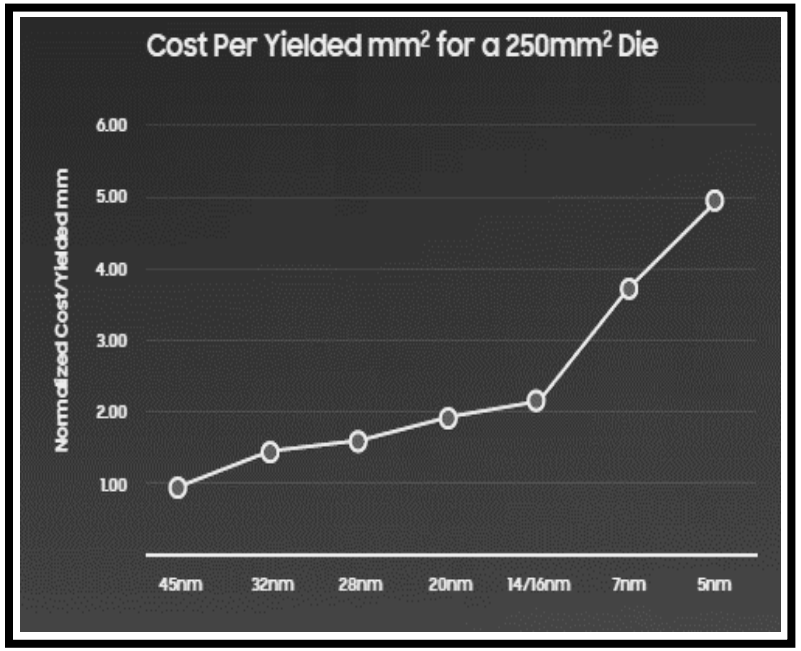
Why advanced packaging?

Advanced packaging techniques are utilized to meet the market needs



Moore's law predicts the exponential growth of ICs since 1970s---***Market needs***

https://semiconductor.substack.com/p/the-relentless-pursuit-of-moores

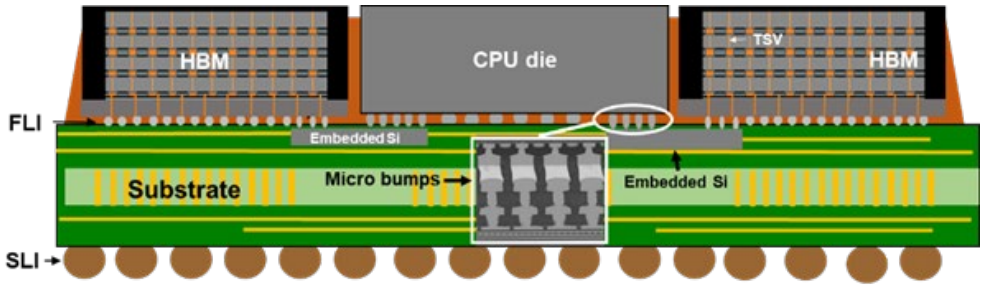


The exponential growth of cost per Yielded mm^2 for 250 mm^2 die ----***Challenges for Si level scaling and yielding***

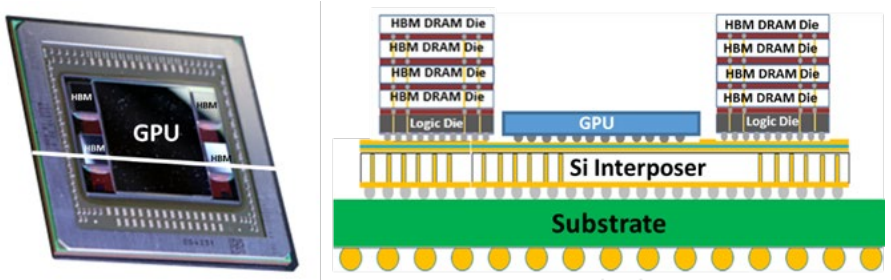
- **Chiplet**
- **Heterogeneous integration**
- **Die stacking**

Advanced packages on market

Smaller interconnects; Higher performance; Lower power consumption

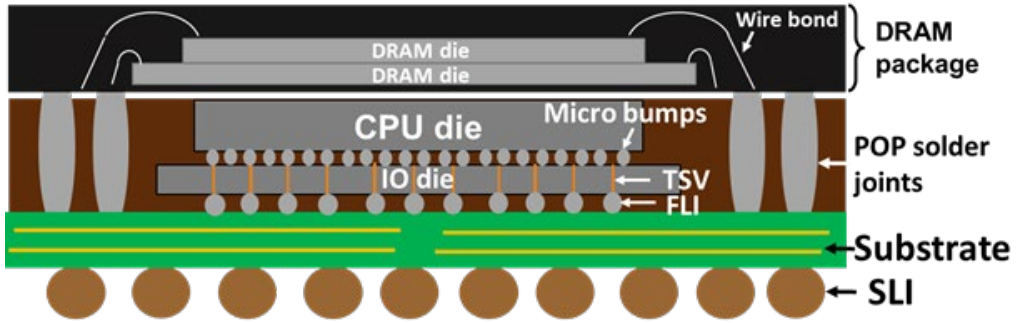


Embedded Multi-Die Interconnect Bridge (EMIB) from Intel

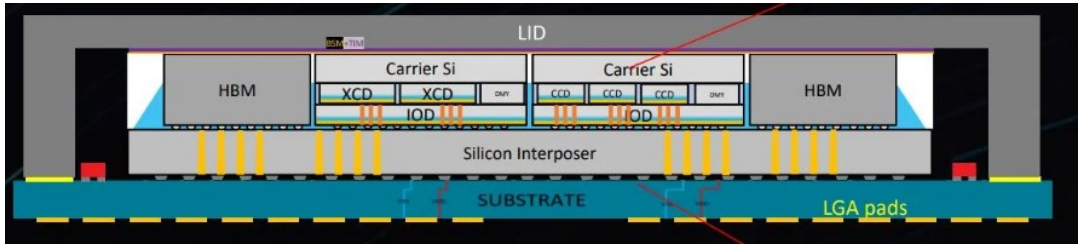


AMD Radeon™ Fury

Chip-On-Wafer-On-Substrate (CoWoS) from TSMC



Foveros technology from Intel



AMD Instinct™ MI300 Family

3D Hybrid bonded chips on CoWoS from TSMC

3D Microelectronic Packaging: From Architectures to Applications, 2nd edition, Springer, 2021, ISSN 1437-0387

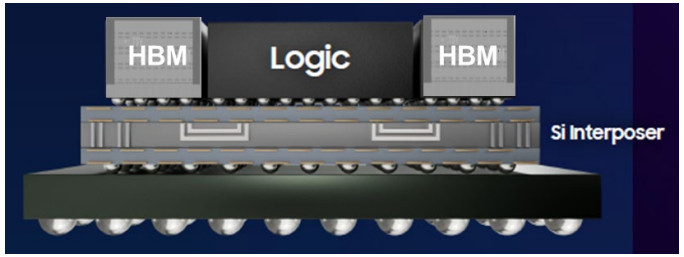
https://www.club386.com/amd-instinct-mi300-architecture-speaks-to-massive-ai-performance/

Introduction

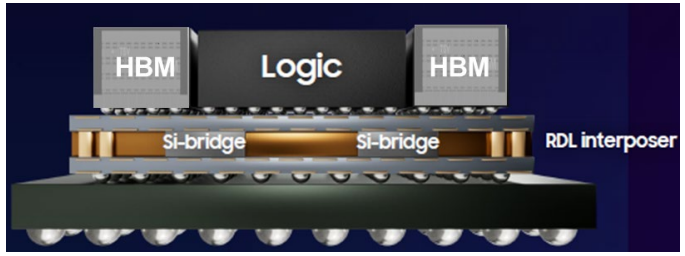
Advanced packages on market

https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10195617

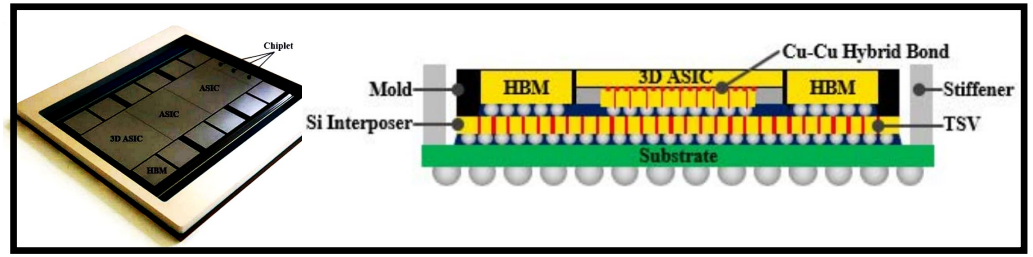
Smaller interconnects; Higher performance; Lower power consumption



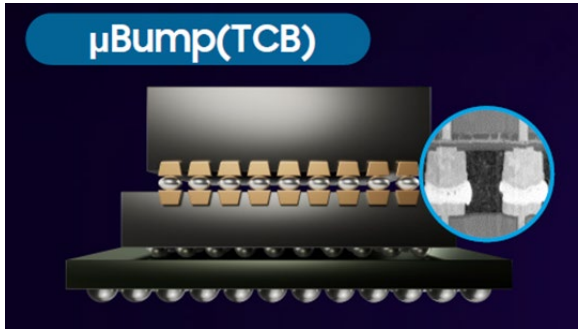
I-Cube S: Si interposer from Samsung



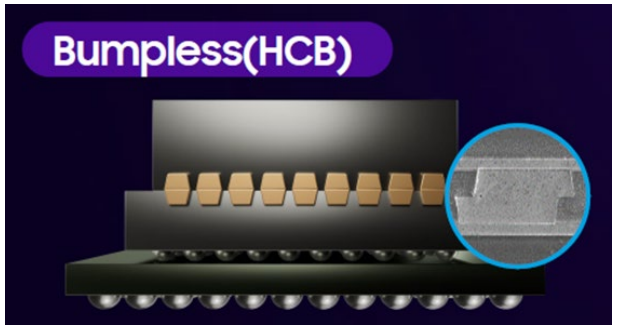
I-Cube E: Embedded Si bridge RDL interposer from Samsung



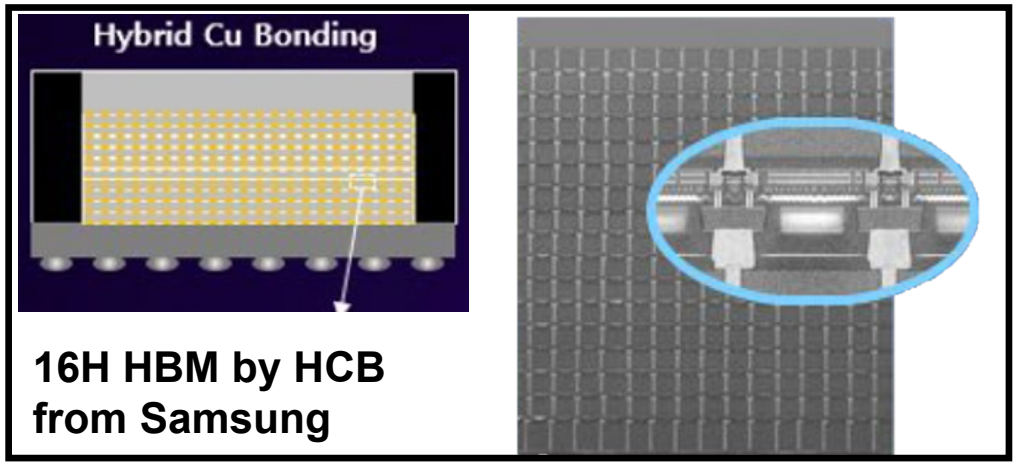
3.5D packaging hybrid bonding 3D chips on Si interposer from Samsung



X-Cube: logic to logic die stacking- µBump from Samsung



X-Cube: logic to logic die stacking- Hybrid Cupper Bonding Samsung

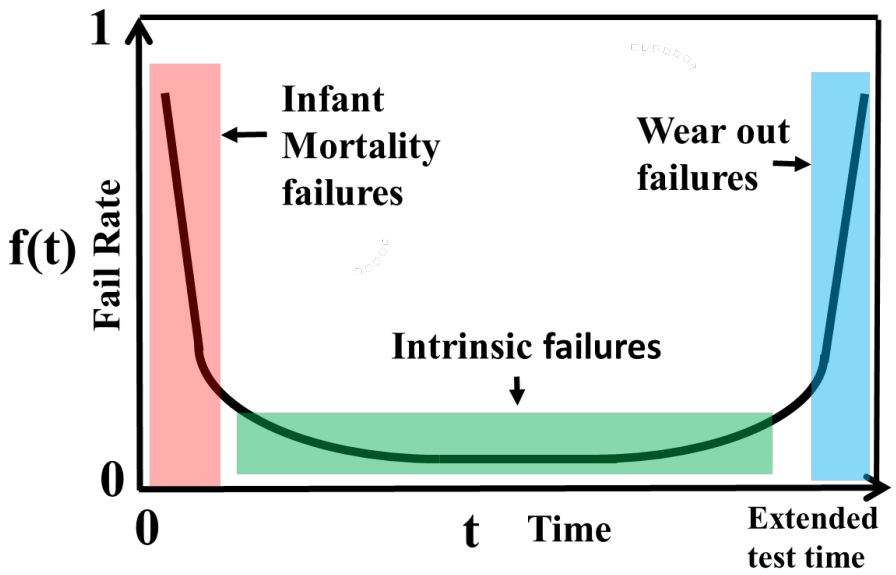


16H HBM by HCB from Samsung

W. Kim, "Advanced Packaging in the Era of HPC and AI" Seventh Annual Symposium on Heterogeneous Integration, February, 2024.
https://ieeetv.ieee.org/video/heterogeneous-integration-platform-for-next-generation-computing-beyond-moore

Quality and Reliability Concerns

3D Microelectronic Packaging: From Architectures to Applications, 2nd edition, Springer, 2021, ISSN 1437-0387



Schematic of Bathtub curve showing failure rate versus reliability test time

- **Product Use Condition**
- **Reliability Tests:**
  - ✓ Preconditioning (PC) Test
  - ✓ Temperature Cycling (TC) Test
  - ✓ Baking Test
  - ✓ Unbiased Highly Accelerated Stress Test (UHAST) and Biased Highly Accelerated Stress Test (BHAST)
  - ✓ Interconnect Electron Migration (EM) Test
  - ✓ Thermal Test

Quality and Reliability Concerns

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Failure Mode examples

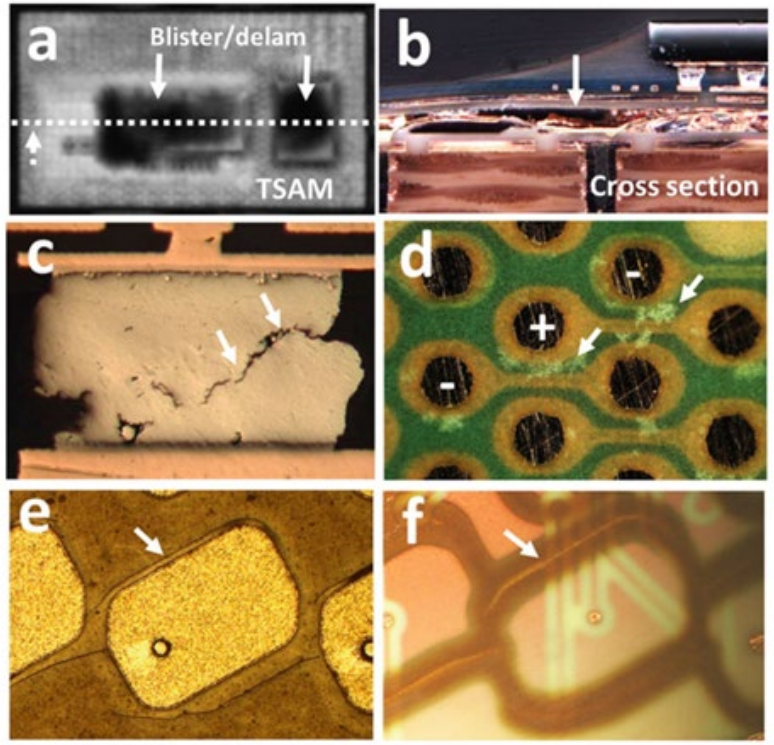
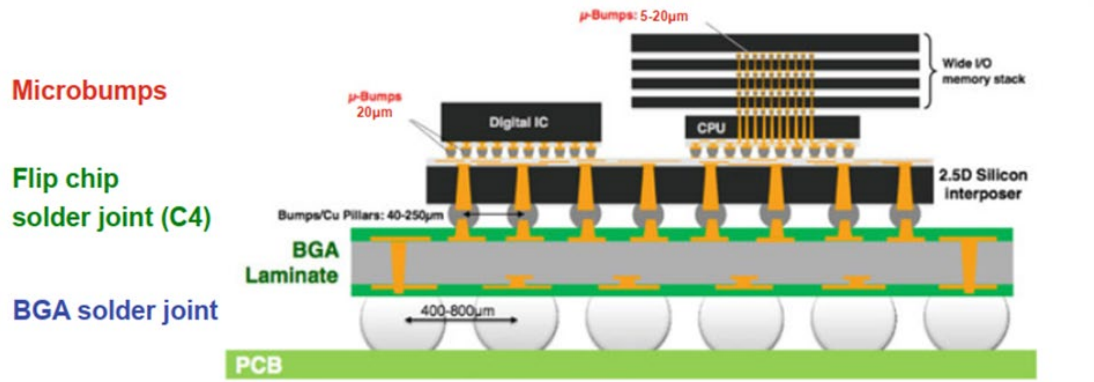
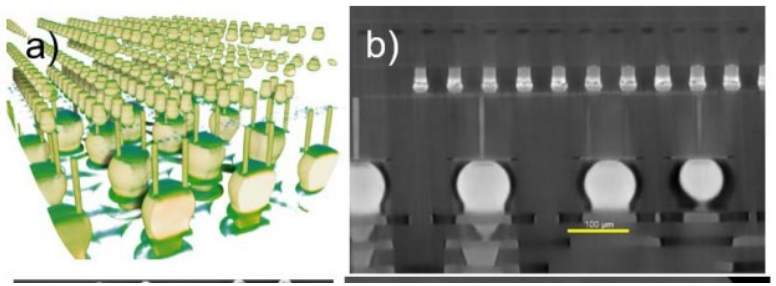


Fig. 18.33 (**a**), (**b**) The TSAM and cross sectional optical image of big substrate blisters in a package post PC test due to "popcorn", respectively. (**c**) A typical fatigue crack in MLI solder joints post extended TC tests. (**d**) Cu dendrite between the adjacent Cu pads of FLI solder interconnects with different polarities post extended BHAST tests. (**e**), (**f**) Substrate solder resist layer crack post extended Bake Tests, which lead to substrate trace cracks





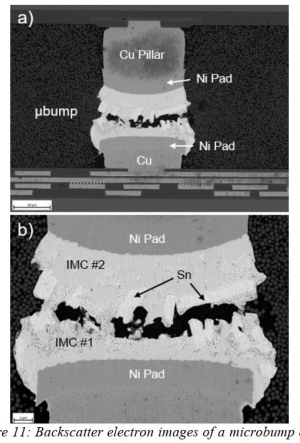


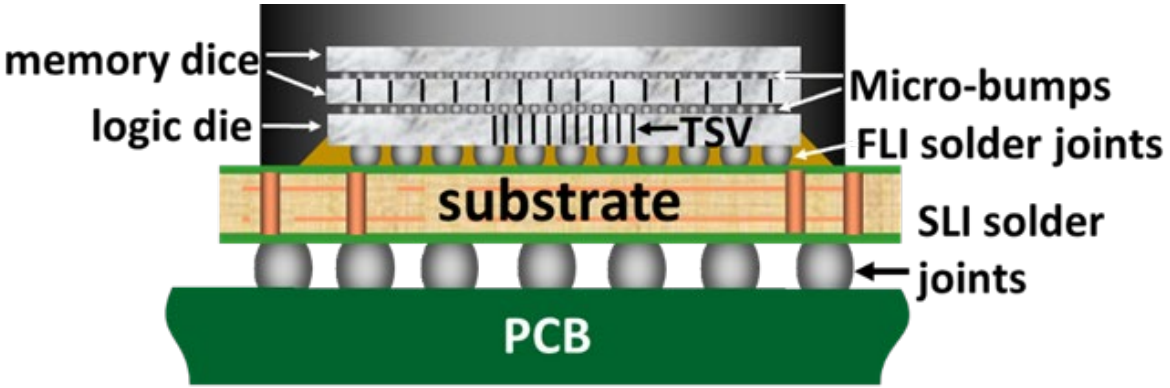
Figure 11: Backscatter electron images of a microbump crack imaged at 5 kV acc. voltage with an annular backscatter detector. a) 37 nm/pixel; Scale bar: 10 μm. b) 15 nm/pixel; Scale bar: 2 μm.

Why FA?

- Identify defects of Electrical Device Failures (post reliability tests or at End of Line)
- Investigate root cause of the failures (Propose failure mechanisms)
- Provide data feedbacks and solution paths for problem solving.

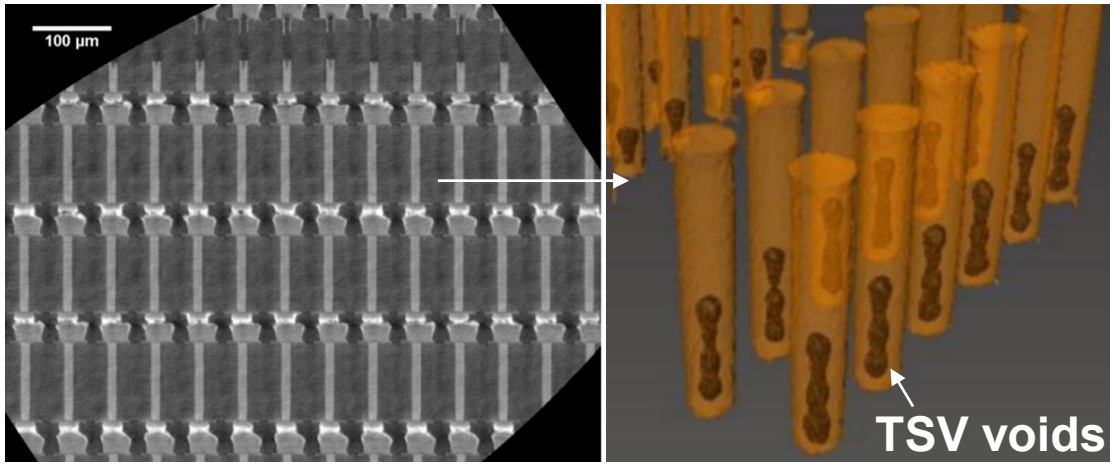
Fault Isolation and Failure Analysis Challenges

Challenges from Technical Point of View



- **Physical Failure Analysis:** 1) artifact free 2) revealing fine features in a large area
- **Material analysis:** 1) ppm level contamination at interface; 2) organic materials with sub micron resolution

- **Electrical Failure Analysis:** 1) Multiple failures in one unit. 2) Each failure needs x, y, and z identification
- **Imaging:** 1) Non-destructive. 2) high resolution 3) large field of view



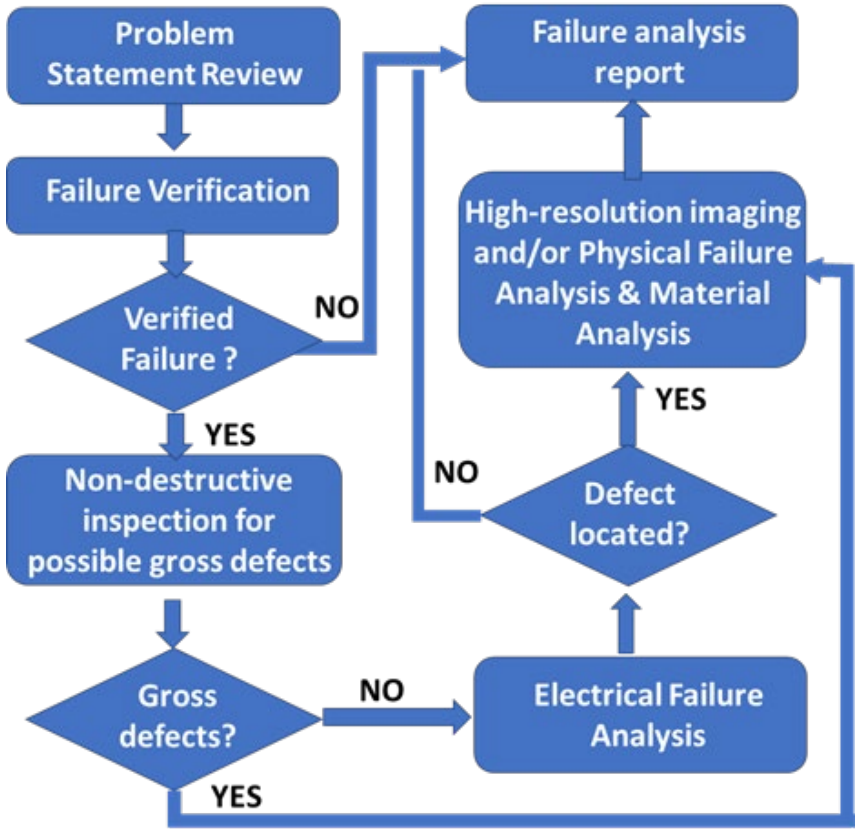
Challenges from Business Point of View

Demand of Short product develop timeline; High volume manufactory; Cost saving

- **Low Cost**
- **Short Through Put Time (TPT)**
- **High Success Rate**

Fault Isolation and Failure Analysis Approaches

Generic failure analysis flow



Schematic of failure analysis flow.

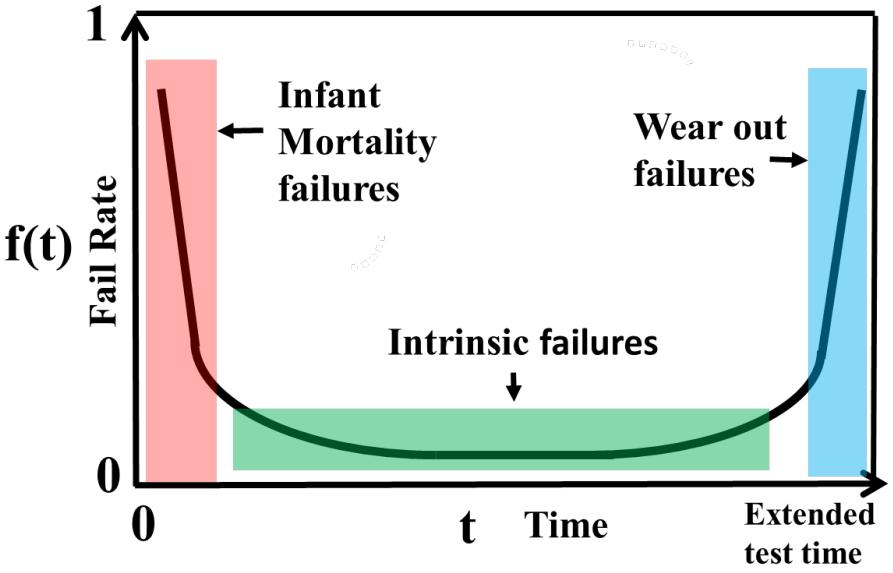
- **Problem statement review**
- **Failure verification,**
- **Non-destructive investigation**
- **Electrical Failure Analysis**
- **High resolution imaging or Physical Failure Analysis** (Sample Preparation; Defect Imaging; Material Analysis)

Fault Isolation and Failure Analysis Approaches

FA workflow: Problem Statement Review

The most critical step for successful failure analysis

- **Failure occurrence condition and history—**EOL? Post Reliability test? Customer Return?
- **Failure rate analysis ----**Failure rate at EOL; Failure rate vs Reliability test time
- **Historical failure analysis data leveraging**

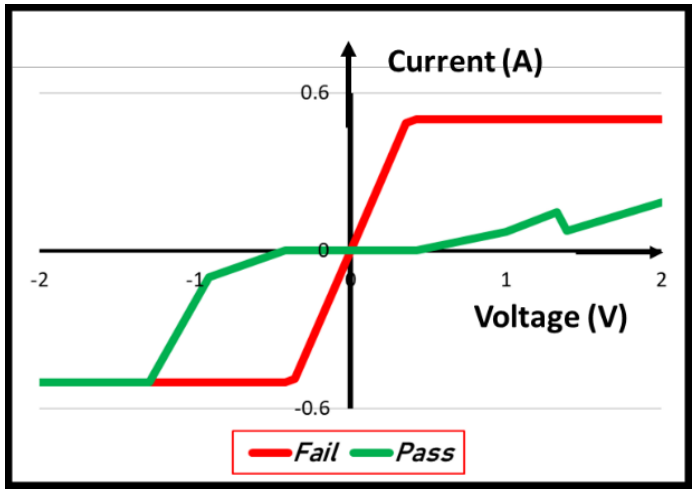


Schematic of Bathtub curve showing failure rate versus reliability test time

Fault Isolation and Failure Analysis Approaches

FA workflow: Failure Verification

Common tester contact issues, test program immaturity, and failure intermittency



I-V curve trace from a passing (in green) and a failing unit (in red).

- **Parametric Failures —** I-V Curve trace; Resistance or Current measurement; comparing with those from a test good device
- **Functional Failures —** Debug testers and test programs; compare results from “failing” vs “passing”

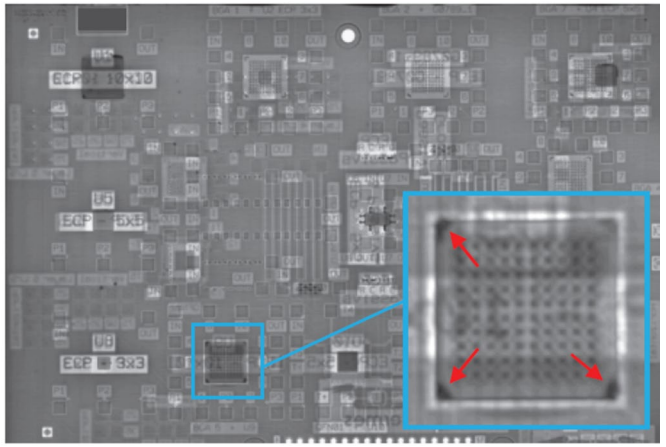
Fault Isolation and Failure Analysis Approaches

FA workflow: Non-destructive investigation

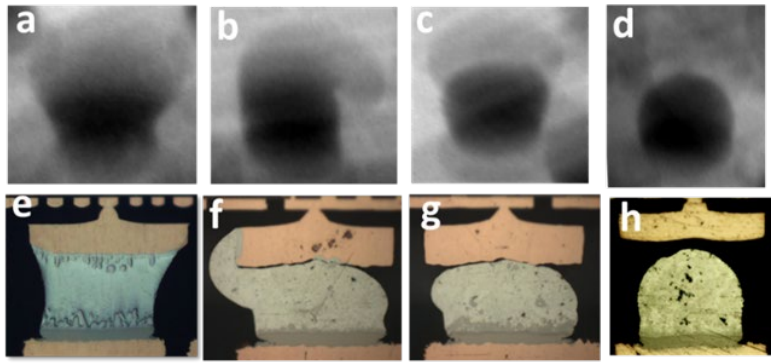
Non-destructive; large field of view; inspect the whole "Area of Interest (AOI)"

- **Optical Microscopy**
- **Infrared (IR) Imaging**
- **Scanning Acoustic Microscopy (SAM)**
- **2D X-ray**

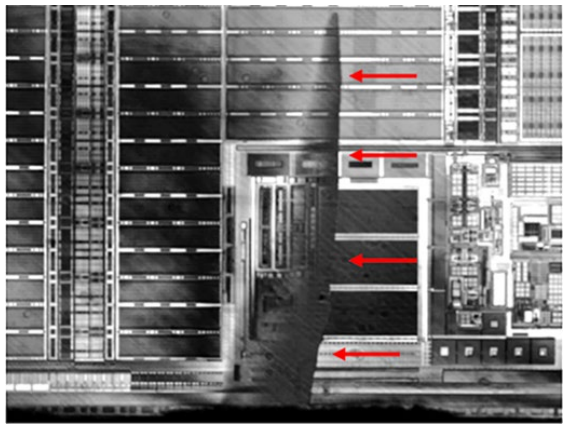
Fast TPT for units having Gross Defects



TSAM of a PCB with embedded chips showing defects in one embedded chip



2D X-ray images taken non-destructively and the corresponding optical images of FLI solder interconnects cross sectioned post 2D X-ray imaging: (a) & (e) normal or defect free, (b) & (f) partial non-wet, (c) & (g) complete non-wet, (d) & (h) non-contact open



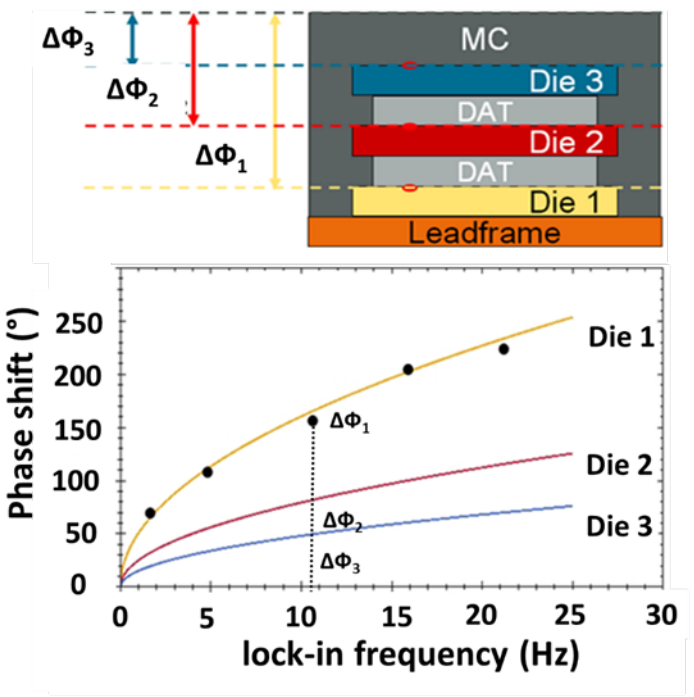
IR image taken from die backside showing internal die cracks highlighted by the red arrows

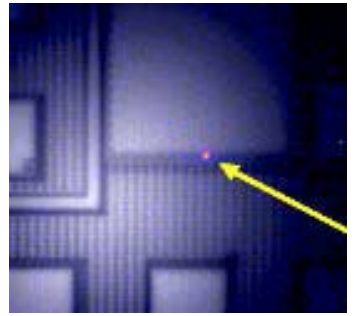
Fault Isolation and Failure Analysis Approaches

FA workflow: Electrical Failure Analysis (EFA)

locate tiny defects in very complicated electrical systems

- **Parametric failures** —Time-domain reflectometry (TDR), Lock-In Thermography (LIT), Magnetic Field Imaging (MFI), Micron probing
- **Functional failures----**Optical fault isolation tools, E-beam imaging and probing techniques, nanoprobing
- **Non-destructive, High resolution, providing x, y, z location of defects**





Measurement results of Lock-in frequency vs phase shift curves from reference units with short failures at die 1, die 2, and die 3 of a package with stacked die configuration showing in dots compared to a calibrated simulation model (lines)

Fault Isolation and Failure Analysis Approaches

FA workflow: High resolution imaging

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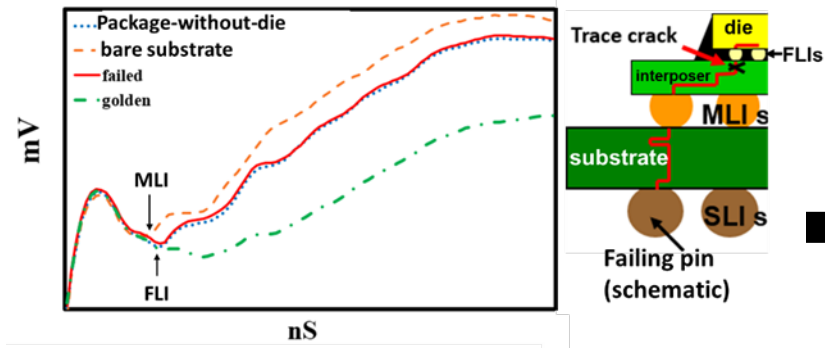
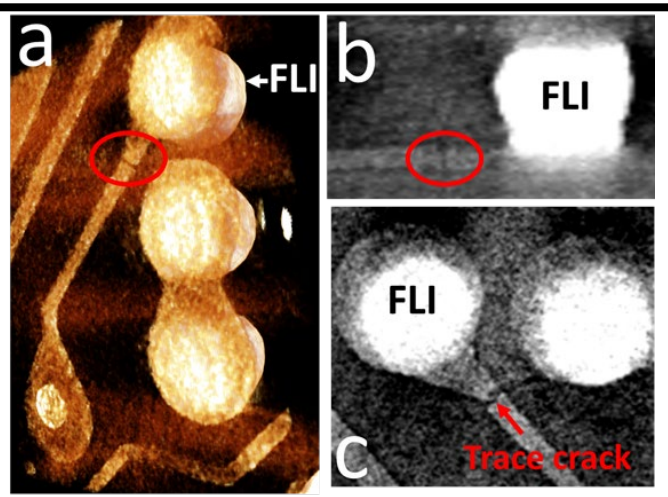
High-resolution imaging of a relatively small AOI defined by Electrical Failure Analysis

- **3D X-ray Computed Tomography (CT)**
- **High resolution SAM**
- **High resolution IR imaging**
- **Non-destructive; good for multiple failures in one unit**

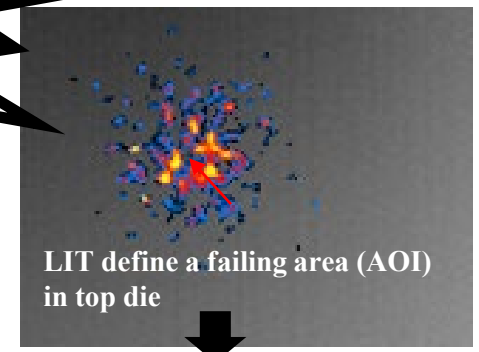
Fast TPT
for units with known failure mechanism

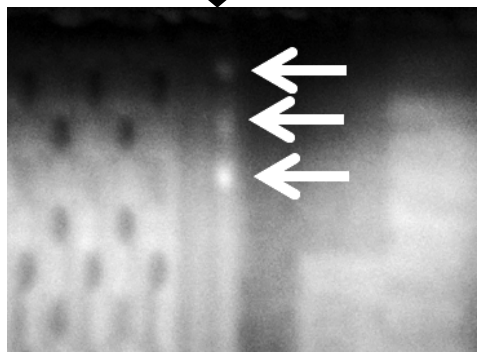


TDR spectra from a failed unit, a golden unit, a bare SIP substrate, and a SIP package without FPGA die, showing the open failure is close to the FLI solder joint in the FPGA package of a SIP package



3D view, (b) virtual cross-sectional view, and (c) virtual planar view of the 3D X-ray CT showing trace crack in a package





CSAM image of the AOI showing three "white spots" (Si layer delam)

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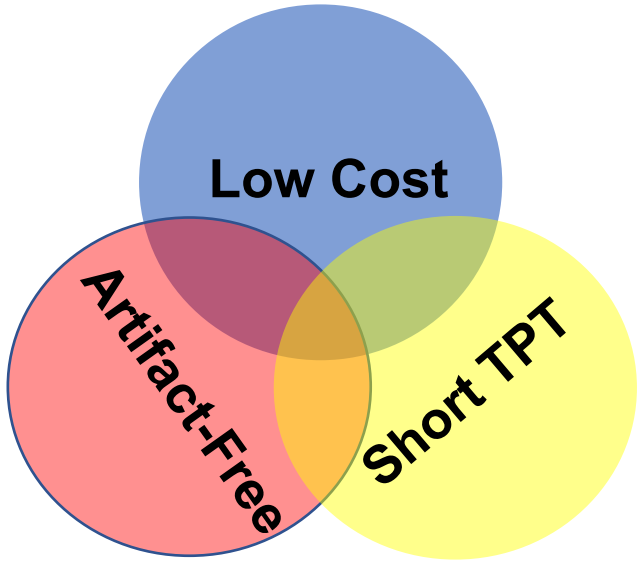
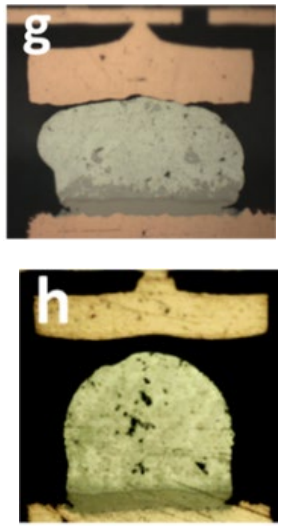
FA workflow: Physical Failure Analysis (PFA)-Sample Preparation

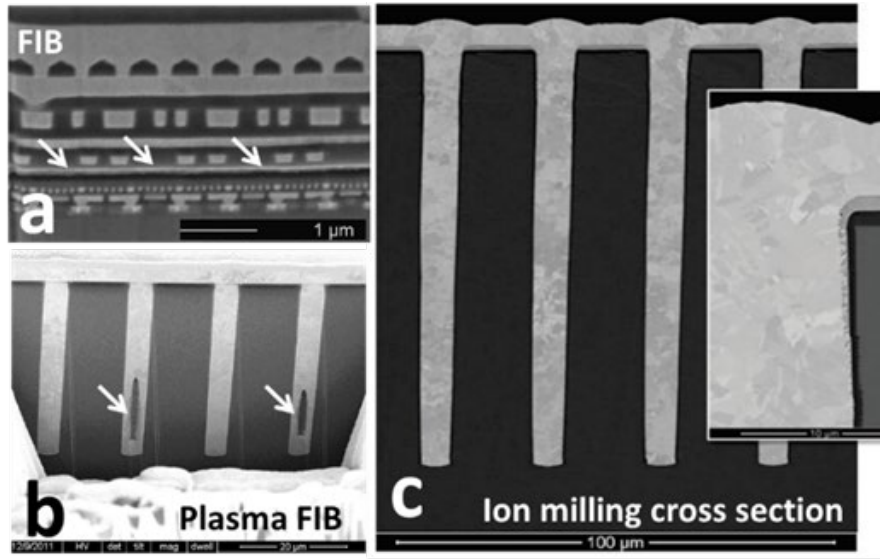
PFA --1) Disclosing the details of defects for root cause investigation
2) Utilizing techniques of sample preparation, defect imaging, and material analysis.

- **Mechanical Polishing** (cross section or planar grinding; low cost; faster TPT; operator dependent)
- **Laser ablation** (relatively fast TPT; low spatial resolution; laser induced thermal damage)
- **FIB** (Ga) **and Plasma-FIB** (Xe)
- **Broad-beam Ion milling** (low cost)





Mechanical polishing



(a). SEM image of Si layer ILD delamination by FIB cross section. (b) and (c). SEM images of TSVs by plasma FIB and Ion milling cross section, respectively

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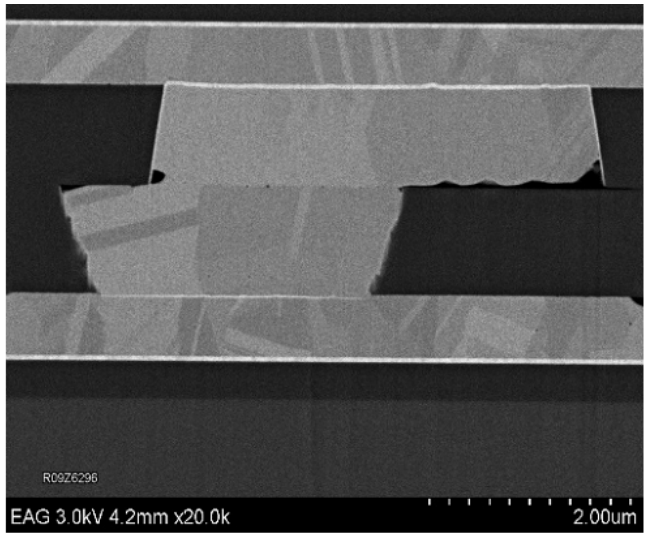
FA workflow: PFA-Defect Imaging

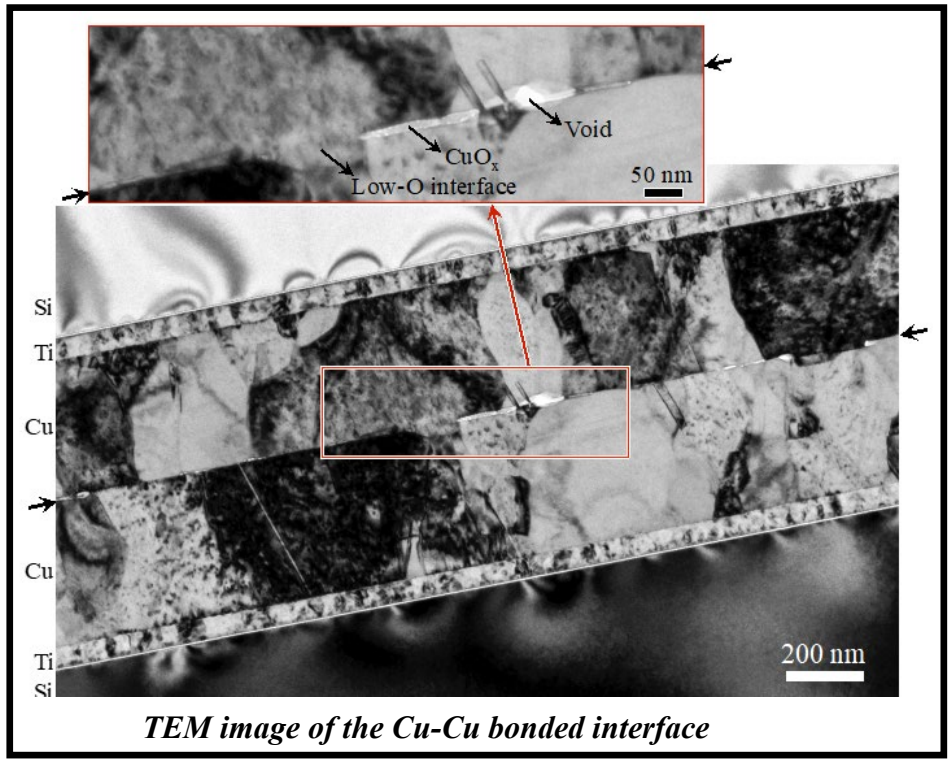
Reveal subtle details of the defects for root cause understanding

- **Optical and IR microscopy**
- **Scanning Electron Microscopy (SEM)**



SEM cross-sectional image of bump-less Cu-Cu bonded structure

- **Transmission electron microscopy (TEM)**



TEM image of the Cu-Cu bonded interface

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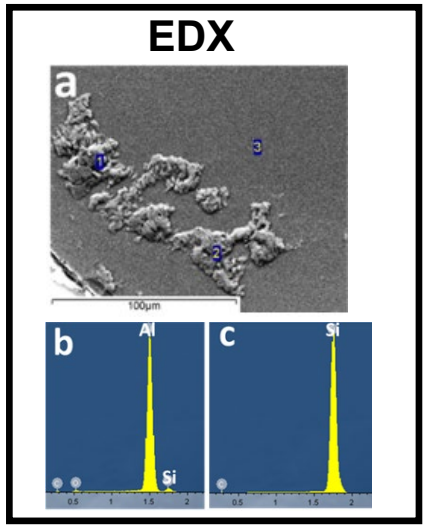
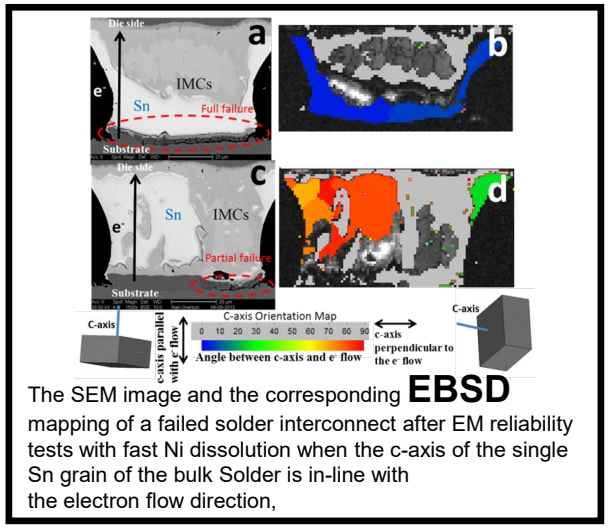
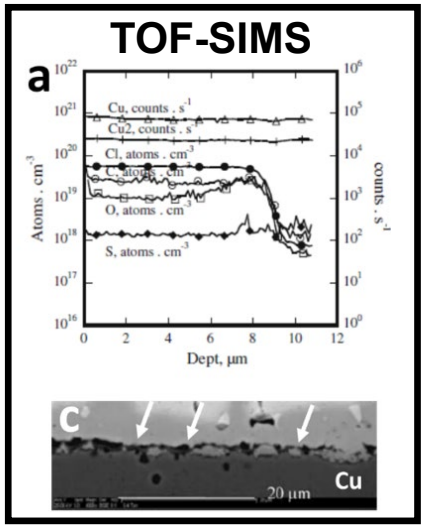
FA workflow: PFA- Material Analysis

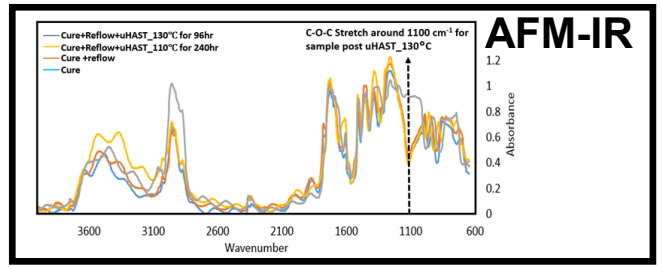
Crucial for failure mechanism hypothesis, validation, and solution path identification

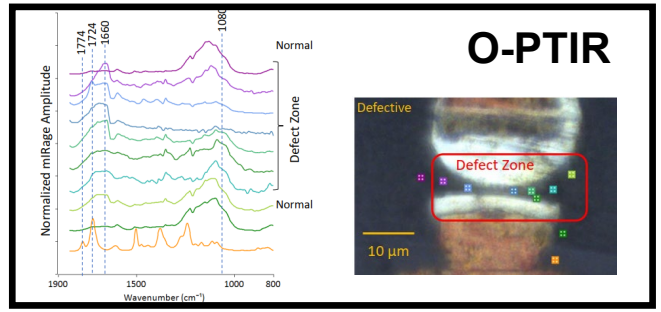




The SEM image and the corresponding **EBSD** mapping of a failed solder interconnect after EM reliability tests with fast Ni dissolution when the c-axis of the single Sn grain of the bulk Solder is in-line with the electron flow direction,





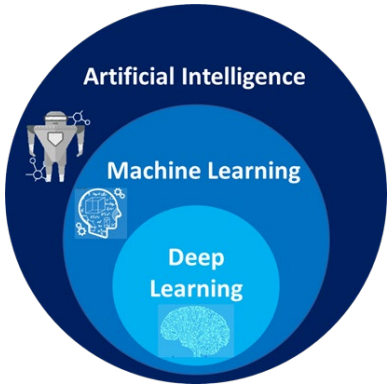


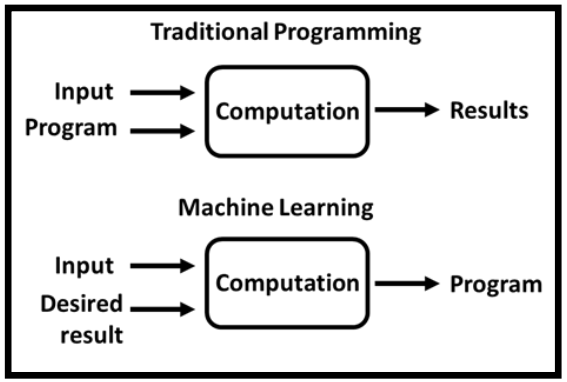
www.microscopy-today.com • 2020 May, P29

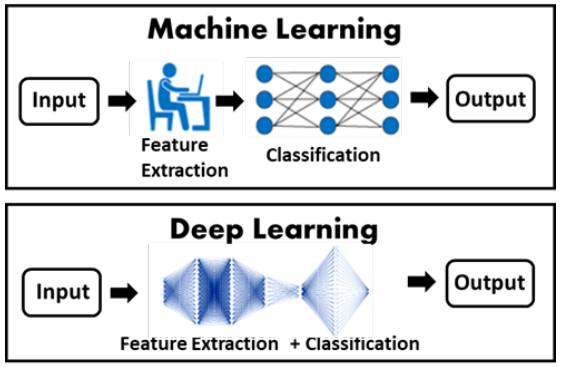
- **Energy-dispersive X-ray spectroscopy (EDX)** (Elemental information)
- **Electron Backscatter Diffraction (EBSD)** (crystallographic orientation)
- **X-ray Photoelectron spectroscopy (XPS) &Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS),** (surface or interface ppm level contamination; chemical state)
- **Fourier Transform Infrared spectroscopy (FTIR), Atomic Force Microscopy based Infrared spectroscopy (AFM-IR), and Optical Photothermal Infrared Micro spectroscopy (O-PTIR)** (organic material identification, sub-micron, liquid, etc.)

Future Development Trends

Automation and Artificial Intelligence (AI) applications in Failure Analysis

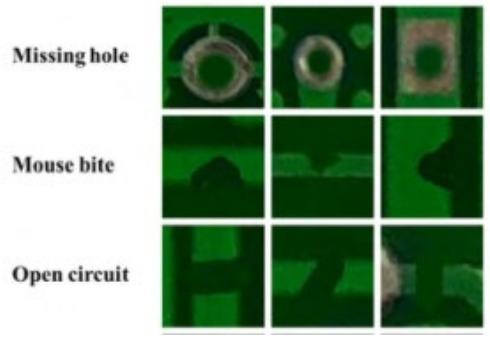




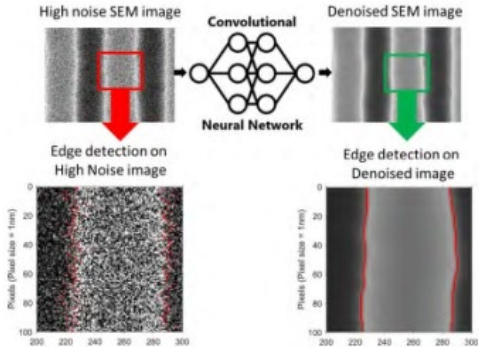


- **Combination of Automation and AI in imaging and Fault isolation.**
- **Failure mode identification and prediction** (Pattern recognition; Classifying FA report)

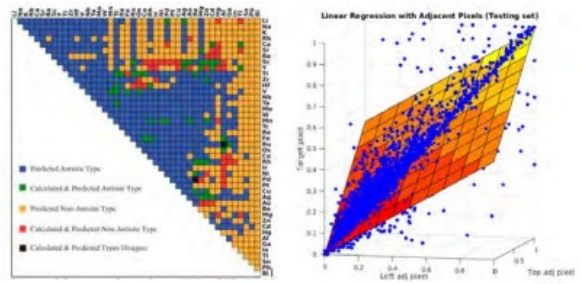
M. Kögel et. al, ISTFA 2021



Defect detection and classification



Noise reduction in SEM/TEM/SAM images



Failure mode identification by clustering and pattern recognition

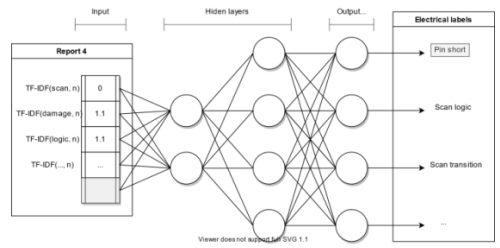
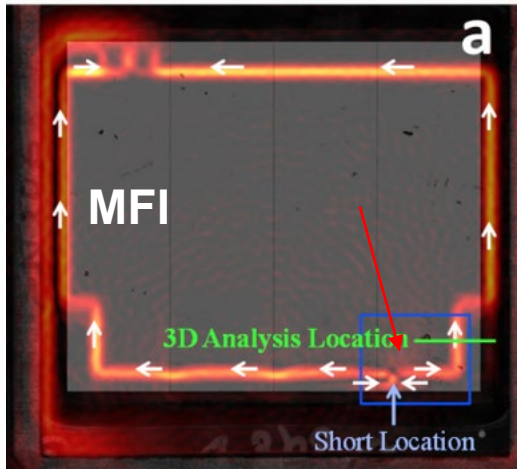


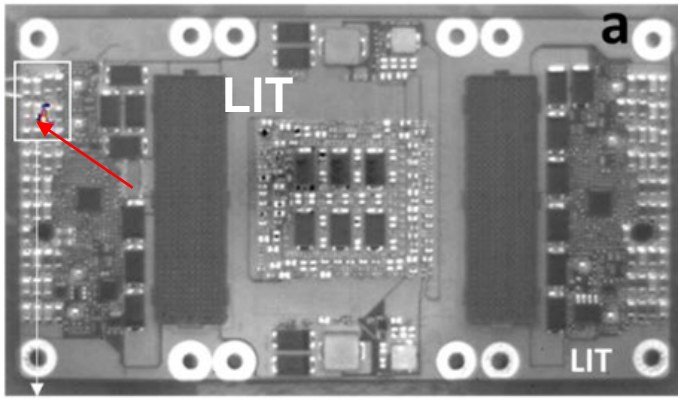
Figure 2. Structure of a conventional DNN for the example with the Report 4 as input

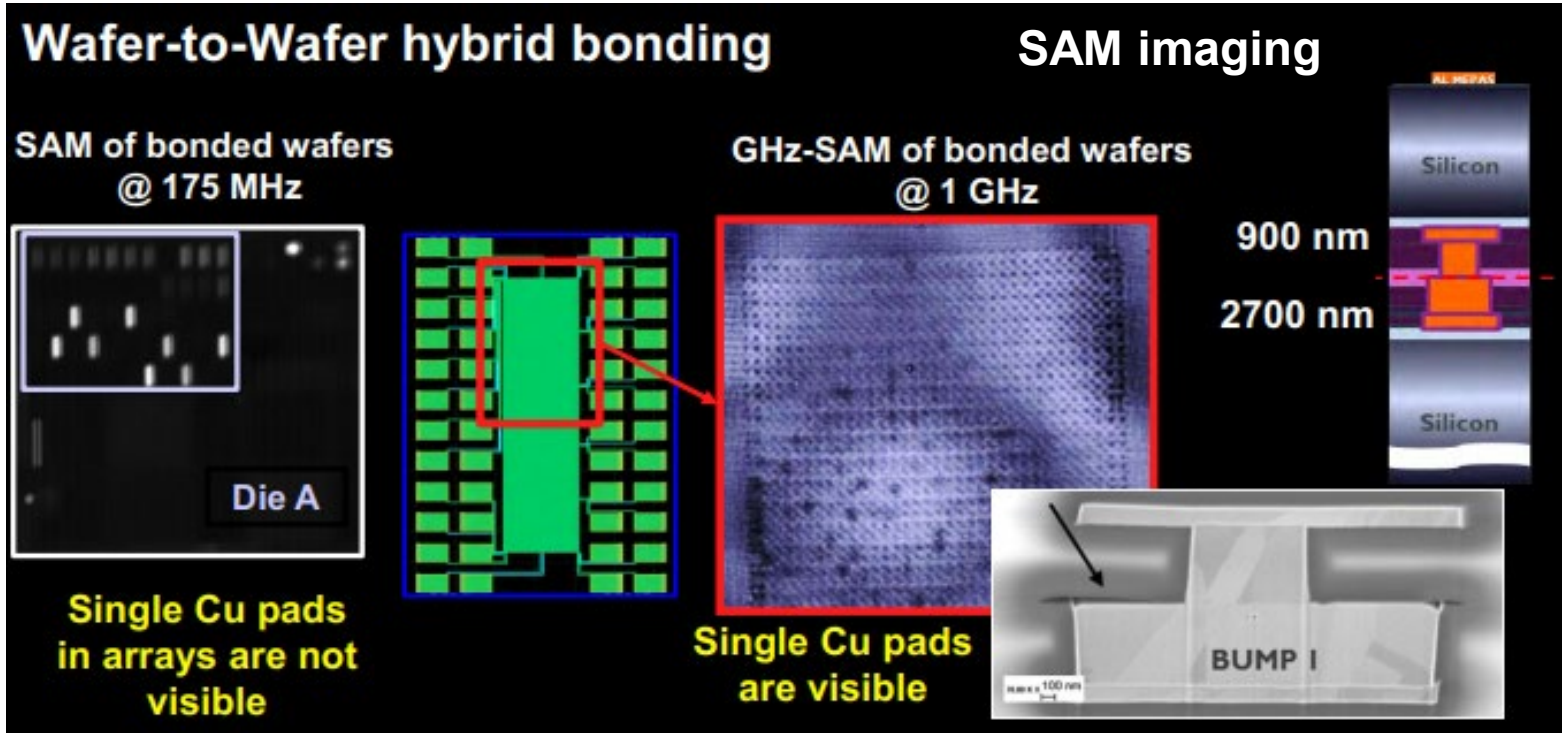
Failure Analysis report Classification and Failure mode prediction

Future Development Trends

Fast, High resolution, and Non-destructive Fault isolation and imaging techniques





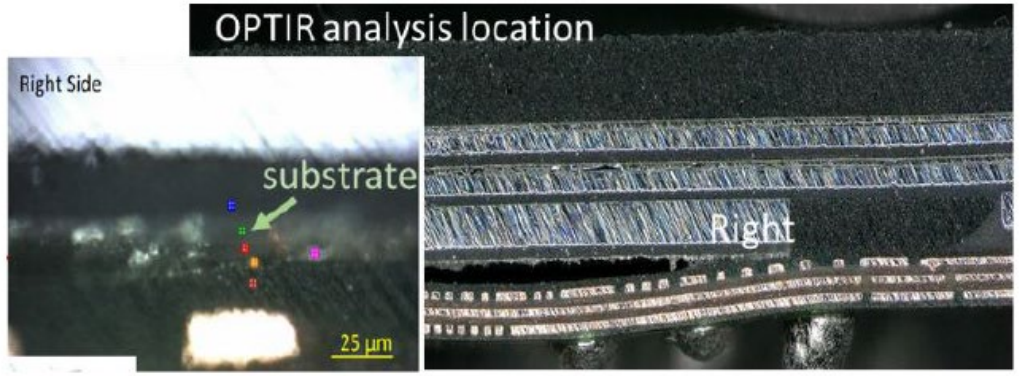


T. Gandhi, Microelectronics Failure Analysis Desk Reference 7th edition, ASM International, 2019

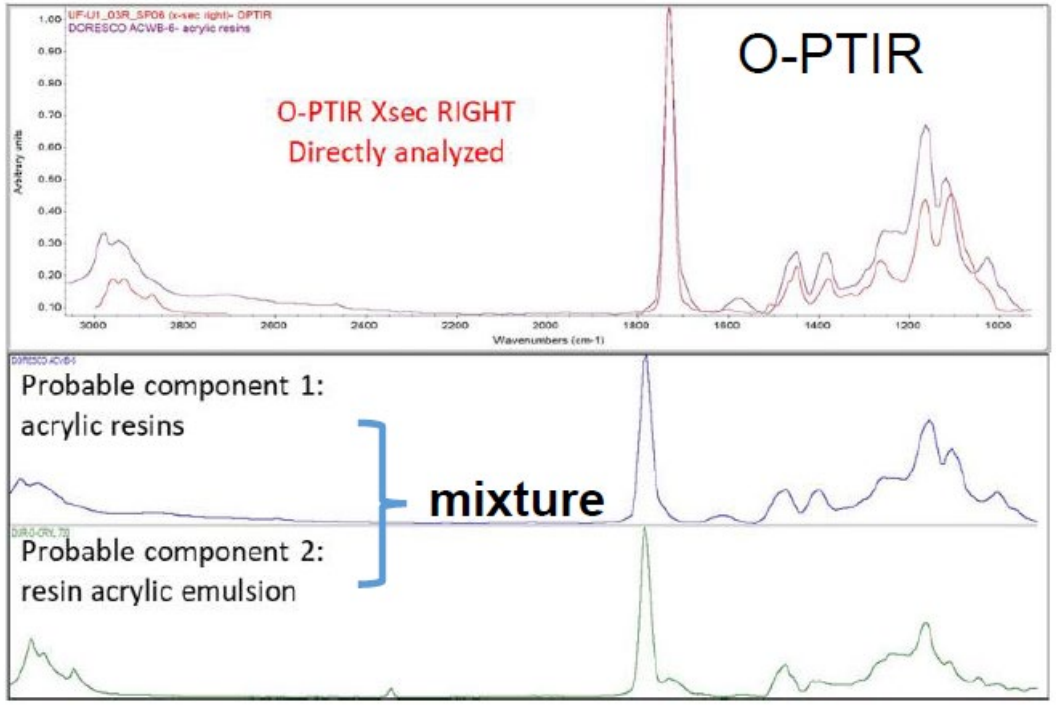
De Wolf et. al, ISTFA 2018

Future Development Trends

Sensitive Material Analysis tools for sub-micron resolution with minimal or no sample preparation needs



O-PTIR analysis on sub-micron Foreign Materials



Lau, 2023, IPFA, Paper 116; 10.1109/IPFA58228.2023.10249138

Future Development Trends

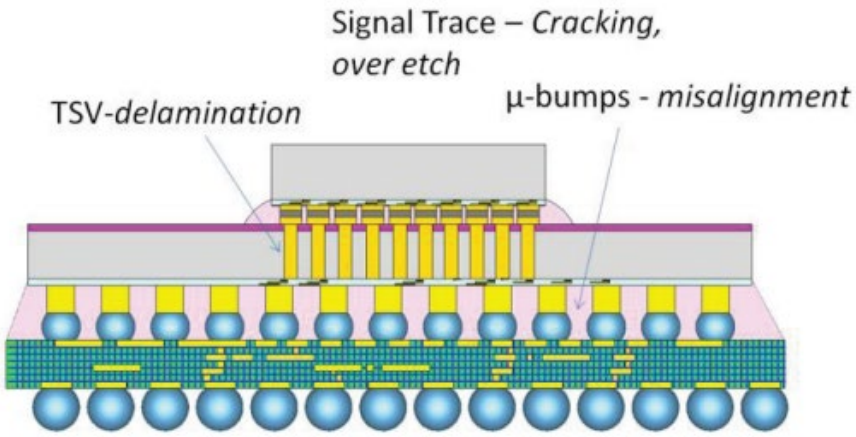


Fig. 1: Possible locations in 3D-IC where failure may occur

- Modeling and Simulation assisted FA
- Design for test and FA

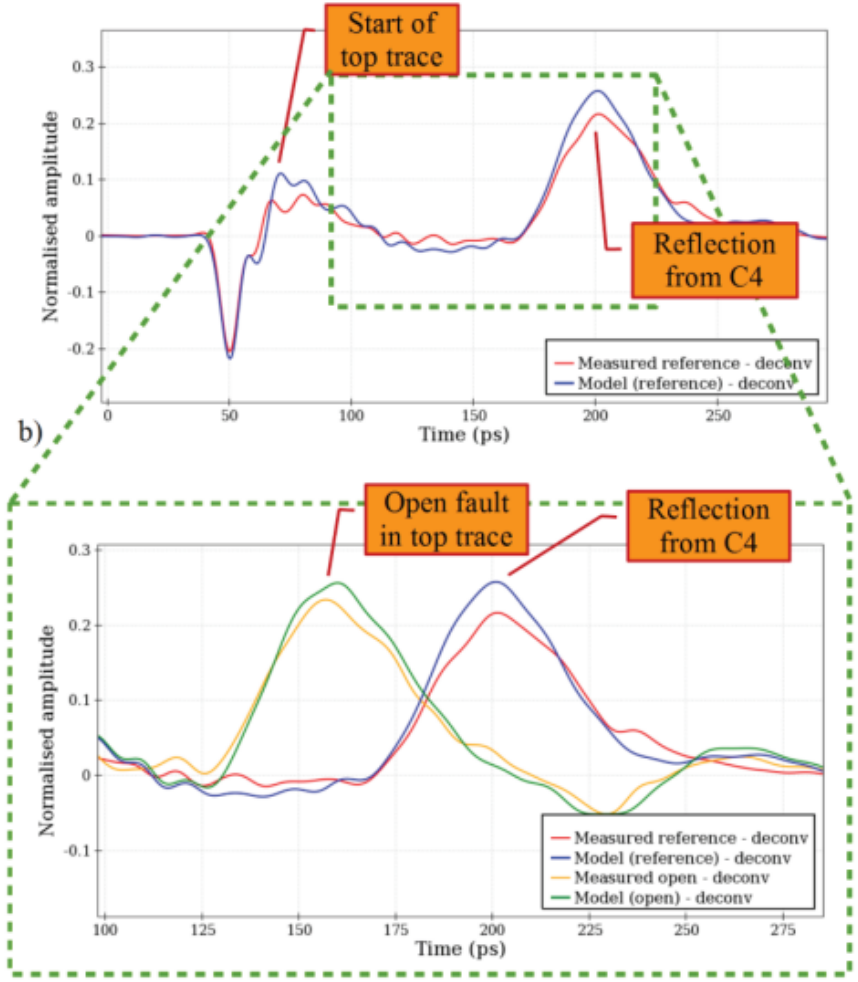


Fig. 4: Comparison of the measured waveform against the optimised EM model. Waveform features are annotated using the time-of-flight information obtained from the voltage monitors.

Emma Kowalczuk et al. IEEE International 3D System Integration Conference, December, 2014

Conclusion

- **Advanced Packaging is the industry trend**
- **FI and FA Challenges and approaches**
- **Automation, AI, and Innovative Techniques to overcome the Challenges**