Accelerating Time To Yield By Means Of Advanced eBeam Technology and A Compact Engagement Model

Jeong Ho Yeo, Aviram Tam

PDC, Applied Materials

FCMN 2026, March 18th 2026

APPLIED MATERIALS™

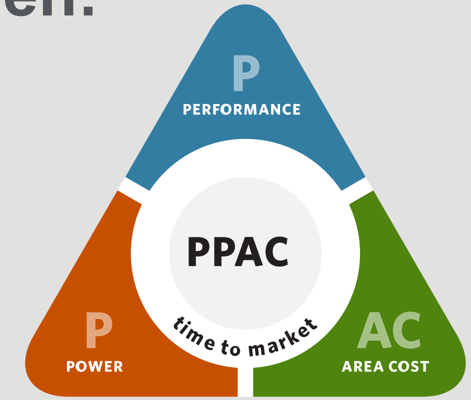
AGENDA

- Introduction
- eBeam Playbook
- Accelerated Workflow
- Summary

AGENDA

PPACt™ - The New Playbook

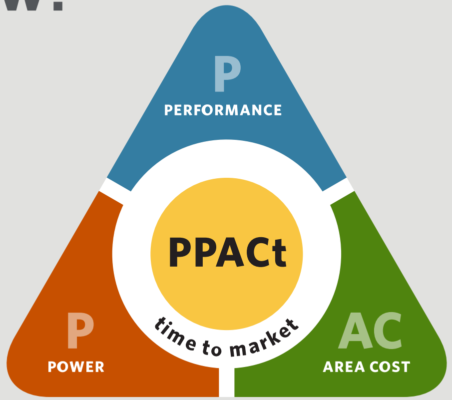
Then:



ENABLED BY

- “Classic” 2D feature shrink
- Materials engineering

Now:



ENABLED BY

- New **architectures**
- New **materials**
- New **structures / 3D**
- New ways to **shrink**
- Advanced **packaging**

Single process step metrology loses correlation to yield/performance

Insufficient relevant Data to Drive Action

t Time to Market has become more critical

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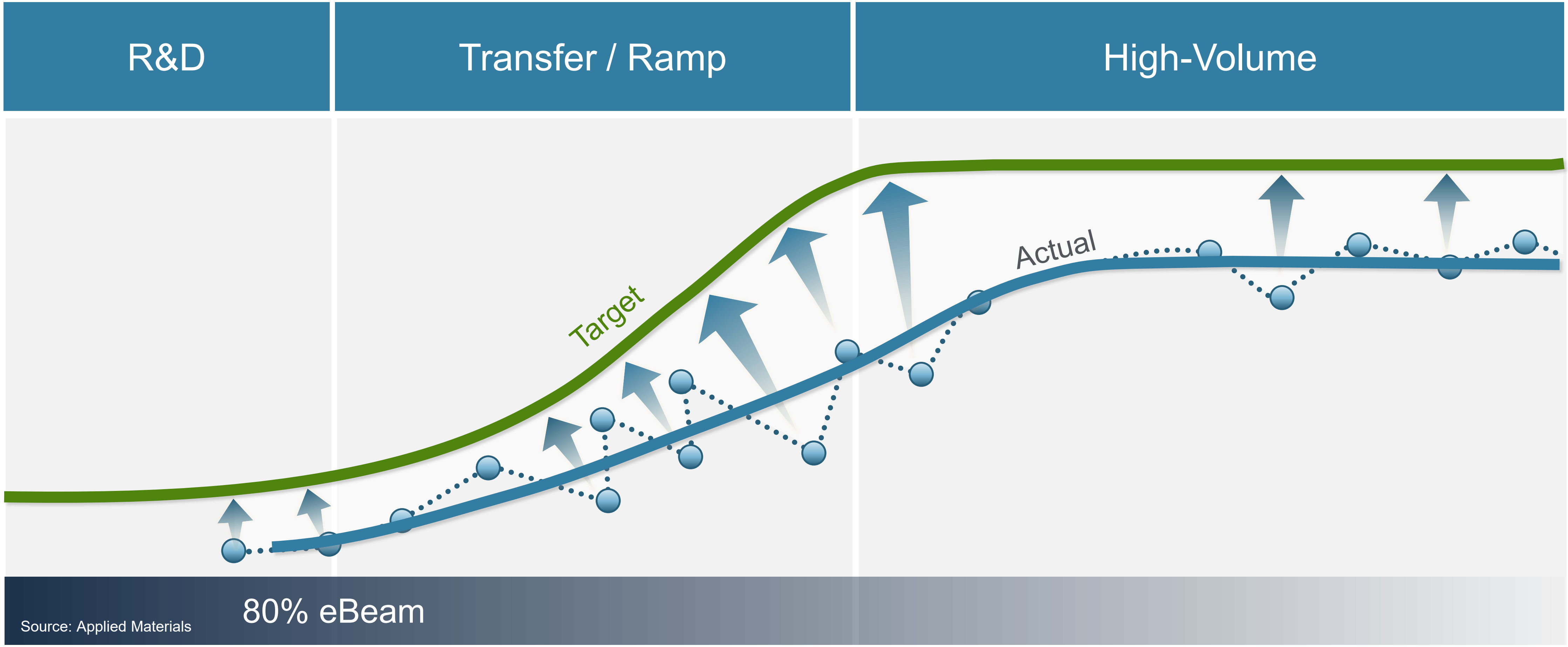
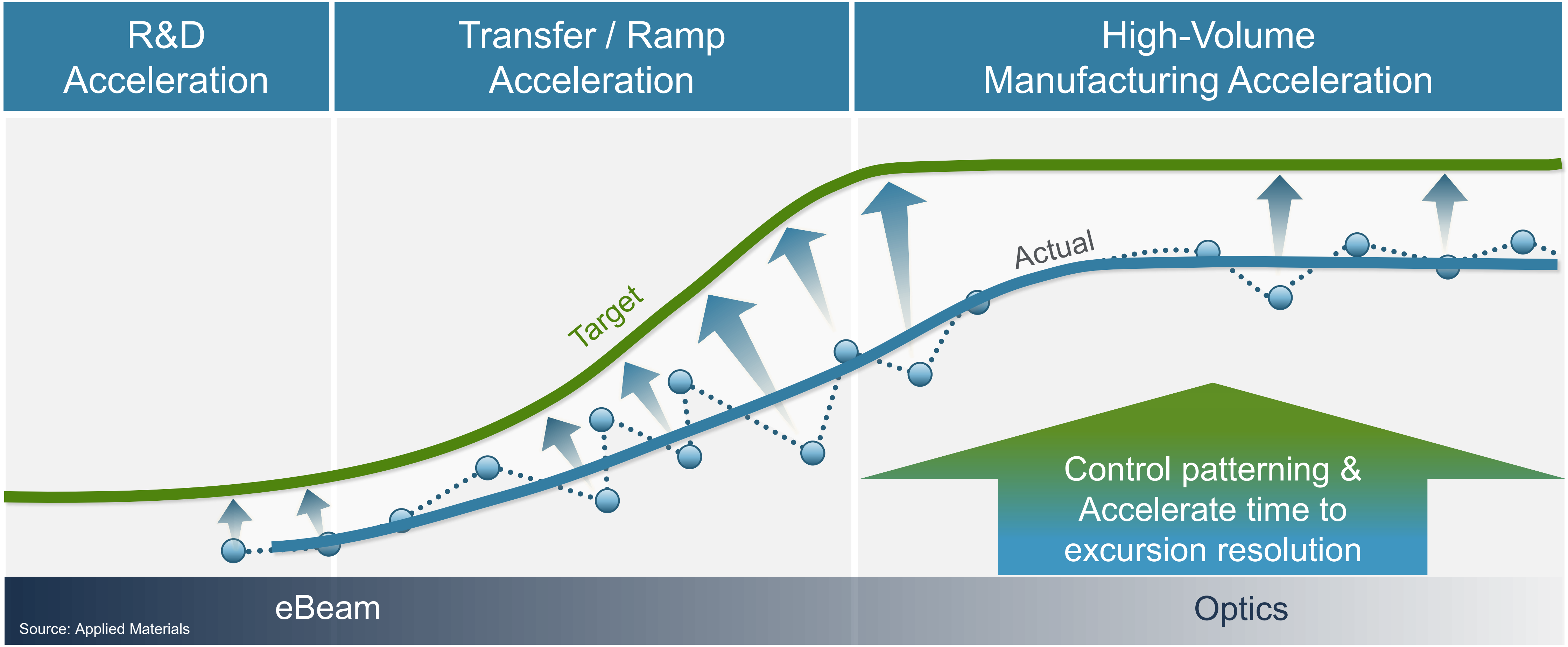
Yield and Time to Yield Challenge Increase with Device Complexity



Source: Applied Materials

eBeam Role



Accelerate R&D and Ramp

Resolution and localized information

AGENDA

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- eBeam Playbook
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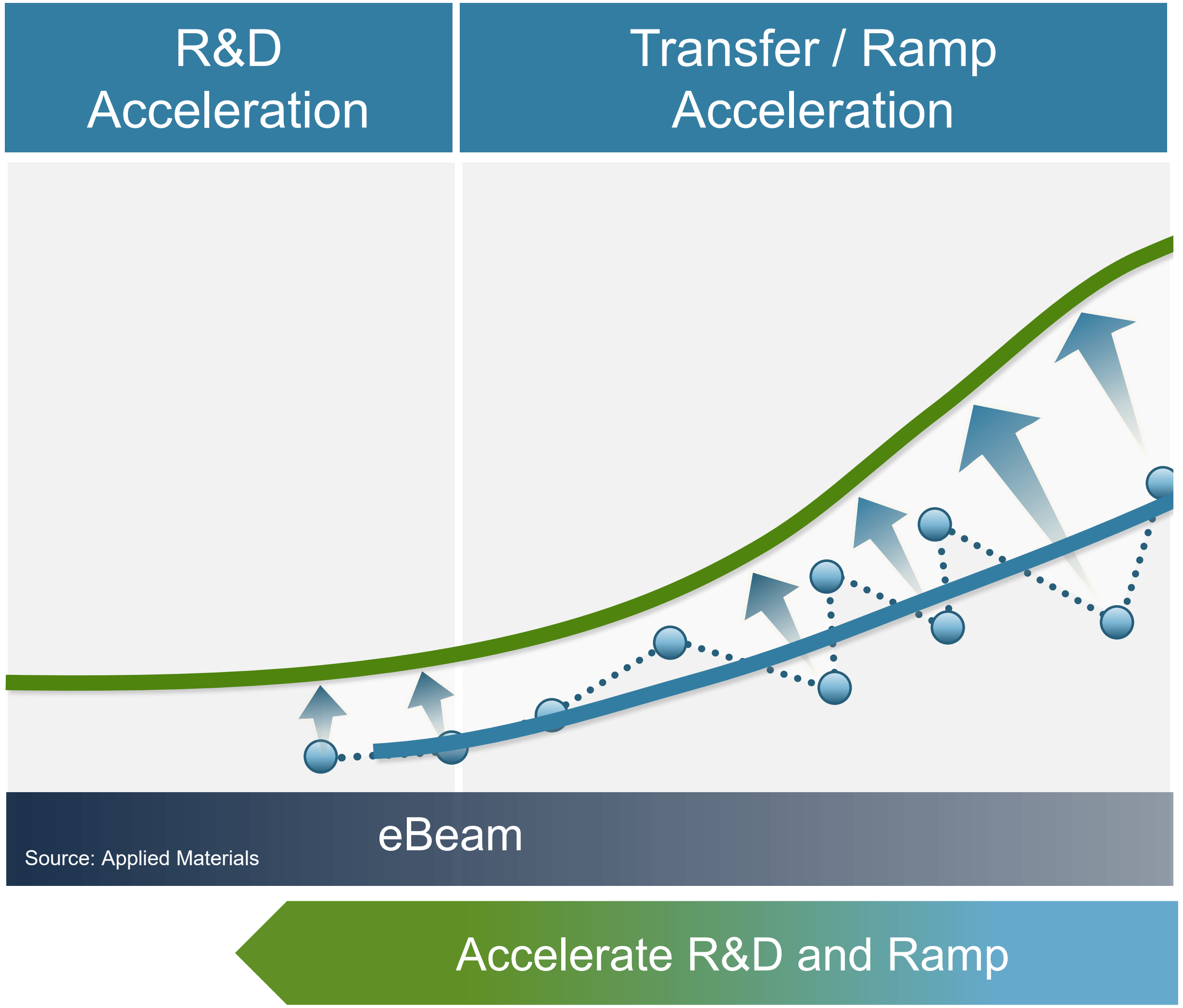
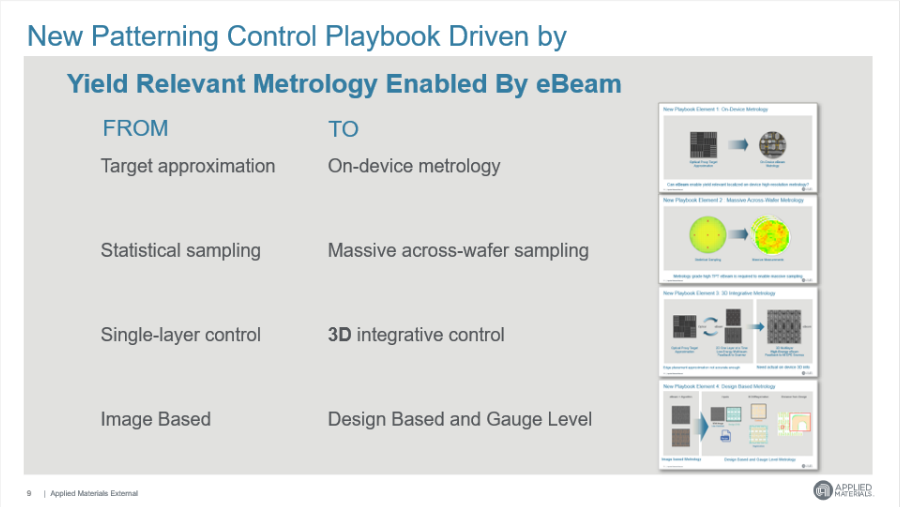
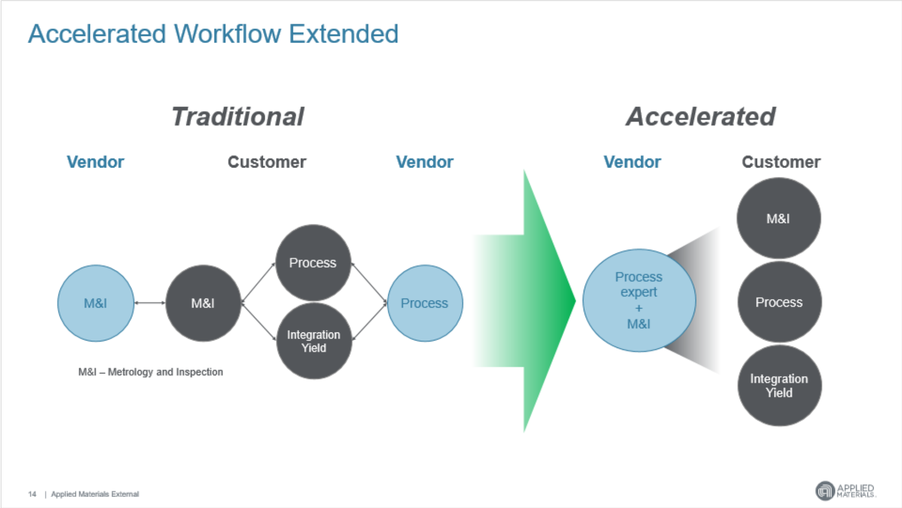
The Million(s) Dollar Question – How Do We Accelerate The Ramp?





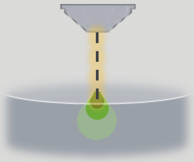


eBeam Imaging Race and Technological Requirements

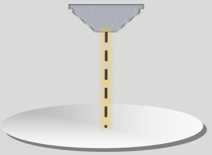
Signal **Relevance**

Reach the Location of Interest

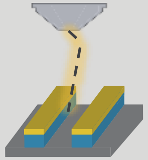
Landing Energy



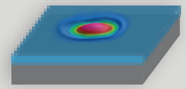
Resolution

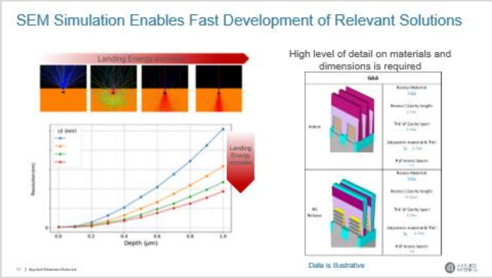


Tilt



Simulation

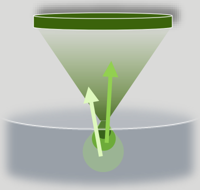




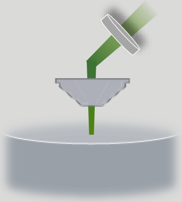
Signal **Extraction**

Collect the electrons that matter

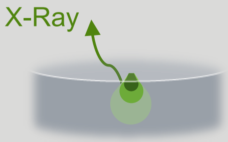
SE/BSE Collection



Signal Manipulation and Filtering



Material Analysis



Signal **Interpretation**

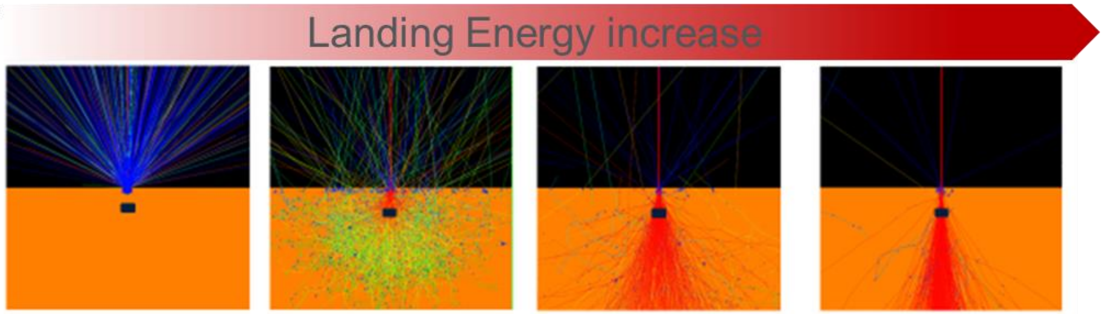
Physics-Algo $x=y^2$

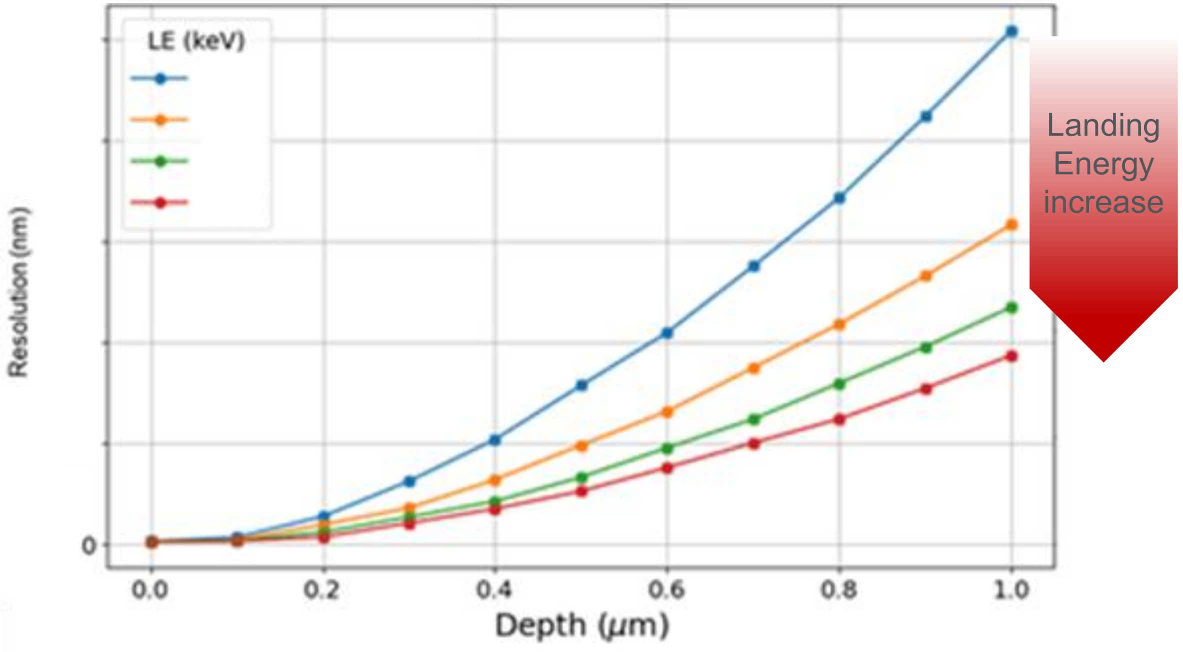
AI, DL, GenAI 

Model-Based 

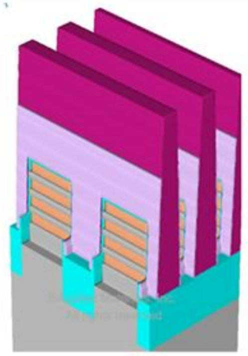
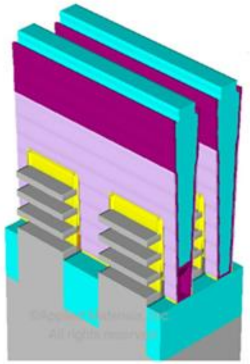
AI = artificial intelligence
DL = deep learning

SEM Simulation Enables Fast Development of Relevant Solutions





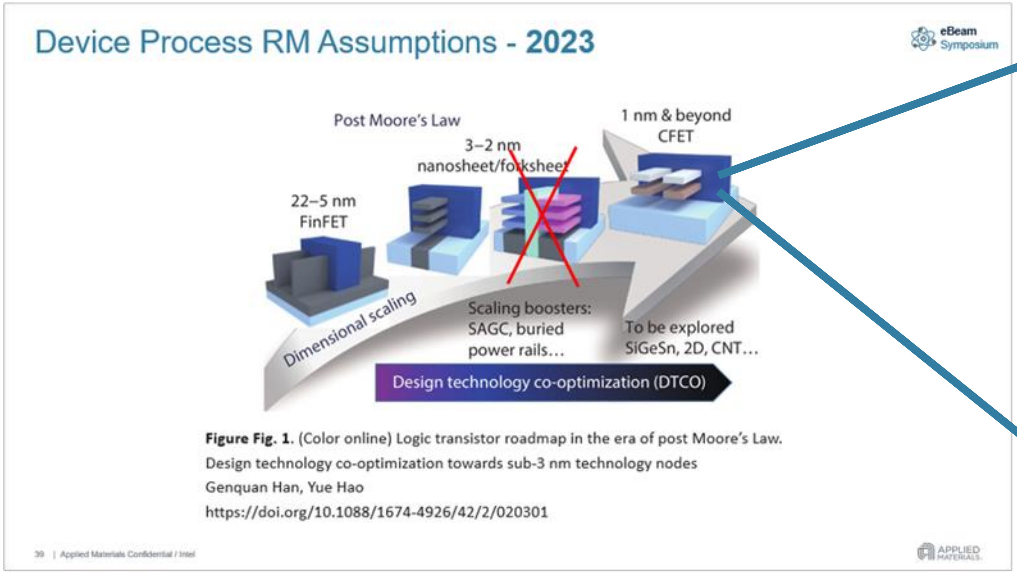
High level of detail on materials and dimensions is required

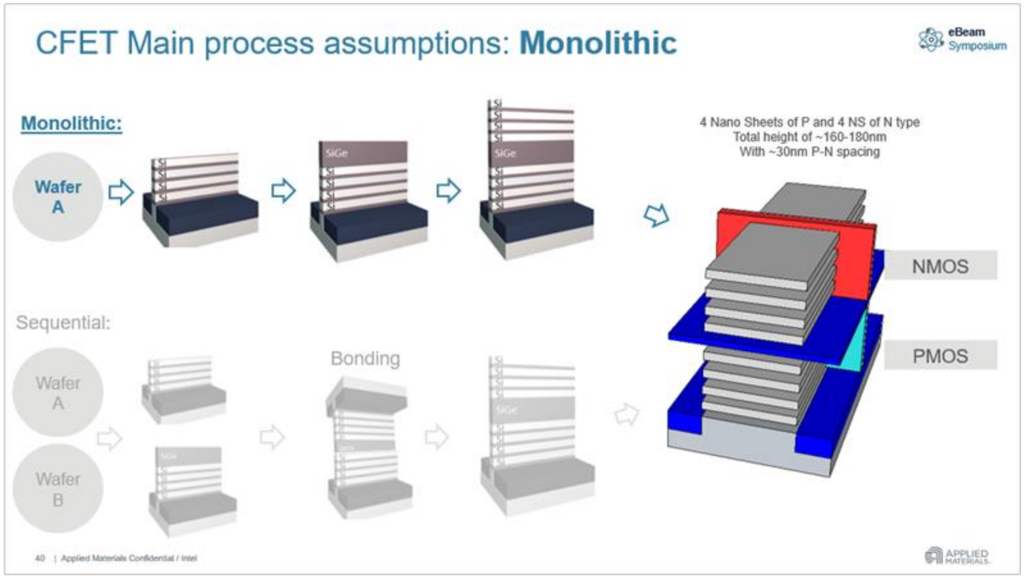
GAA		
Indent		Recess Material: SiGe Recess \ Cavity length: 3-7nm Thk' of Cavity layer: 2-7nm Adjustent material & Thk': Si, 2-7nm # of recess layers: 3-5
NS Release		Recess Material: SiGe Recess \ Cavity length: 4-12nm Thk' of Cavity layer: 2-7nm Adjustent material & Thk': Si, 2-7nm # of recess layers: 3-5

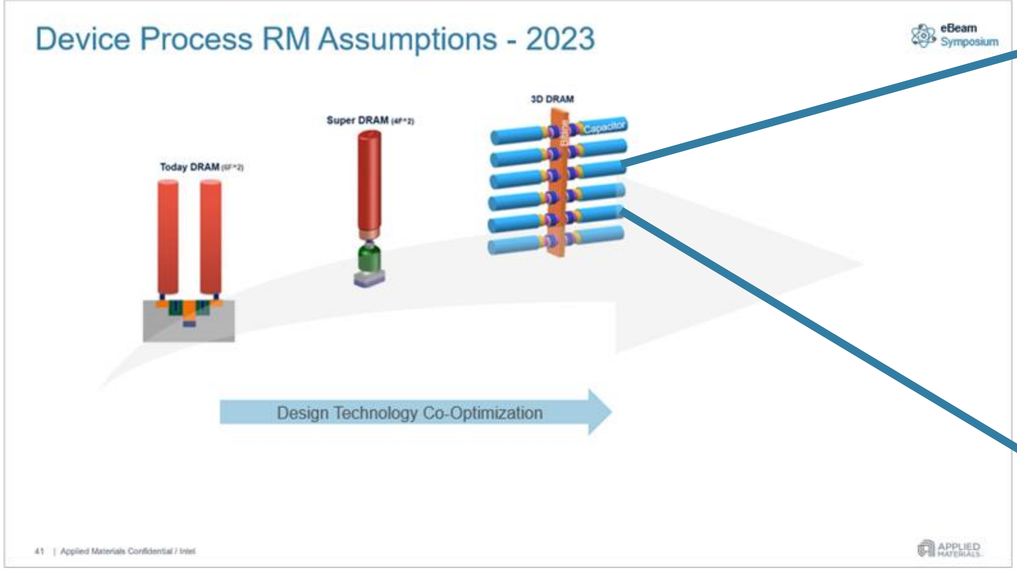
Data is illustrative

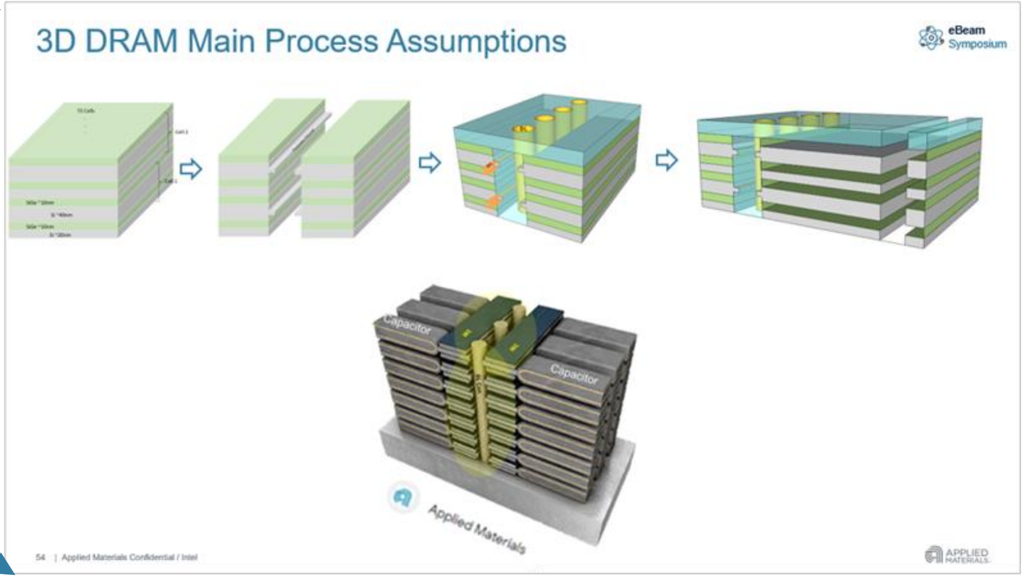
APPLIED MATERIALS

Device Roadmap Assumptions - Examples







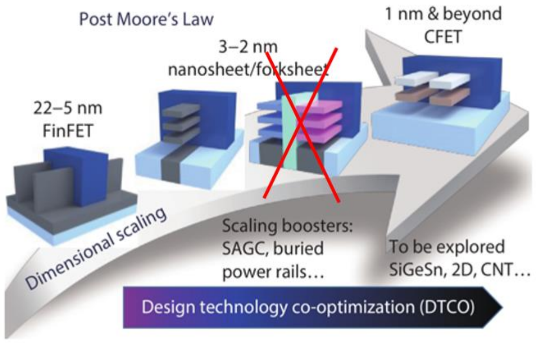


APPLIED MATERIALS

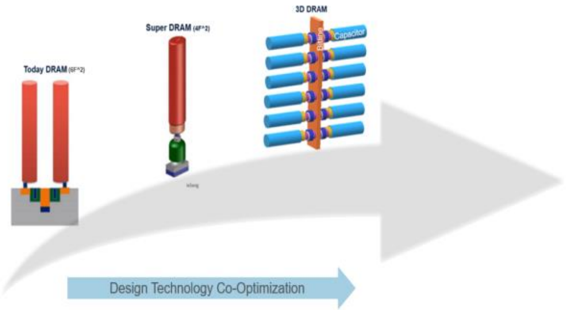
New Challenges Assumptions – 3D Architectures

New Architectures:

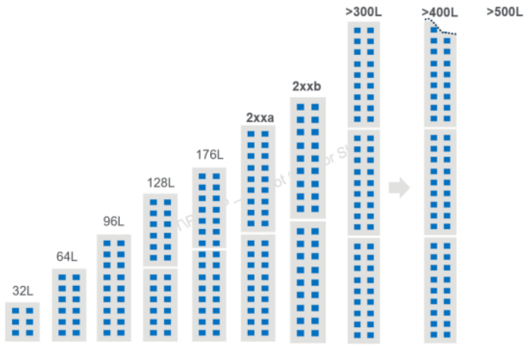
Logic



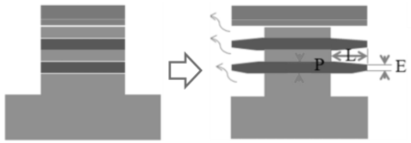
DRAM



3D NAND

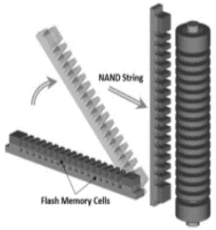


New Architectures leading to new process challenges:



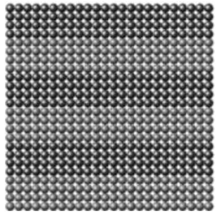
Lateral Etch / Recess

No direct line of sight



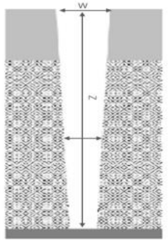
3D structure

Profile and height segmentation for issues



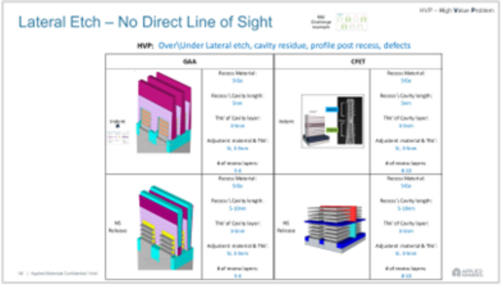
Super lattice

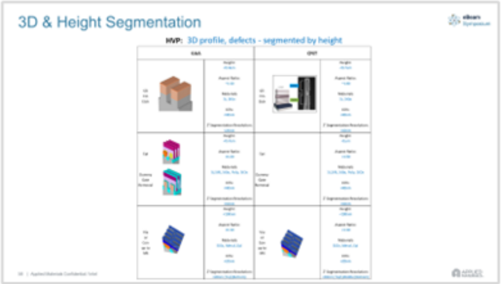
Atomic structure and material characterization

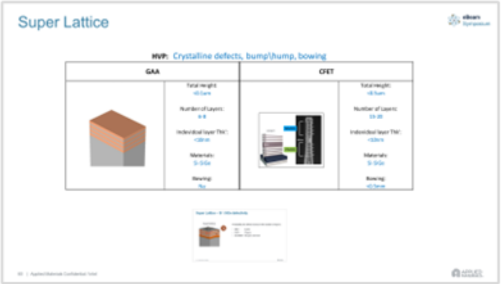


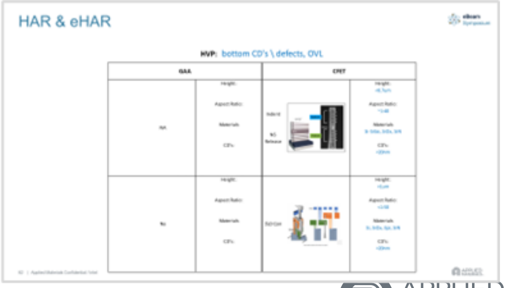
High Aspect Ratio structures

Signal extraction from deeper patterns









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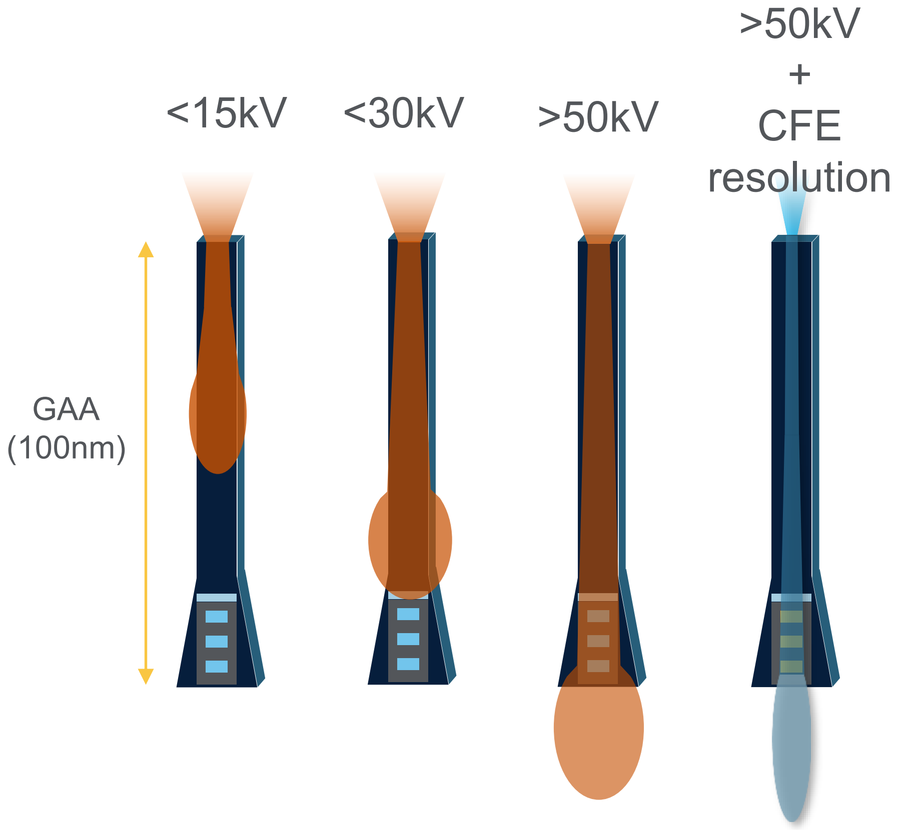
See-through Technology Required to Controls 3D Architectures

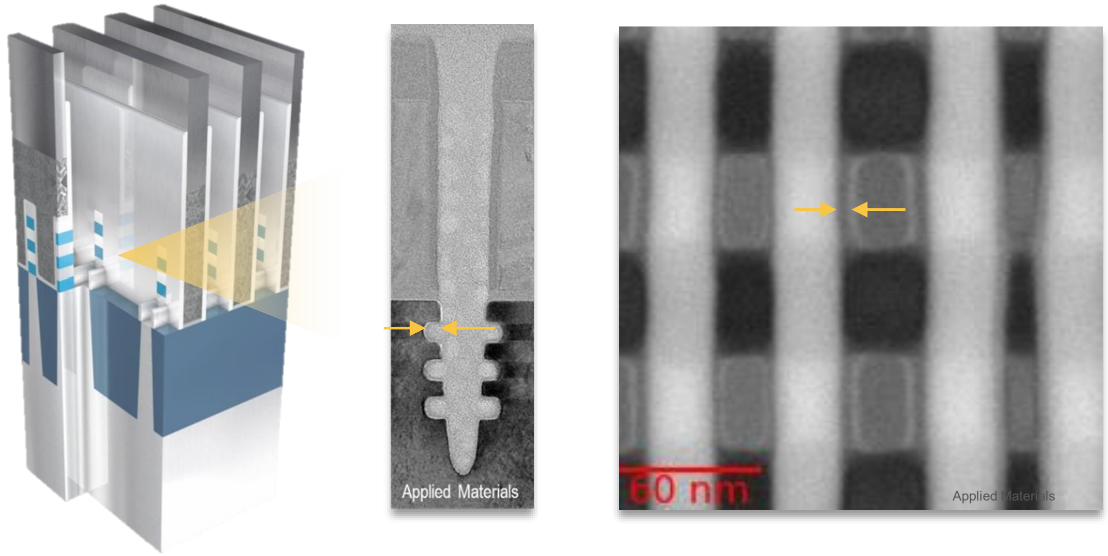
See-Through Imaging



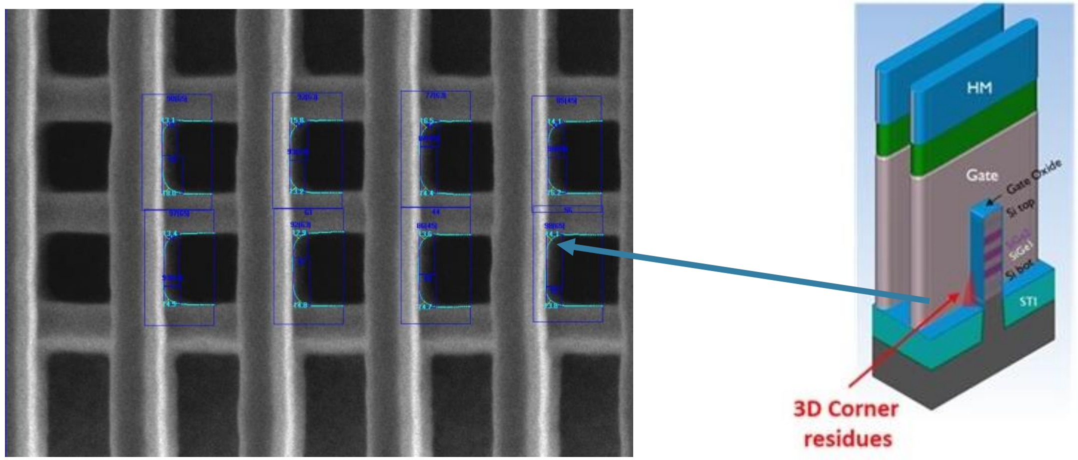
High-resolution imaging through device

GAA: gate-all-around; SiGe: silicon germanium, CFE: cold field emission

SiGe Recess



eTilt for Poly Skirt



Source: imec mCFET

Source: imec mCFET

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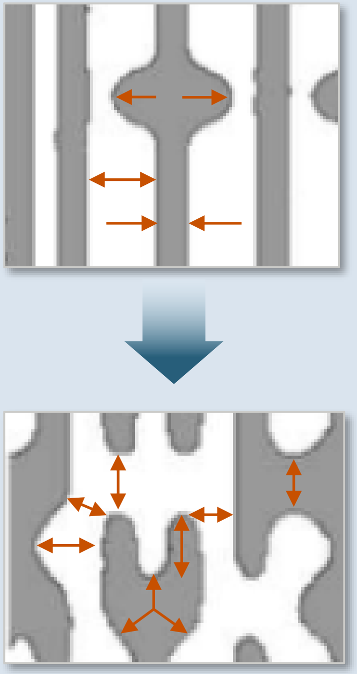
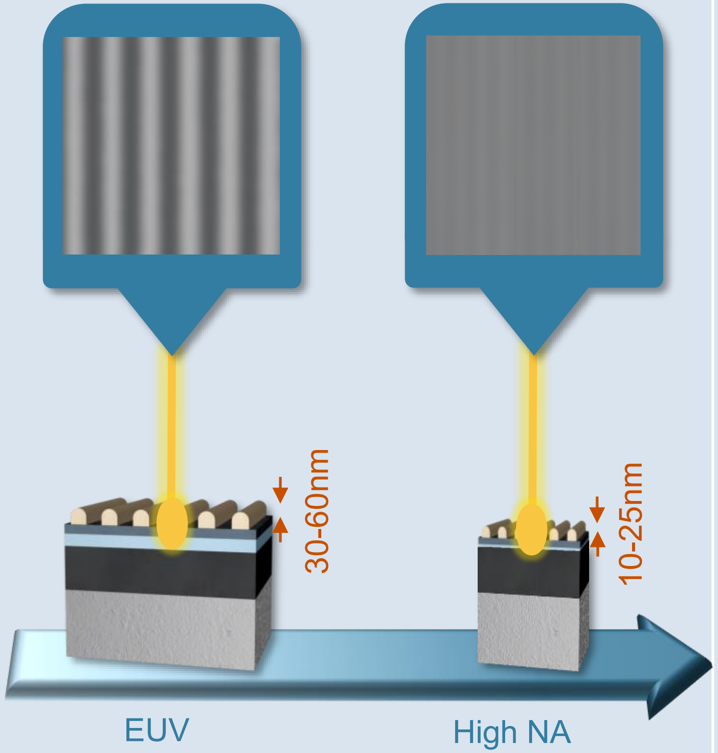
Angstrom Era Lateral Shrink Challenges Continues

Pattern Complexity



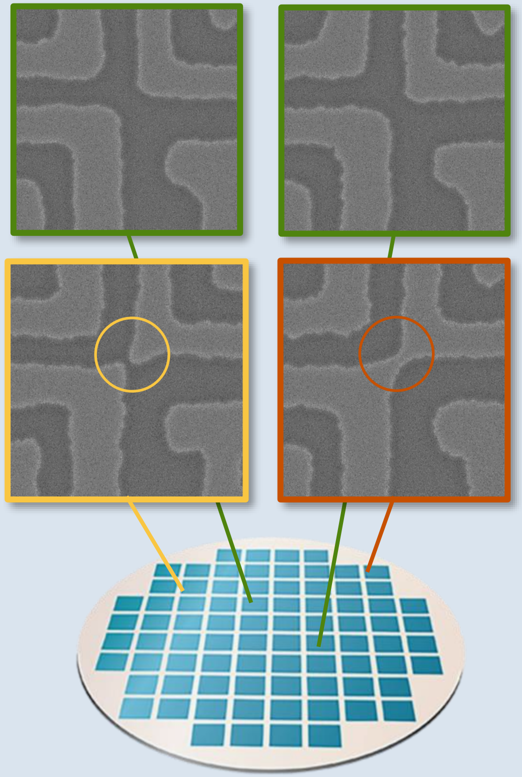
Exponential increase in number of measurements needed for complex shapes

Resist Sensitivity



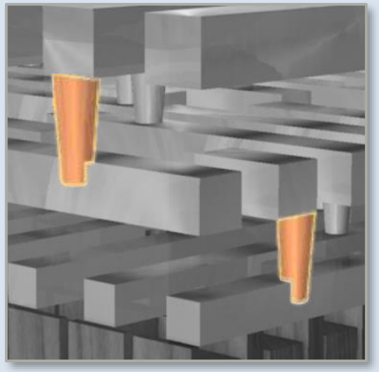
Difficulty resolving patterns without damaging delicate photoresist

Stochastic Patterning Failures

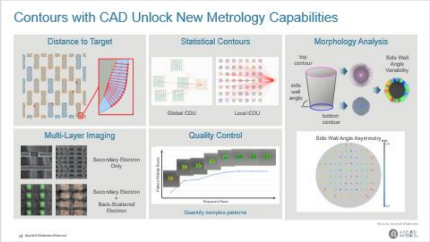


Stochastics increase the chances of patterning failure at hot spots

Edge Placement Errors



EPE limits angstrom era scaling

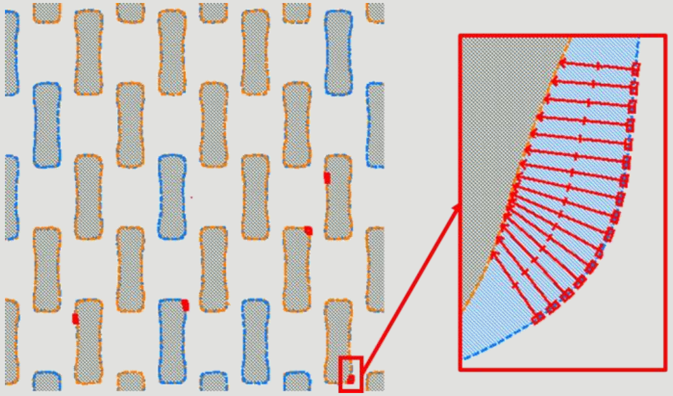


*EPE: edge placement error
Source: Applied Materials

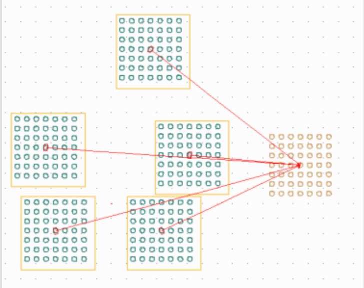
APPLIED MATERIALS

Contours with CAD Unlock New Metrology Capabilities

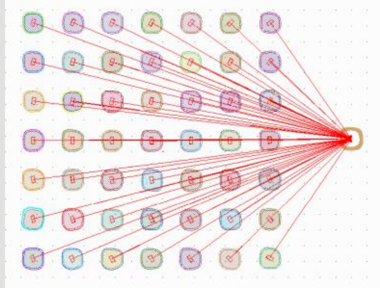
Distance to Target



Statistical Contours

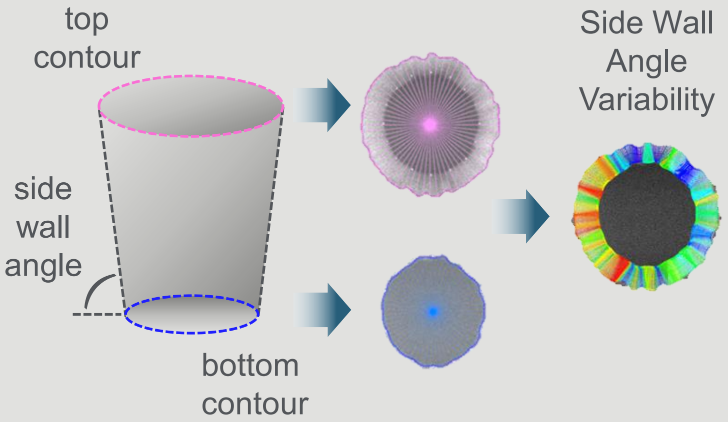


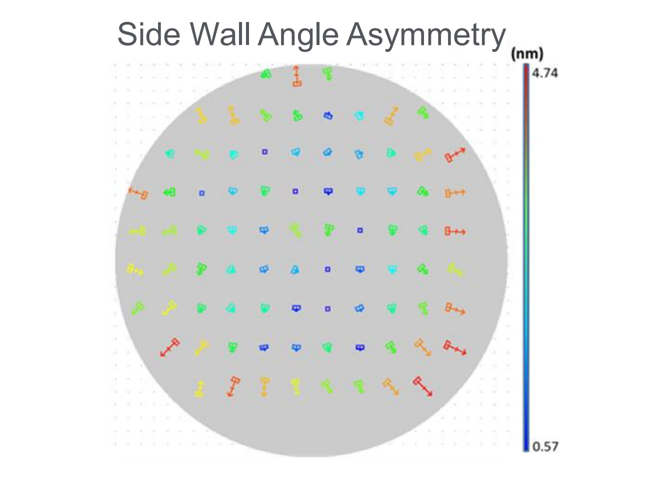
Global CDU



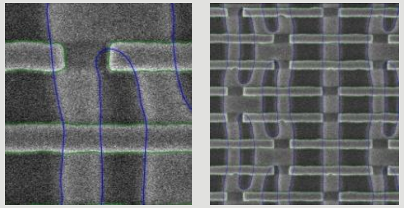
Local CDU

Morphology Analysis

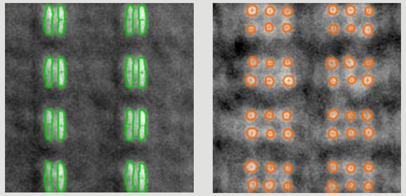




Multi-Layer Imaging

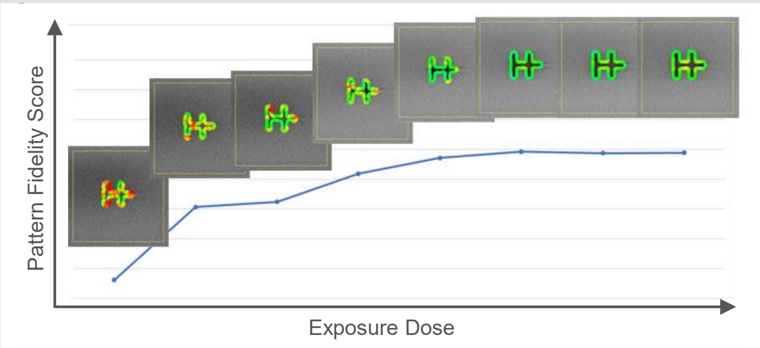


Secondary Electron Only



Secondary Electron + Back-Scattered Electron

Quality Control

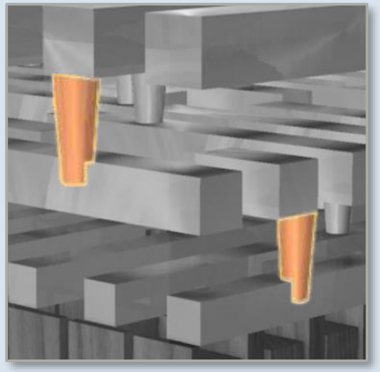


Quantify complex patterns

Source: Applied Materials

Stochastic Errors Become Largest Contributor to EPE

Edge Placement Errors

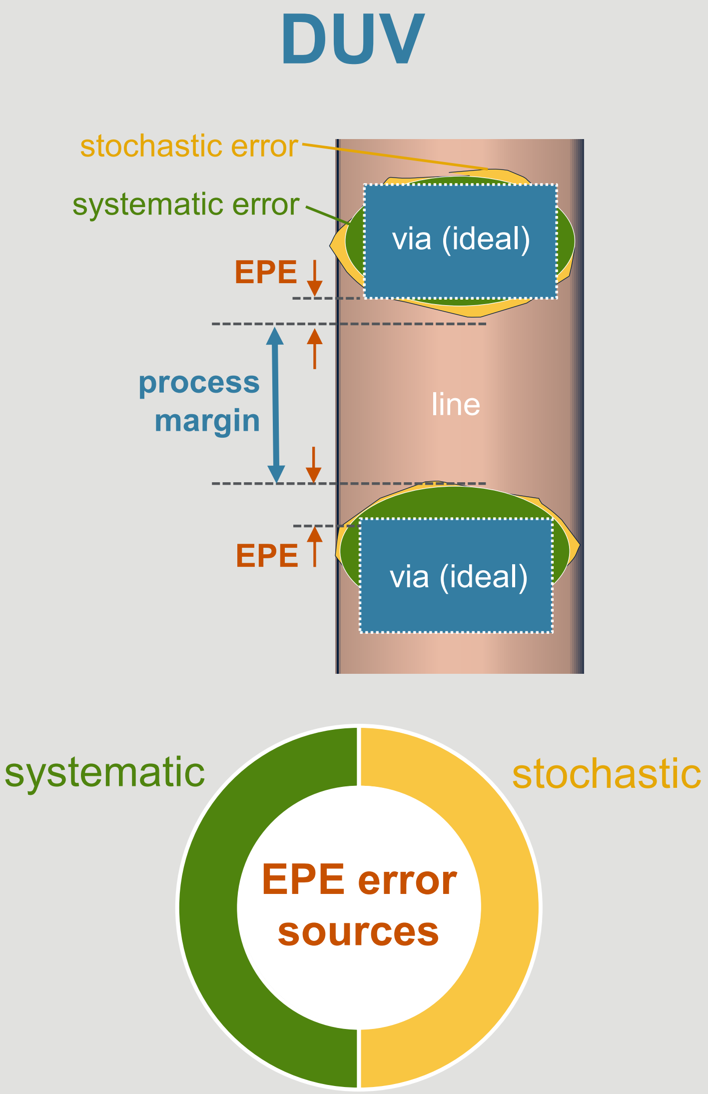


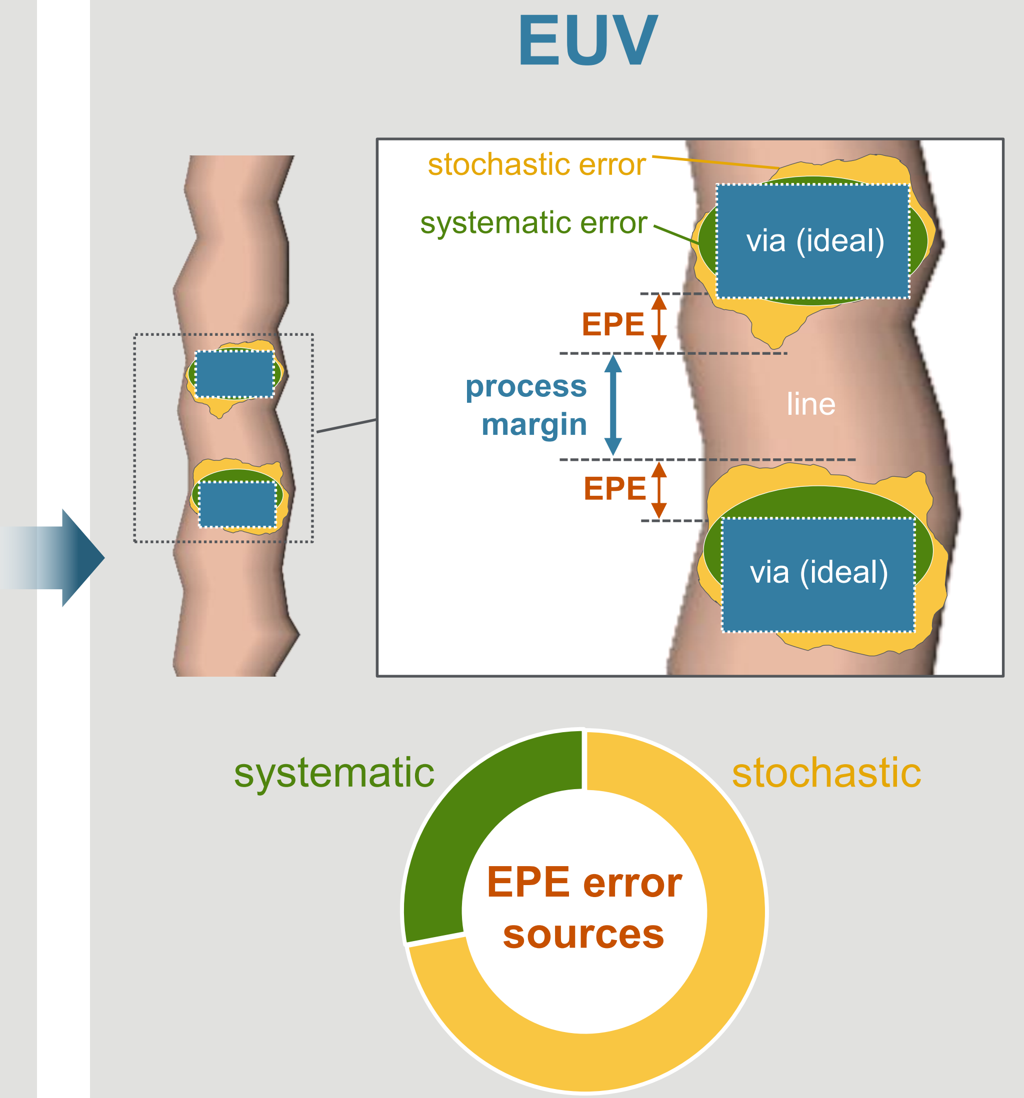
EPE limits angstrom era scaling

Source: Applied Materials

systematic errors: process errors that appear uniformly across an entire die, like CD and overlay

stochastic errors: process errors that appear randomly across an entire die, like LER, LWR and LCDU





Evolution of EPE Control Methods

Optical Overlay

proxy target ~10-30µm

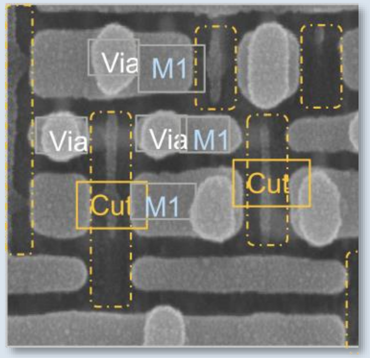
Location: scribe line

Pattern: large pitch

Component: OVL

Stochastics: N/A

eBeam Overlay



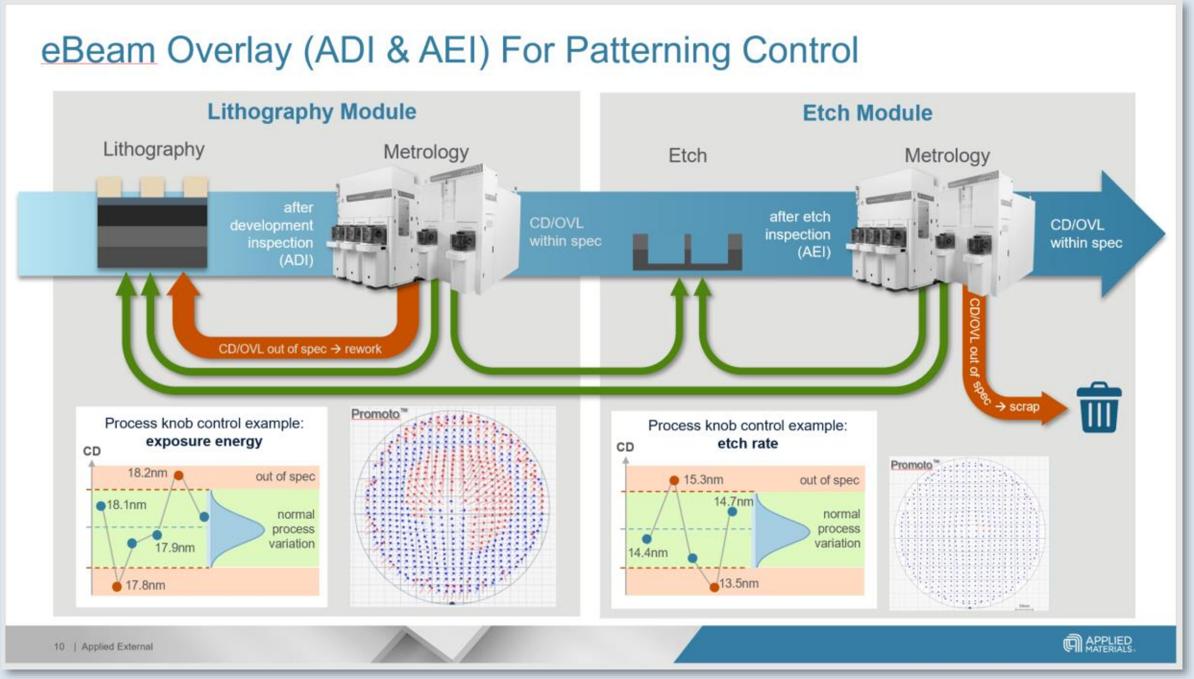
small features <40nm

Location: in die

Pattern: device

Component: OVL

Stochastics: N/A



eBeam Overlay improves systematic errors, but does not address stochastic errors…

Source: Applied Materials

Evolution of EPE Control Methods

Optical Overlay

proxy target ~10-30µm

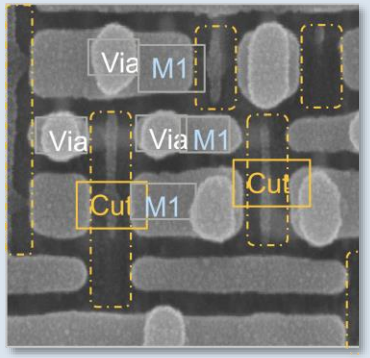
Location: scribe line

Pattern: large pitch

Component: OVL

Stochastics: N/A

eBeam Overlay



small features <40nm

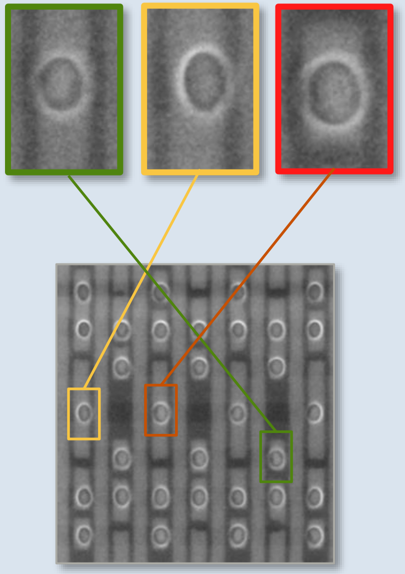
Location: in die

Pattern: device

Component: OVL

Stochastics: N/A

EPE metrology



Location: in die

Pattern: device

Component: OVL, CD, systematic EPE

Stochastics: partial

SPIE Paper Presentation
February 27 @ 4:30pm


We Do Technology | SK hynix

APPLIED MATERIALS make possible

Real time EPE Measurement as a Yield Correlated Metrology on Advanced DRAM Nodes

Taekwon Jee[a], Joonsang You[a], Hong-Goo Lee[a], Seungmo Hong[a], Jonghoi Cho[a], Taeseop Lee[a], Jong-hyun Seo[a]
Michael Shifrin[b], Amir Rosen[b], Rohit Kumar Singh[b], Jeong-Ho Yeo[b]
Younghoon Kim[c], Jun Park[c], Byung-Jo Lim[c], Chan-Hee Kwak[c]
(a) SK hynix, Icheon, Korea
(b) PDC business group, Applied Materials, Rehovot, Israel
(c) PDC business group, Applied Materials, Icheon, Korea

Presenter : Younghoon Kim Ph. D
Applied Materials Korea

Source: Applied Materials

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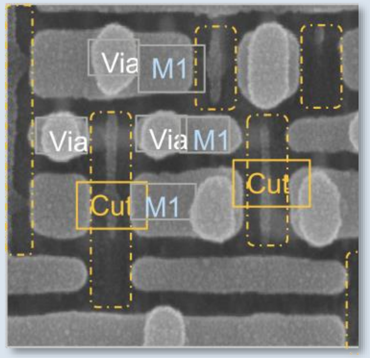
Evolution of EPE Control Methods

eBeam Overlay



small features <40nm

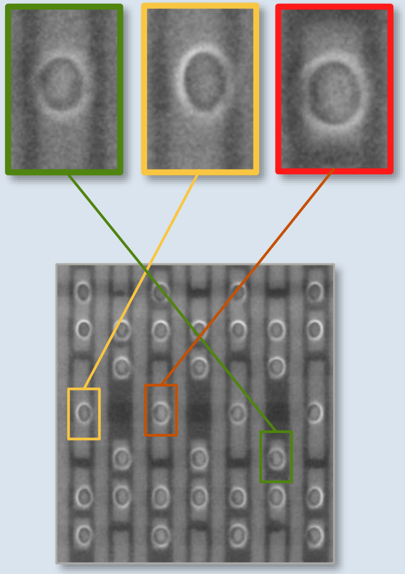
Location: in die

Pattern: device

Component: OVL

Stochastics: N/A

EPE metrology



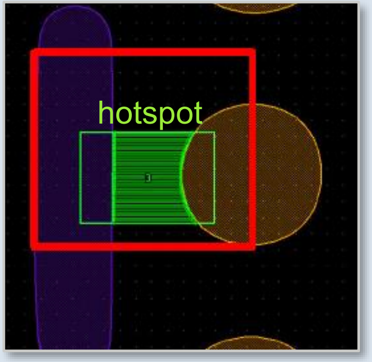
Location: in die

Pattern: device

Component: OVL, CD, systematic EPE

Stochastics: partial

Contour-Based EPE



Location: in die @ hotspot

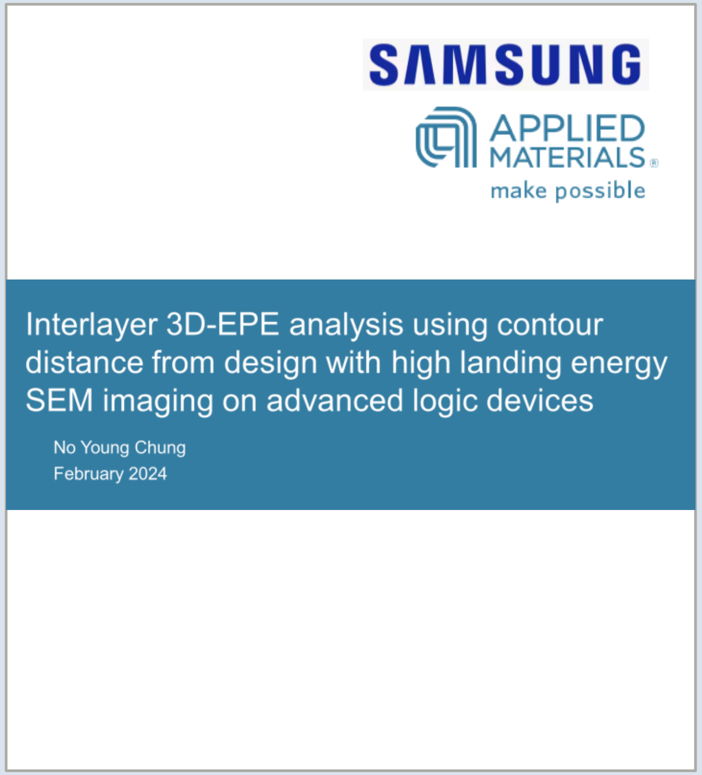
Pattern: device

Measure: OVL, CD, systematic EPE, stochastic EPE

Stochastics: included

SPIE Paper Presentation

February 27 @ 3:50pm


SAMSUNG

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make possible

Interlayer 3D-EPE analysis using contour distance from design with high landing energy SEM imaging on advanced logic devices

No Young Chung

February 2024

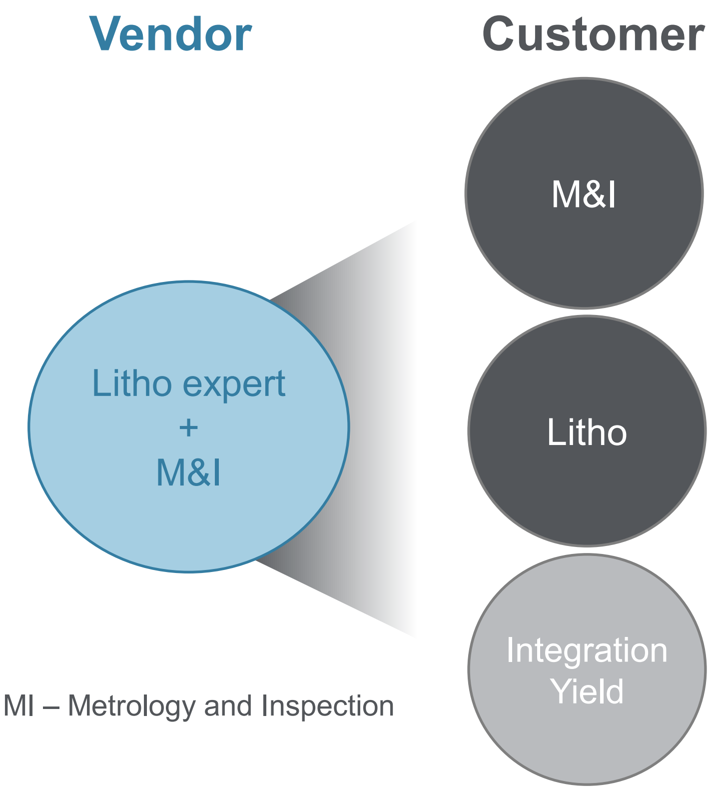
Source: Applied Materials

APPLIED MATERIALS

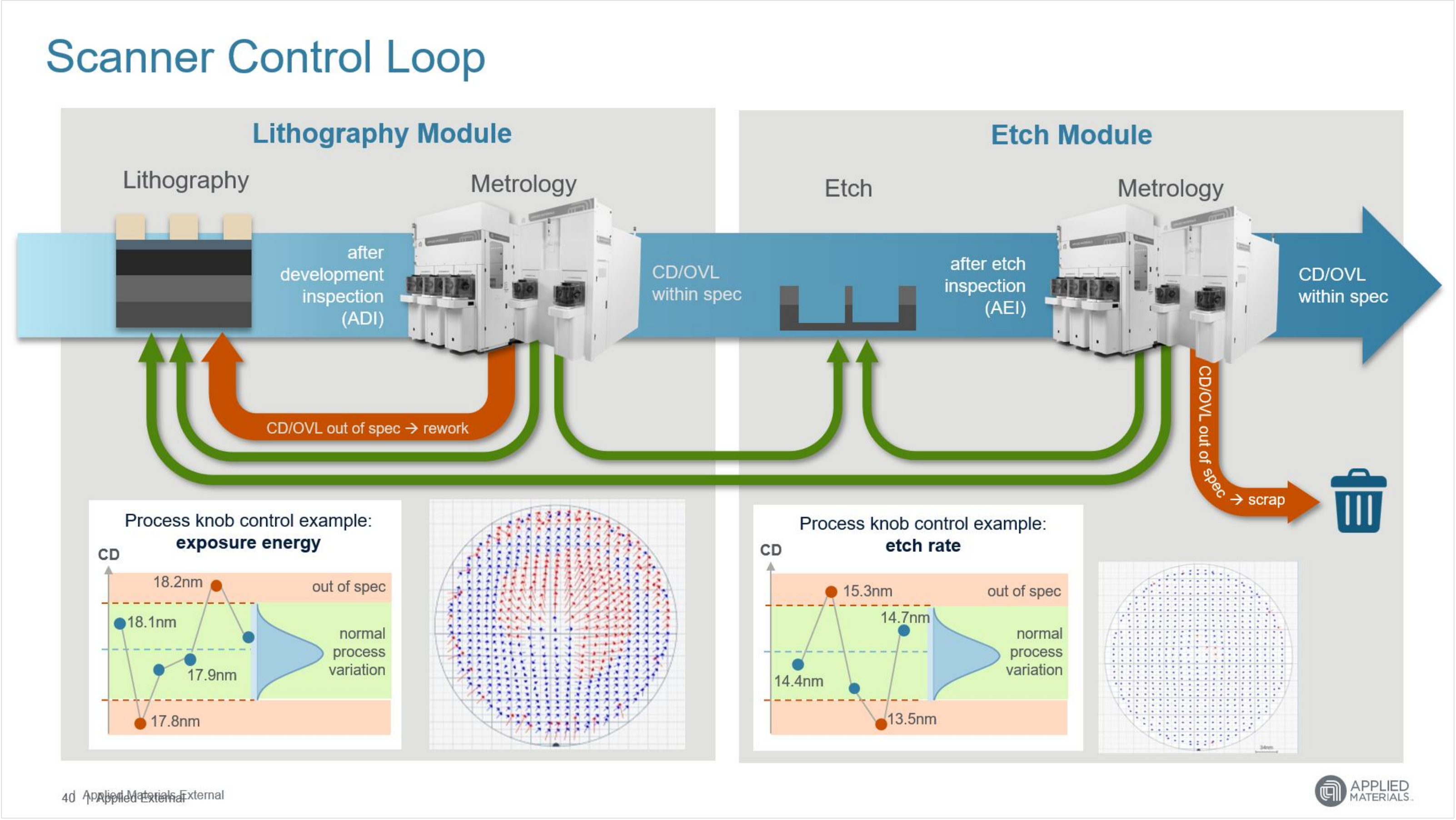
AGENDA

- Introduction
- eBeam Playbook
- Accelerated Workflow
- Summary

Use case: Litho. Overlay Control workflow

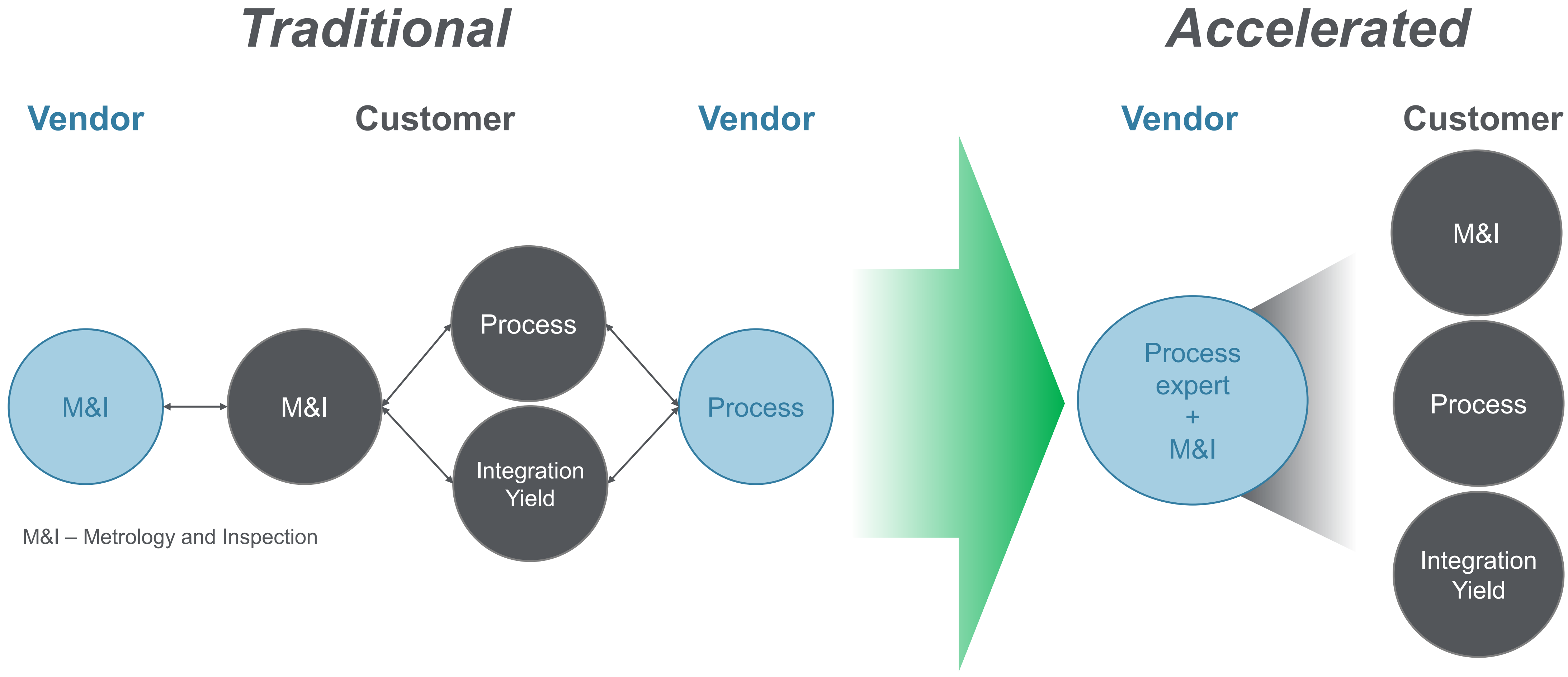


MI – Metrology and Inspection



APPLIED MATERIALS

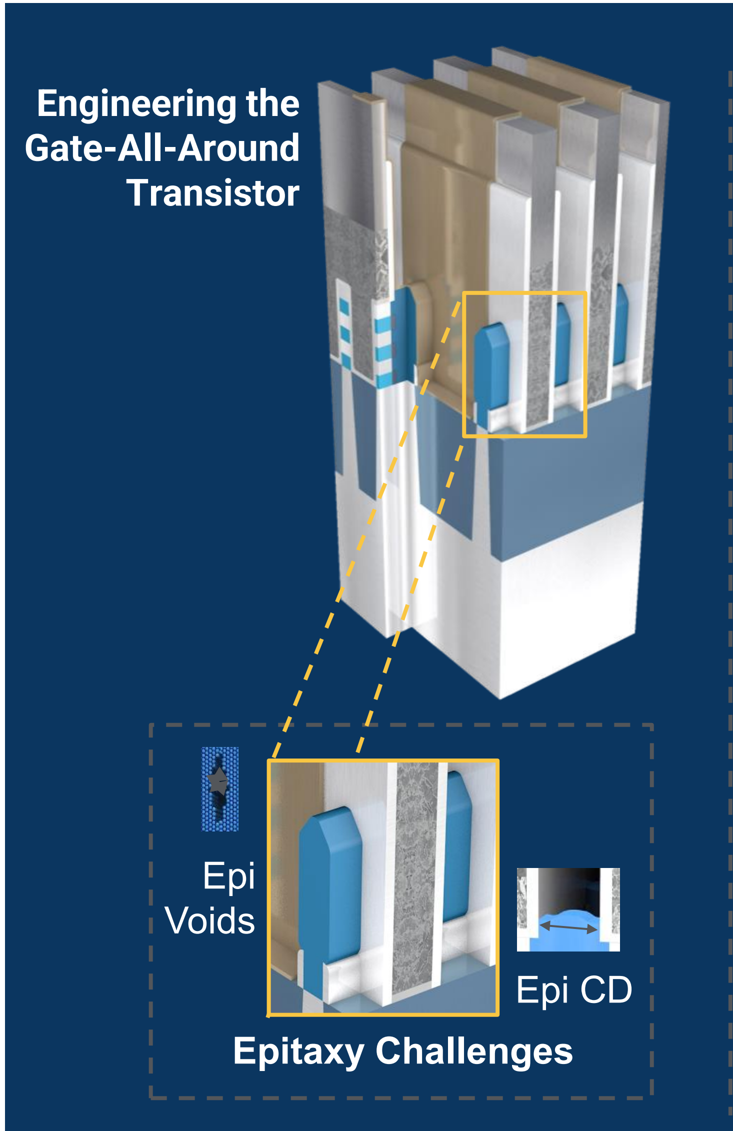
Accelerated Workflow Extended

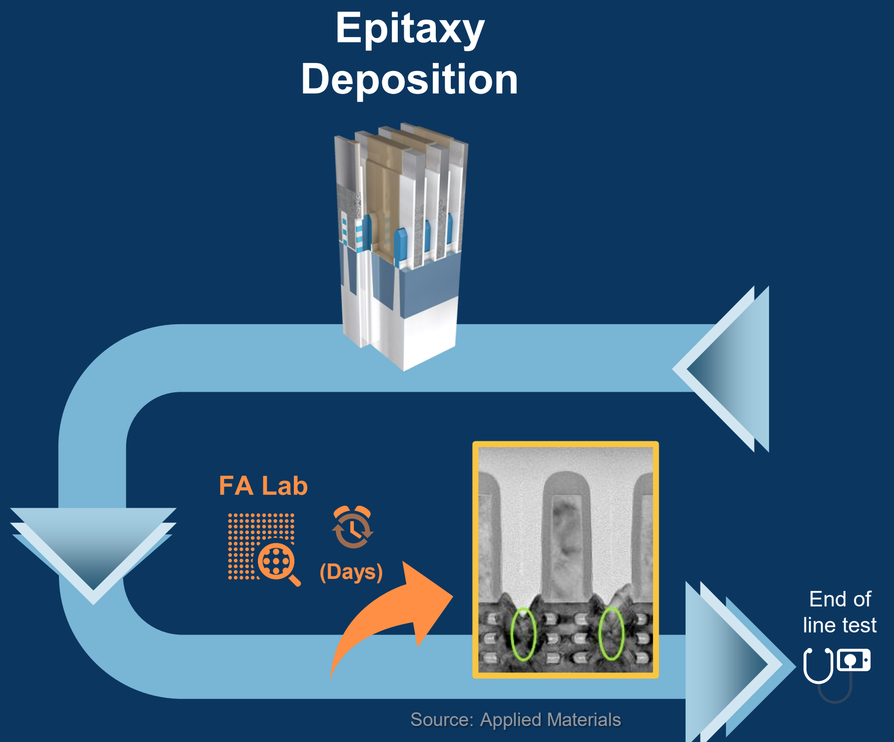


M&I – Metrology and Inspection

- ❑ Tailoring **customer specific** solutions
- ❑ Demonstrated **3x faster TAT** addressing specific yield detractors

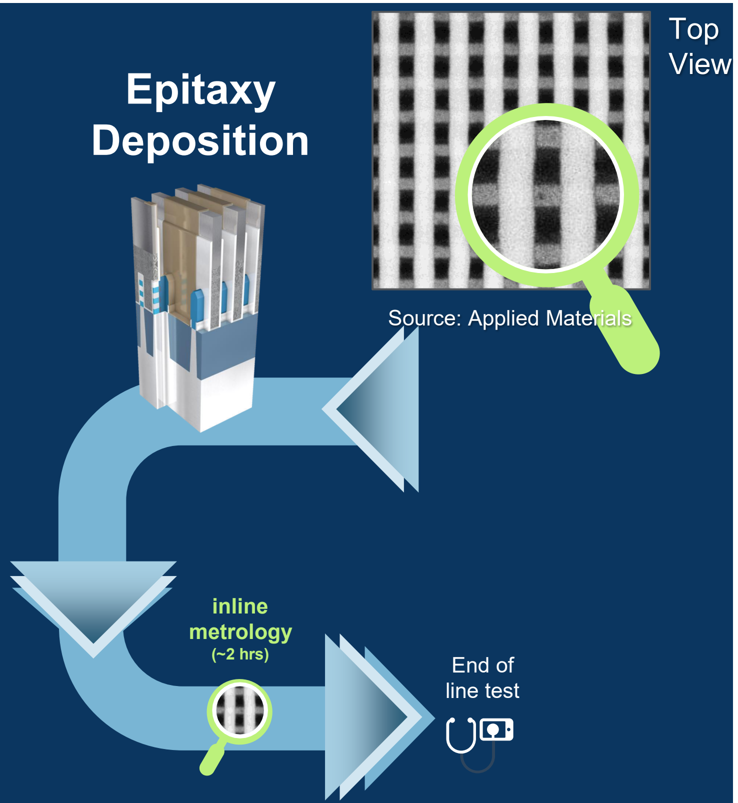
EPI R&D Acceleration – Driven by Accelerated Workflow



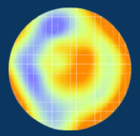


Traditional Flow

- Failure Analysis lab is costly and lengthy
- Limited metrology/measurement options
- End-of-line test lacks the ability to differentiate root cause per step



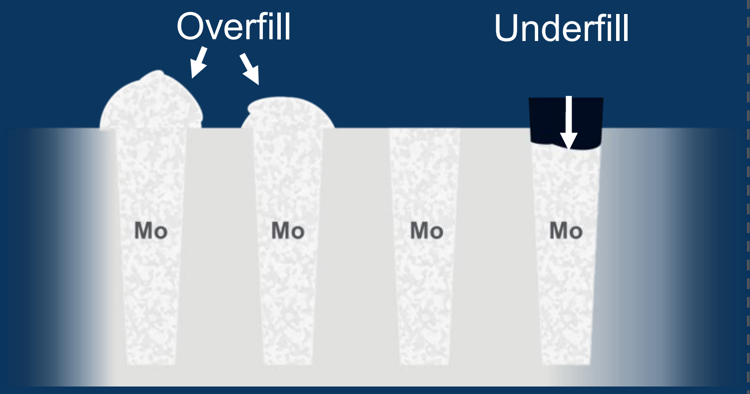
High KeV eBeam Fast Flow



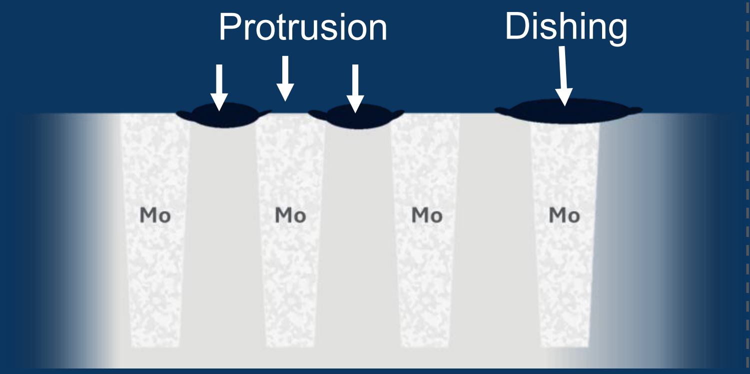
- Fast and Inline (better time to recipe)
- eBeam, on device
- Actionable process control

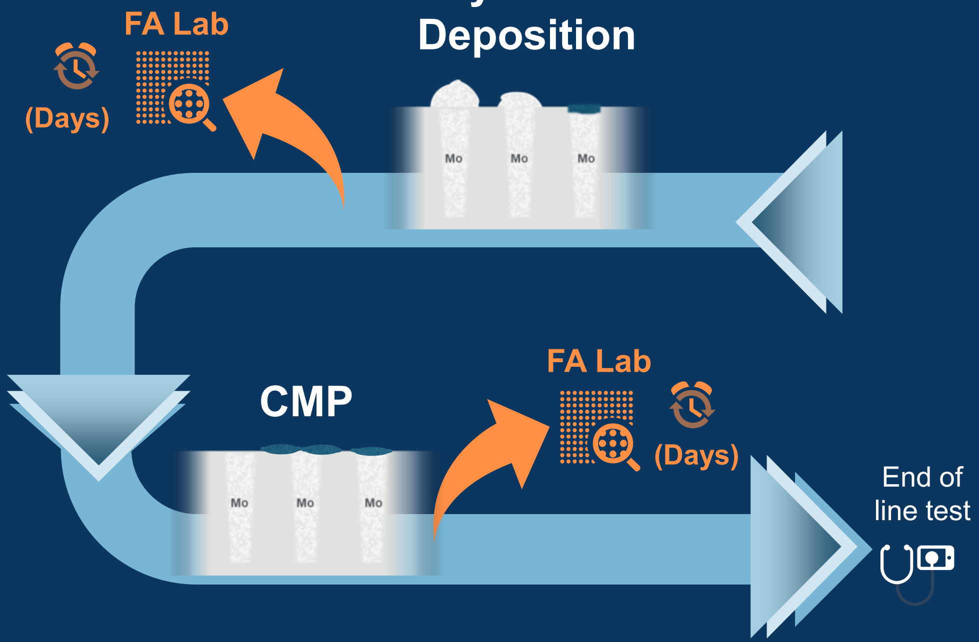
Metal-Dep and CMP R&D Acceleration – Driven by Accelerated Workflow

Deposition Challenges



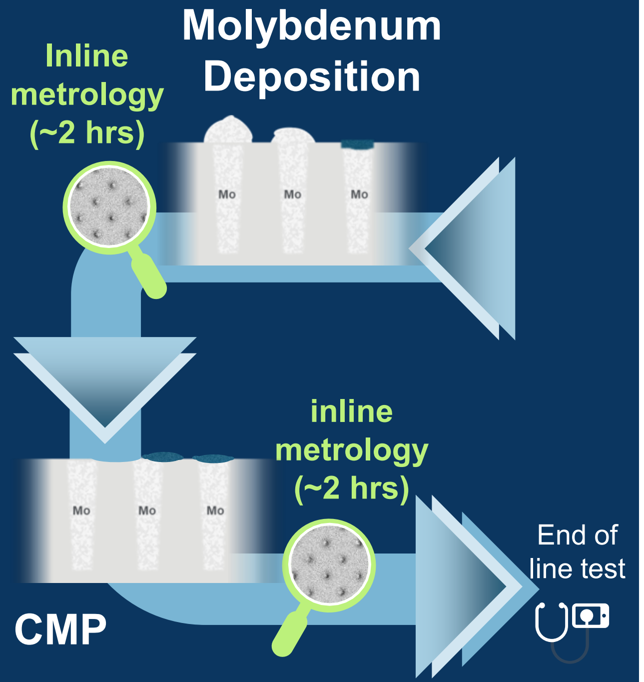
CMP Challenges





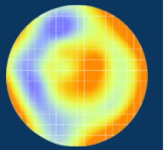
Traditional Flow

- Failure Analysis lab is costly and lengthy
- End-of-line test lacks the ability to differentiate root cause per step



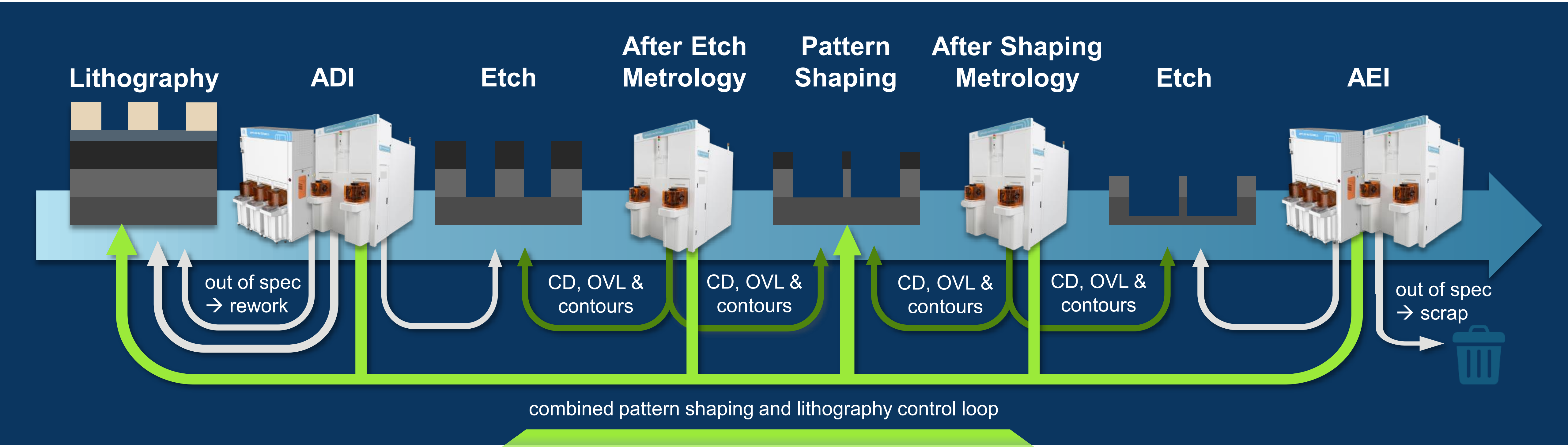
High Current eBeam Fast Flow

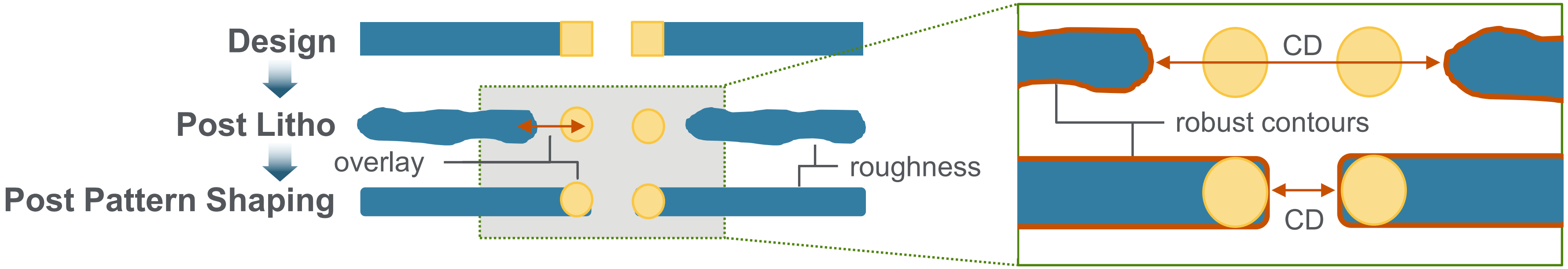
- Fast and Inline (better time to recipe)
- eBeam, on device
- Actionable process control



APPLIED MATERIALS

Pattern Shaping Acceleration – Driven by Accelerated Workflow





New control loops for CD, overlay, line-end shape and roughness

AGENDA

Introduction

eBeam Playbook

Accelerated Workflow

Summary

Summary

- Process is becoming more complex
  Single process step metrology loses correlation to yield/performance

- Time to yield is requiring Yield correlated localized information and accelerated TAT
  We have shown how eBeam is the right technology for localized yield relevant information

- We have proposed compact workflow aiming at accelerating tile to yield
  Demonstrated **3x faster TAT addressing** specific yield detractors

APPLIED MATERIALS

APPLIED MATERIALS™

Material Innovation