Accelerating Accuracy and Speed of Packaged-Device Nanoscale Characterization and FA Using a Novel LaserFIB Workflow

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Introduction

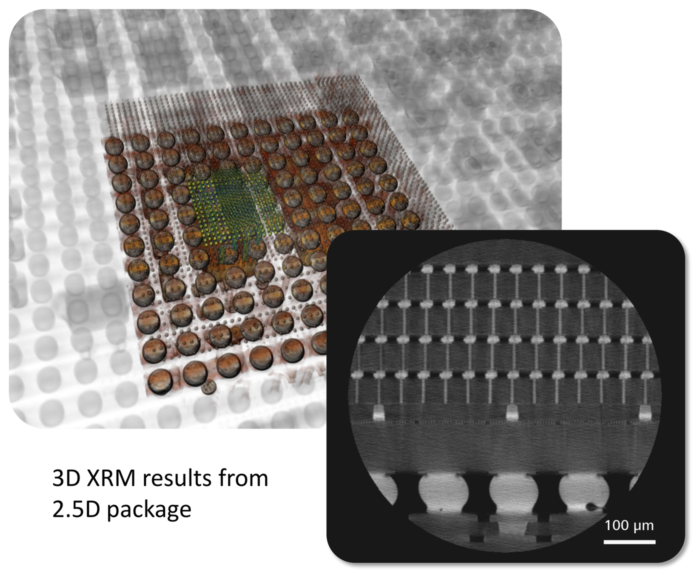
Semiconductor package development and failure analysis require site-specific observation of features with nanoscale resolution. The ability to achieve this is becoming challenged by the emerging and growing trend of heterogeneous integration, an approach which promises to extend device performance in the "More-than-Moore" era by integrating numerous chips or chiplets of diverse functionality directly within the same package. The result is packages with increasing complexity critical to the device performance, often in a larger footprint and including 2.5/3D architectures, higher I/O densities, and shrinking interconnect size and pitch. The package complexity creates added demands on efficient microscopic targeting, navigation, and access to desired regions of interest, which could reside at varied locations including potentially deep within a relatively large 3D volume.

Problem Statement

You have identified a region of interest located somewhere within the deep interior of your package / device. How do you efficiently target, access, and characterize that feature at the micro- to nano-scale?

Existing Techniques in the Toolkit

3D X-ray Microscopy (XRM)



3D XRM results from 2.5D package

- Submicron imaging resolution
- Non-destructive / non-invasive
- Truly 3D volumetric data
- Virtual cross sections at any angle and orientation
- Faster acquisition times powered by deep learning X-ray reconstruction

- *Resolution limited to 0.5 µm*
- *Density-based contrast, no chemical analytics*

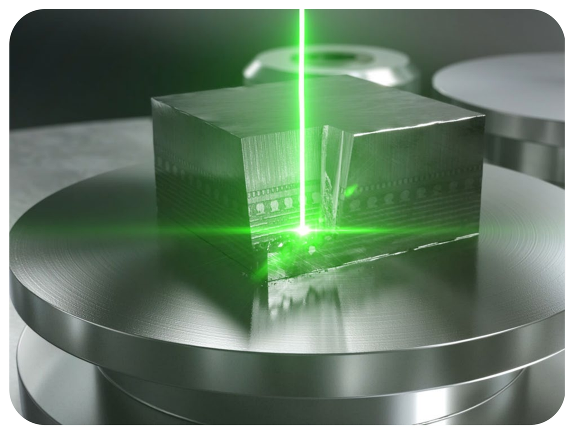
FIB-SEM

Backscattered electron image of IC cross section made by FIB

- Highly precise site-specificity
- Nanometer imaging resolution
- Numerous contrast and analytical modalities
- Simultaneous milling and imaging

- *Focused ion beam access to depths of ~100 µm in practical timeframe*

Femtosecond Laser Ablation



Simulated laser ablation of IC package

- Very rapid, large volume material removal, access mm depths
- Cuts through all typical materials in IC packages
- Ultrashort pulses leave behind little or no residual material damage
- Can be site specific

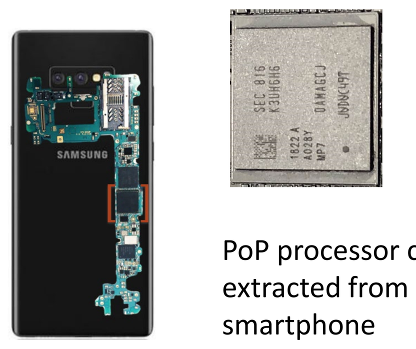
- *Requires high level of targeting/ positioning accuracy to realize efficiency gain*
- *Tuning of laser parameters to optimize milling on new materials*

Approach

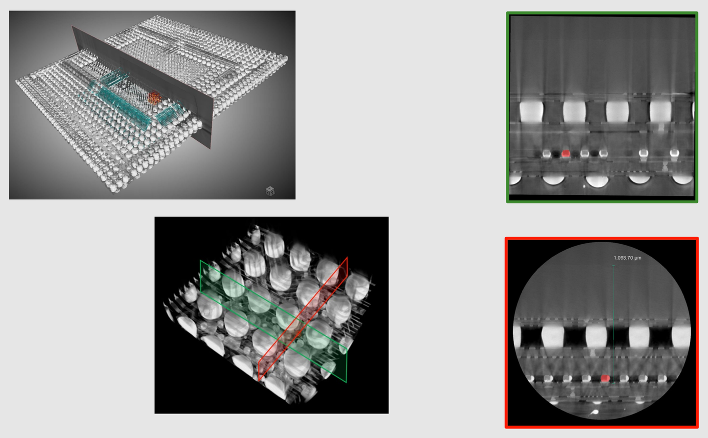
Leverage the respective strengths of each instrument in a correlative imaging workflow consisting of 4 steps:

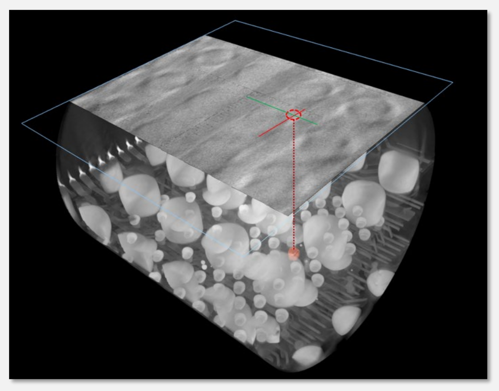
Visualize	Target	Access	Analyze
3D structure by non-destructive submicron XRM	ROI relative to sample surface, correlated in XRM and FIB-SEM views	Perform targeted fs-laser milling to reveal ROI in cross section	FIB polish if required, nm-scale EM imaging & characterization

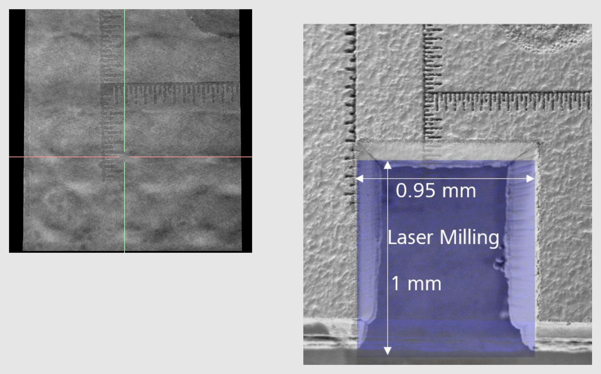
Two Demonstration Cases*



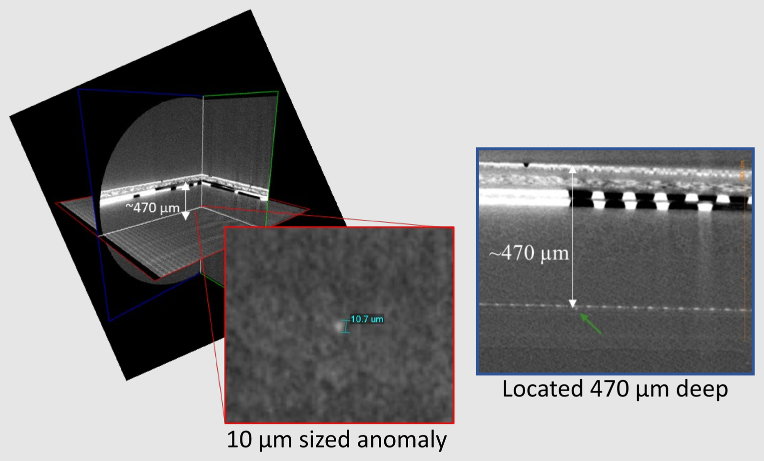
PoP processor chip extracted from broken smartphone

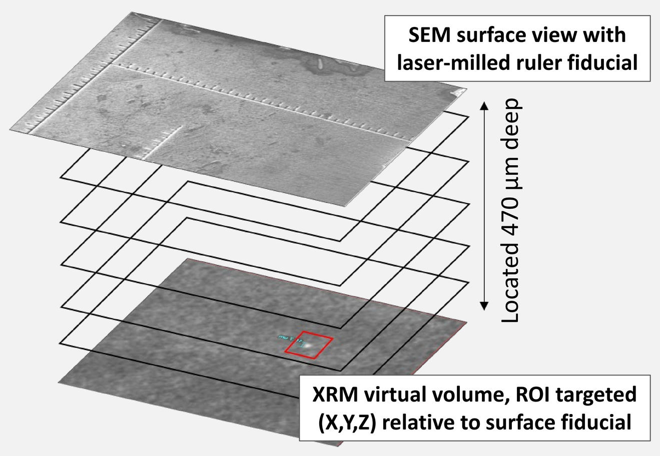


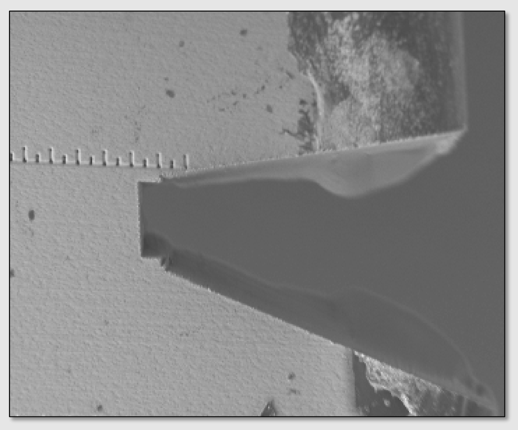


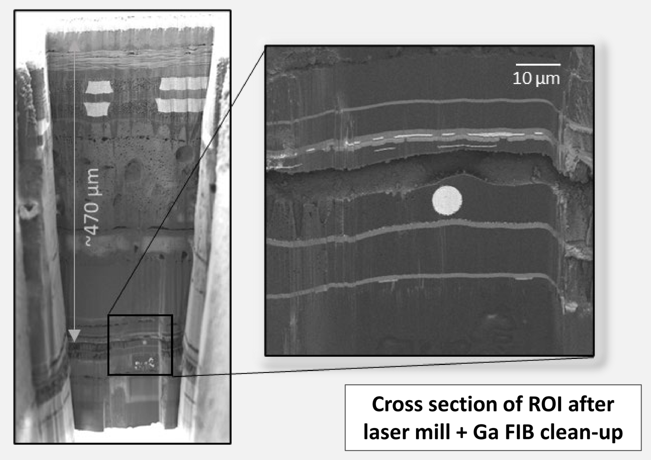


Small piece of AMOLED display from broken smartphone









3D X-ray Microscope → FIB-SEM with fs-laser

*datasets originally presented at 2021 Electronics Packaging Technology Conference, V. Viswanathan et al.

Conclusions & Outlook

- **A correlated workflow using 3D X-ray microscopy and FIB-SEM with integrated fs-laser allows one to efficiently target, access, and characterize regions of interest buried at arbitrary and deep (>1 mm) locations within a larger object**
- **This addresses multiple sample and feature types, with regions of interest down to <10 µm dimensions**
- **The targeting accuracy is a function of the region of interest's depth beneath the sample surface and control of the laser's spot profile and taper.**
- **Now developing parameter optimization procedure and recipe- and material-based milling protocols to quickly tune workflow to new devices → future improvements in automation**

References

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[3] B. Tordoff, et al. *Applied Microscopy*., **50**, 24 (2020)
[4] C. Hartfield, et al., *Chip Scale Review,* **24**, 39-42 (2020)
[5] V. Viswanathan and L. Jiao, *IEEE Electronics Packaging and Technology Conference*, 2021