
IBM Research
Inventing what's next.

In-Line Metrology for Sub-2nm Technology Nodes

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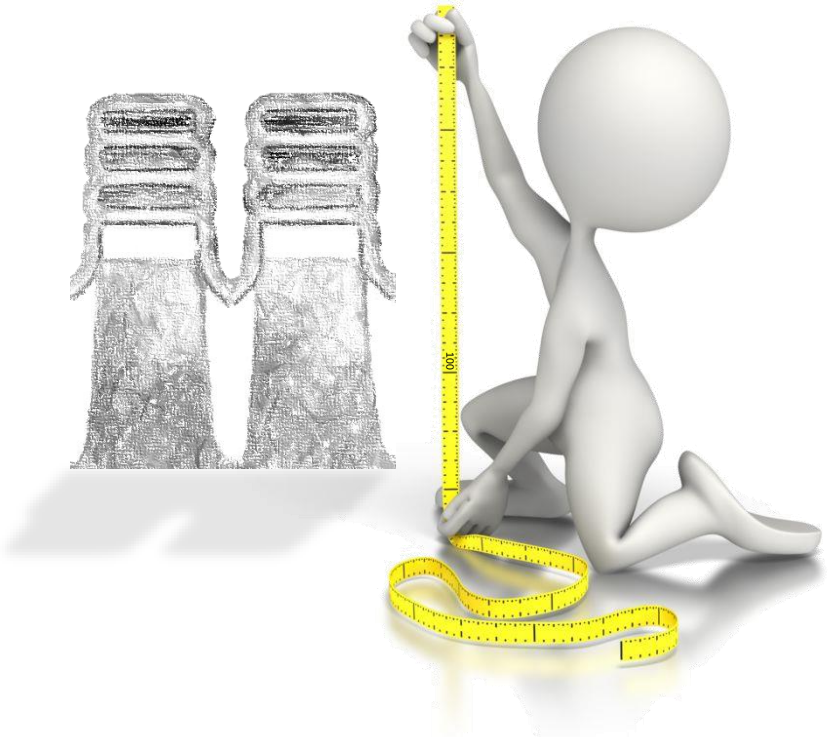
Outline

- IBM Semiconductors
- Industry Roadmap
- In-Line Metrology
  - Recent Innovations
  - High-NA EUV Challenge
  - Next-Gen Techniques
- Takeaways



You can’t control what you can’t measure

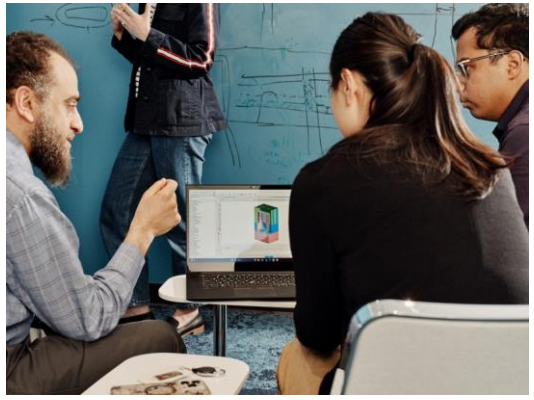
IBM Semiconductors

Logic Technology

Developing the next generation of chips to increase performance and improve energy efficiency.

Chiplet & Adv Packaging

Developing chiplet and packaging architectures built for next generation AI.



Design & Enablement on Cloud

Enabling partners with our expertise across chip design and hybrid cloud.

Intelligent Fab

Using AI and automation to make semiconductor manufacturing faster and smarter.

Albany NanoTech – Leading Edge 300 mm R&D

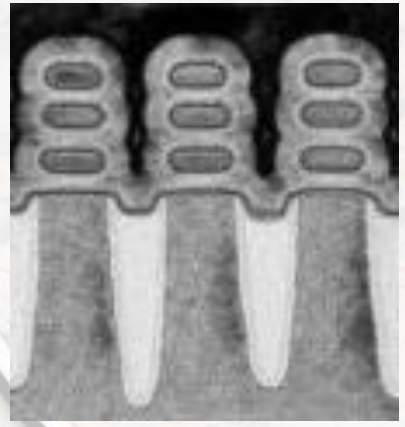
- public-private partnership
- >$15B cumulative investment
- >150,000 sq-ft of cleanrooms
- IBM (largest tenant), TEL, AMAT, LAM, and many others

advanced, full manufacturing capability including EUV lithography (NXE:3400B)

→ High-NA fab coming soon

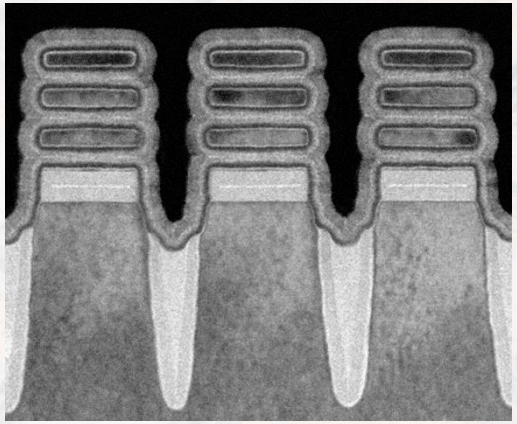
IBM Semiconductors Logic Developments

1st Gen Nanosheet
VLSI 2017



First Gate-all-Around Architecture
L_g = 12 nm
Gate Pitch = 44/48 nm
1.3x W_{eff} over FinFET

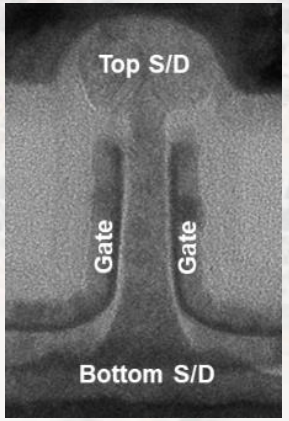
2 nm Node
May 2021



Bottom Dielectric Isolation
EUV Variable Sheet Patterning (15 to 70 nm)
pFET Strain Engineering
Multi-Vt scheme

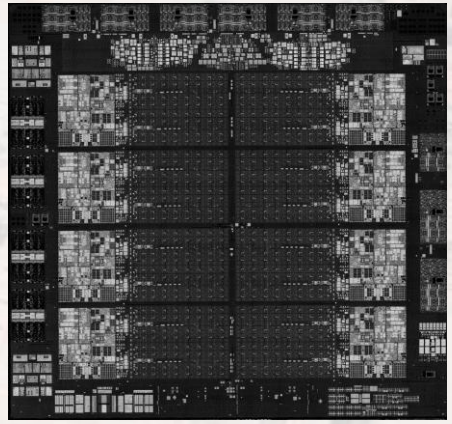
https://research.ibm.com/blog/2-nm-chip

VTFET
IEDM 2021



First Vertical Transport Architecture
Top/Bottom S/D
Zero Diffusion Break

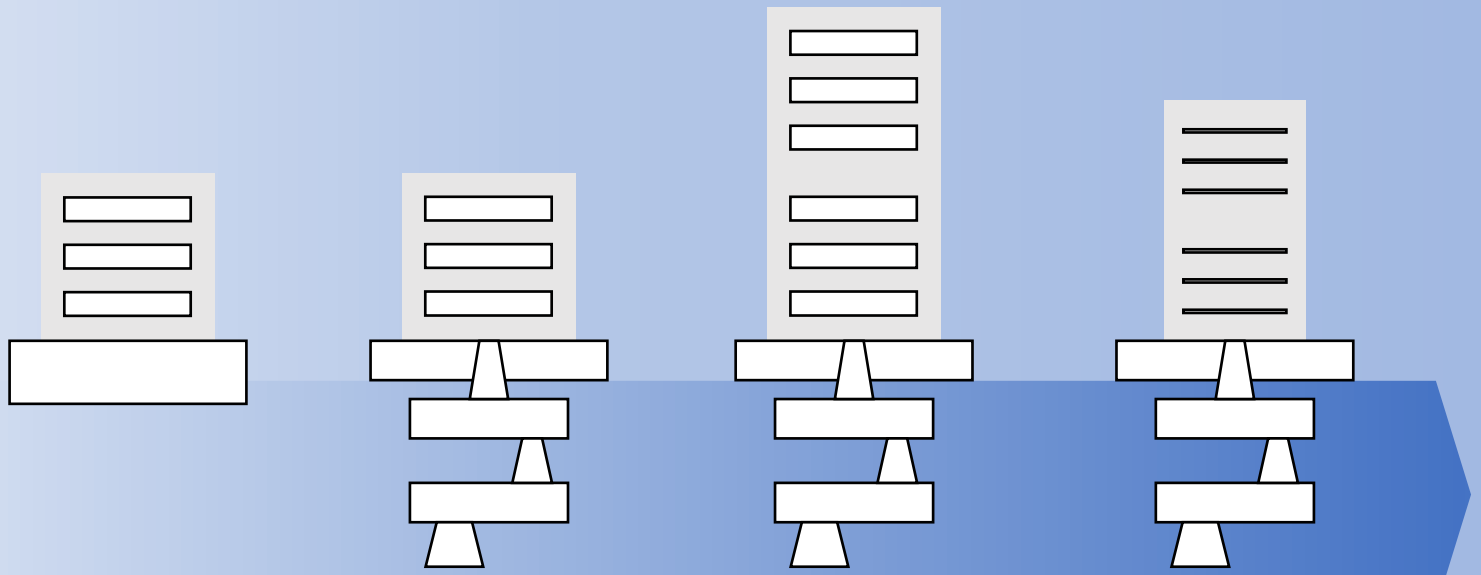
Telum Processor
2022



IBM z16
7 nm EUV Technology
8 Cores (5+ GHz)
AI Accelerator
32 MB L2 per core
22.5 Billion Transistors
530 mm^2 chip size
<3 s downtime/year

https://research.ibm.com/blog/research-powering-ibmz16

Industry Direction: CMOS Scaling, BSPDN, and New Channel Materials



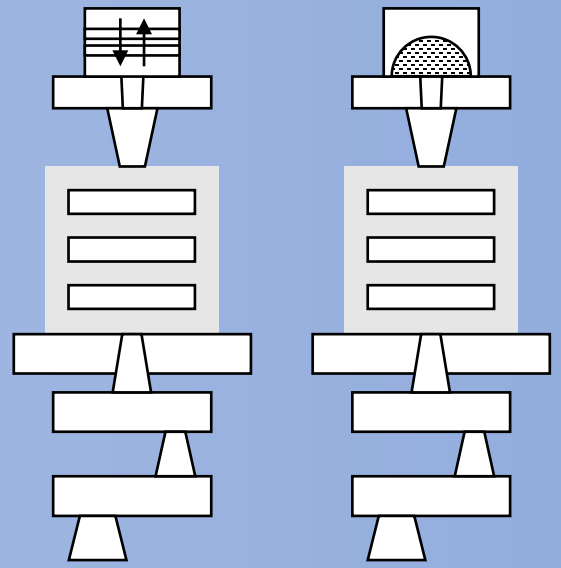
Nanosheet

Nanosheet BSPDN

Stacked FET BSPDN

Stacked FET 2D Channels BSPDN

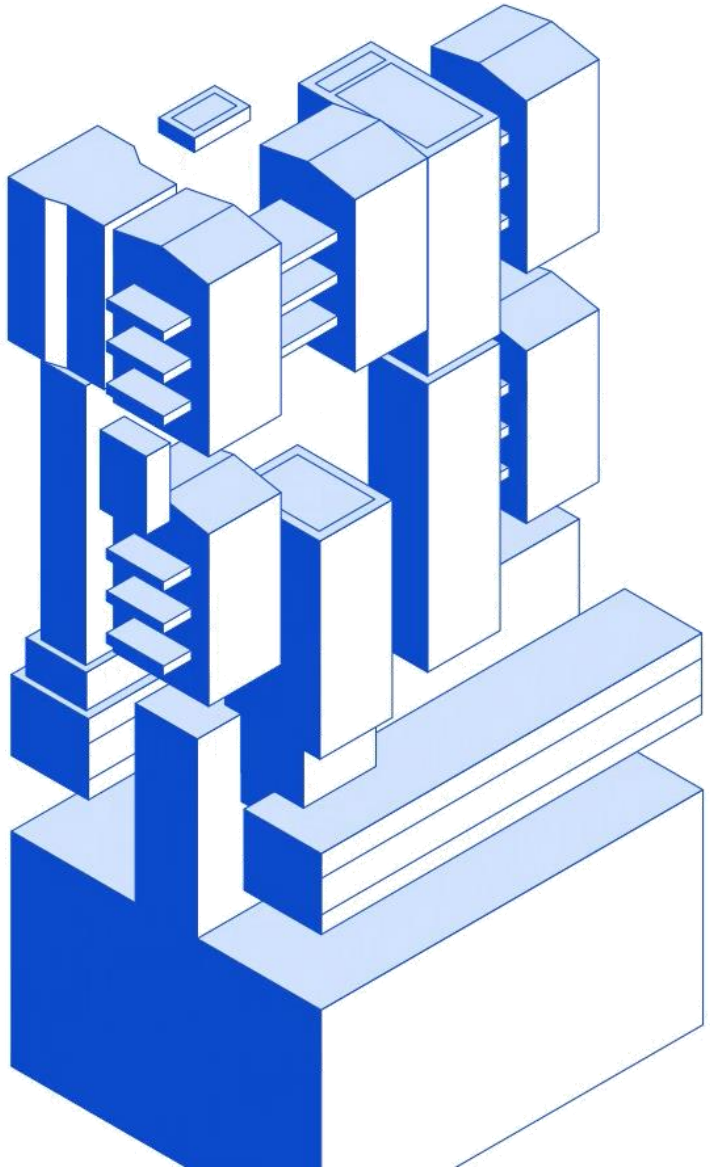
Modular Frontside Functionality



Monolithic MRAM or PCM Integration Examples

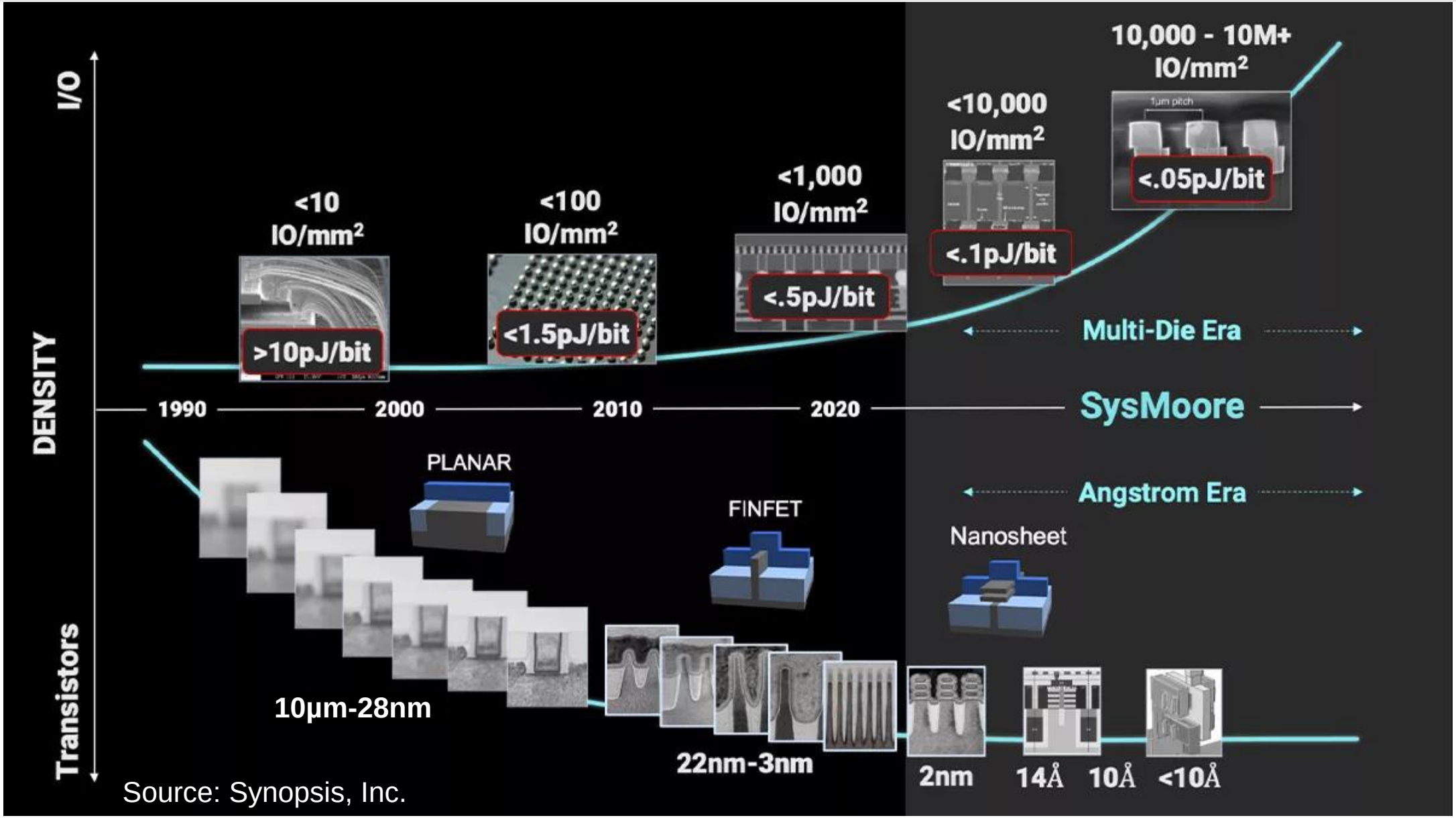
Developments Throughout

- **Pitch Scaling**
  - EUV DP and High-NA Lithography
  - Subtractive Metal Patterning
- **Backside Power**
  - Front- and Backside Processing, Bonding
- **Monolithic Integration**
  - Transistor Stacking (nMOS on pMOS)
  - Frontside Functionality (Memory Elements)
- **Material Innovations**
  - Interconnects, Dipoles, 2D Materials
- **Chiplet Technology**
  - Chip Stacking (die-die, die-wafer)



Metrology Needs

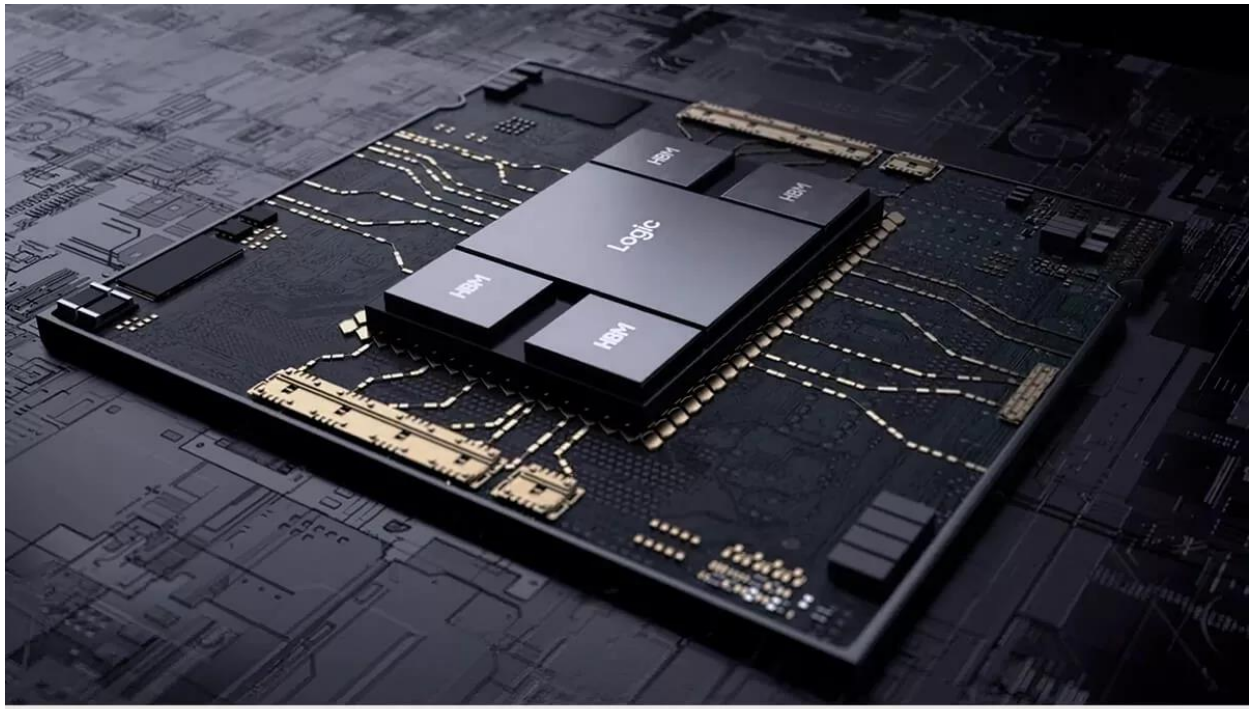
• **Pitch Scaling** – EUV DP and High-NA Lithography – Subtractive Metal Patterning	• **CDSEM, Scatterometry (higher energy)** – small pitches with feature profiles – metal etch (top via)
• **Backside Power** – Front- and Backside Processing, Bonding	• **Wafer Shape, Overlay, Scatterometry** – distorted wafers, complex stacks
• **Monolithic Integration** – Transistor Stacking (nMOS on pMOS) – Frontside Functionality (Memory Elements)	• **Scatterometry, Raman, XPS** – complex stacks, small volumes – complex stacks, materials
• **Material Innovations** – Interconnects, Dipoles, 2D Materials	• **Raman, XPS, new in-line techniques** – materials characterization
• **Chiplet Technology** – Chip Stacking (die-die, die-wafer)	• **X-rays techniques, Interferometry, Overlay** – large(r) features



Source: Synopsis, Inc.

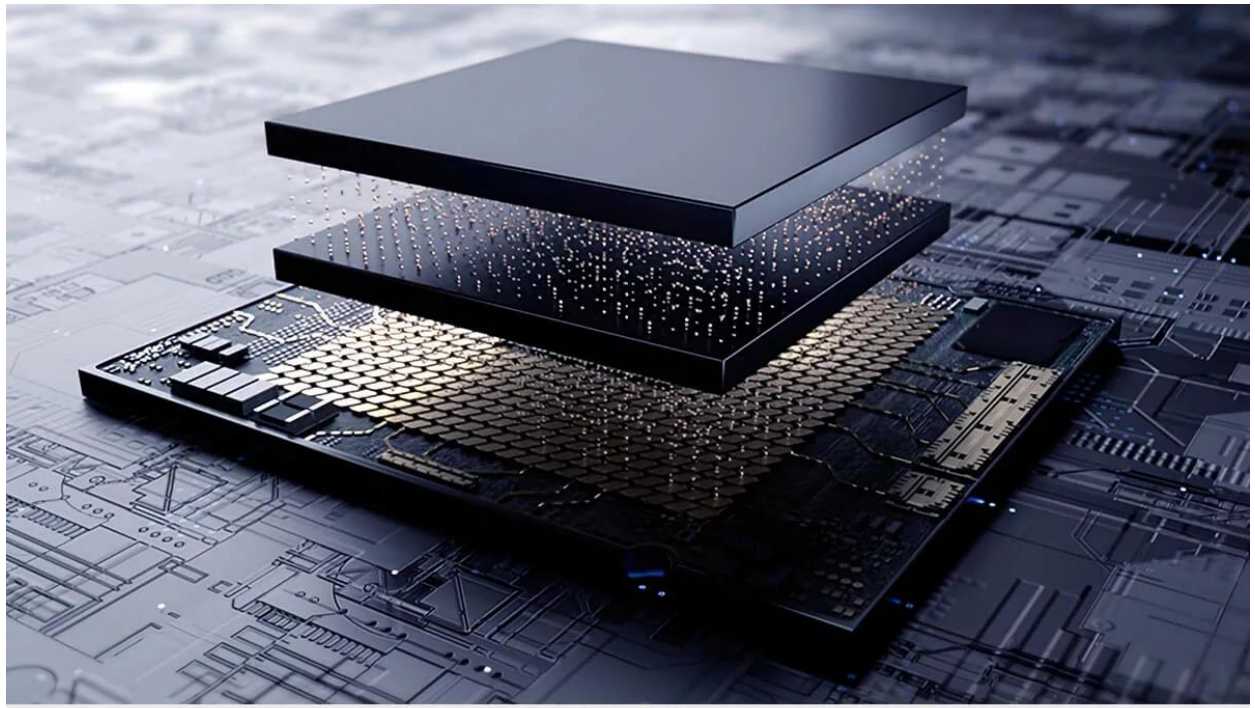
Chiplet Technology

2.5D Integration



Source: Samsung Electronics Co., Ltd.

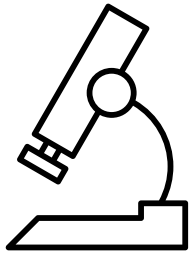
3D Integration



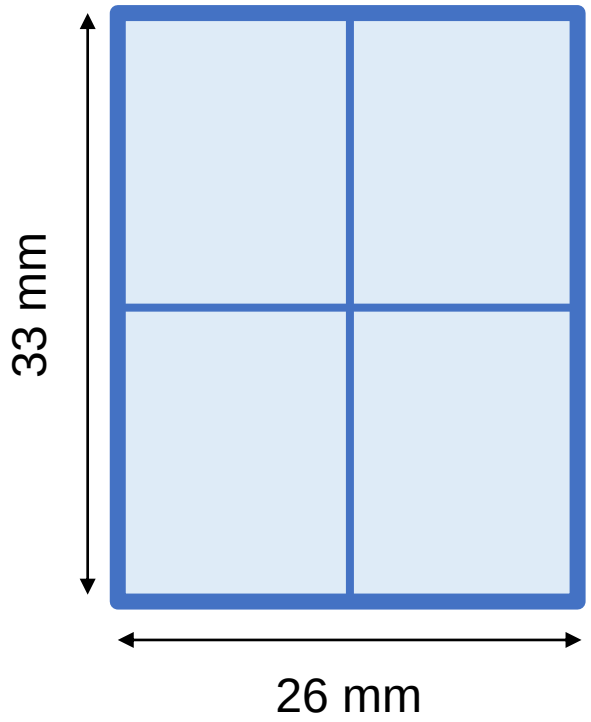
Source: Samsung Electronics Co., Ltd.

https://www.synopsys.com/multi-die-system/how-multi-die-systems-will-change-semiconductor-design.html

GENERAL METROLOGY CONSIDERATIONS



In-line Metrology Requirements



maximum exposure field size on wafer (full-field tool)

Real estate within the exposure field is very expensive

→ scribe lines on the order of 50 to 100 µm must fit all essential metrology targets, such as:

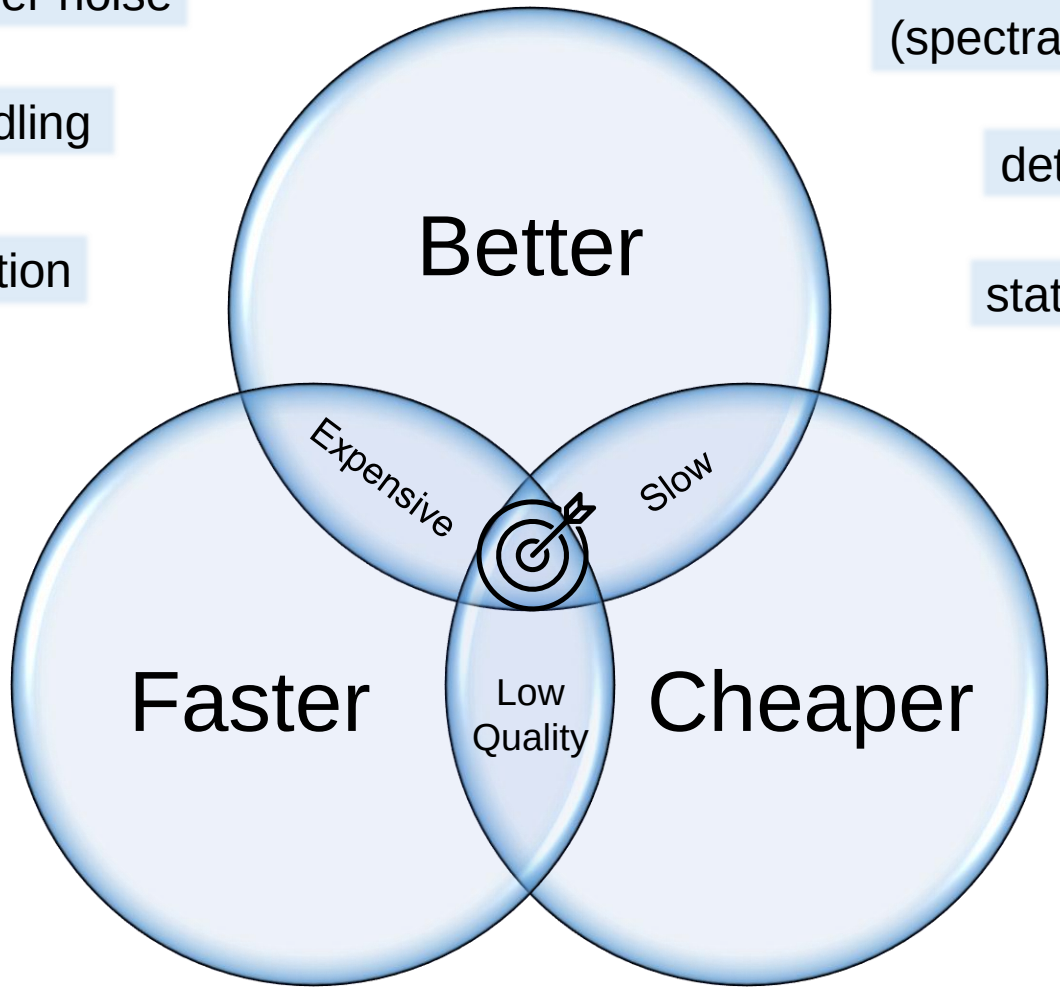
- Alignment marks and overlay targets
- Process control metrology (thickness, CD, material, etc.)

small targets desired (design rule clean, device-like)
more targets, more room for chip area

in-die metrology desired whenever possible
no target area required, “measure where it matters”

across-wafer sampling required
process uniformity important for performance

Metrology – Better, Faster, Cheaper, More



lower noise

big data handling

automation

MAM times

time to solution

defect classification

resolution (spectral, lateral, depth)

detection limits

statistics

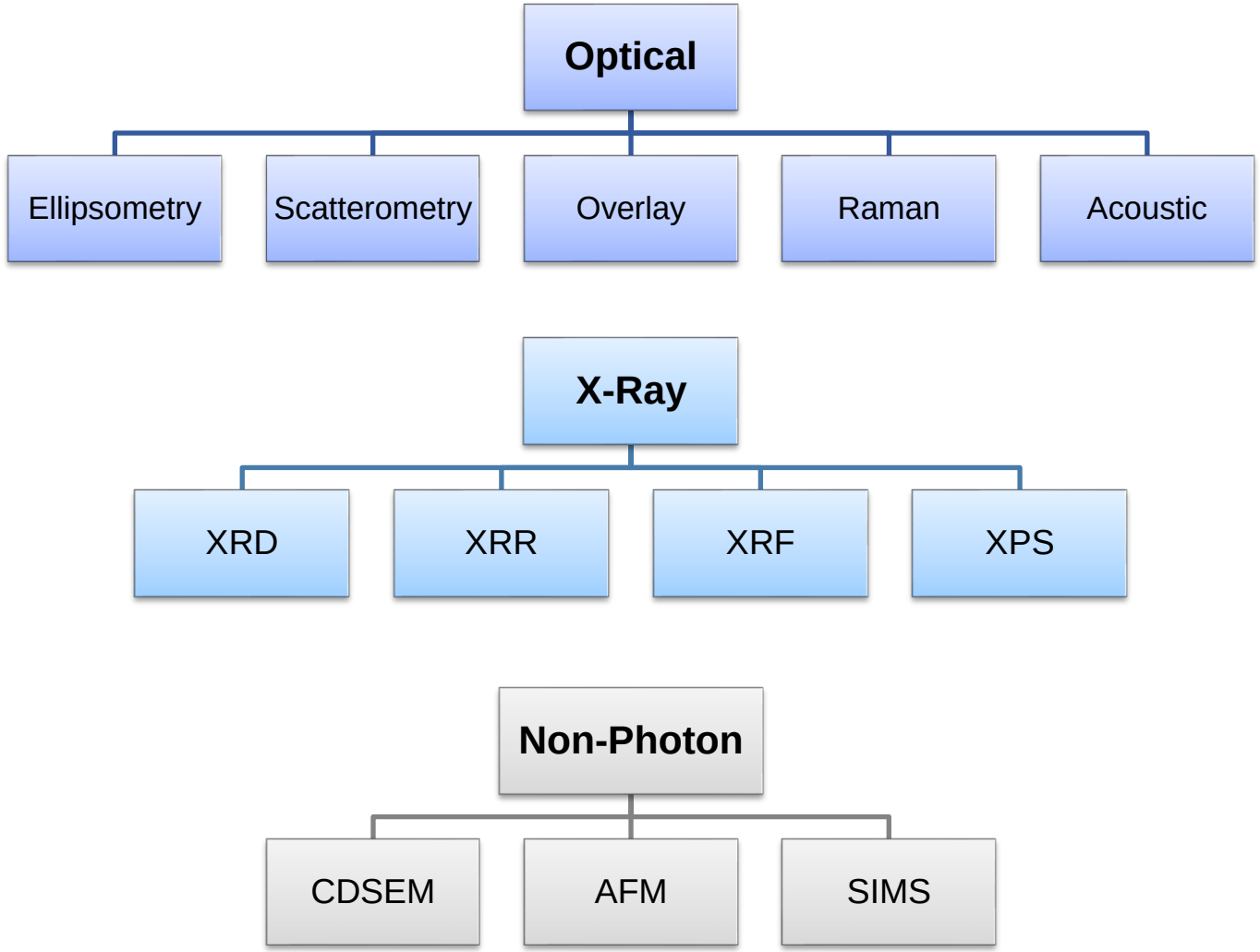
smaller spot size (real estate; in-die)

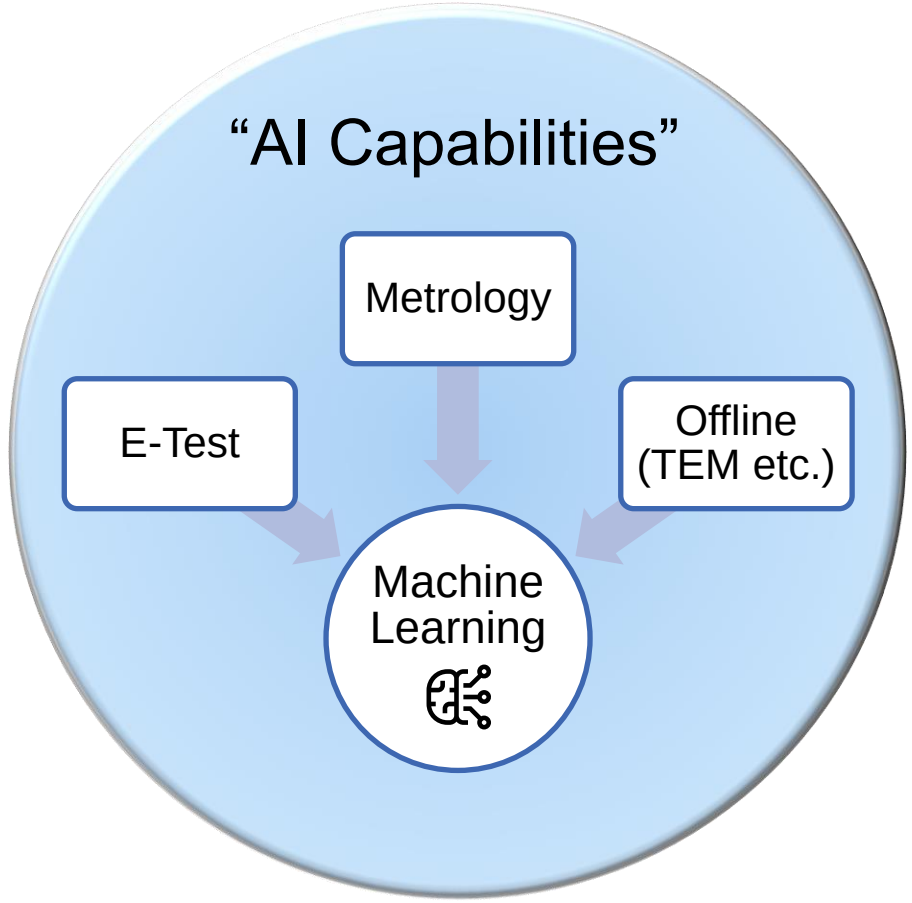
multi-beam

non-destructive

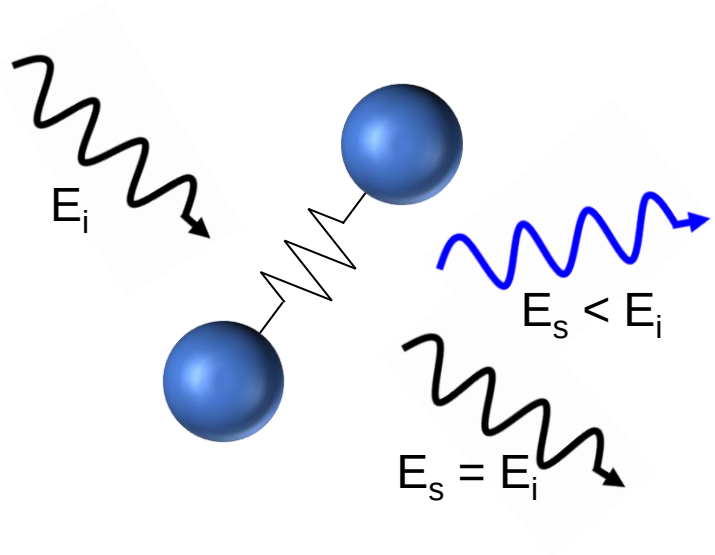
increased sampling (wafer, lot)

Available In-Line Metrology Techniques for Logic





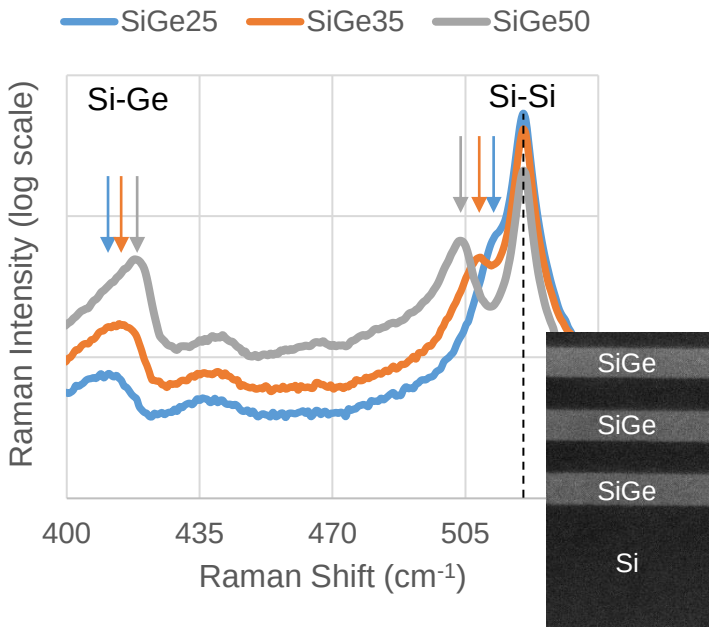
RECENT METROLOGY INNOVATIONS



Raman Spectroscopy

Inelastic scattering of monochromatic laser light

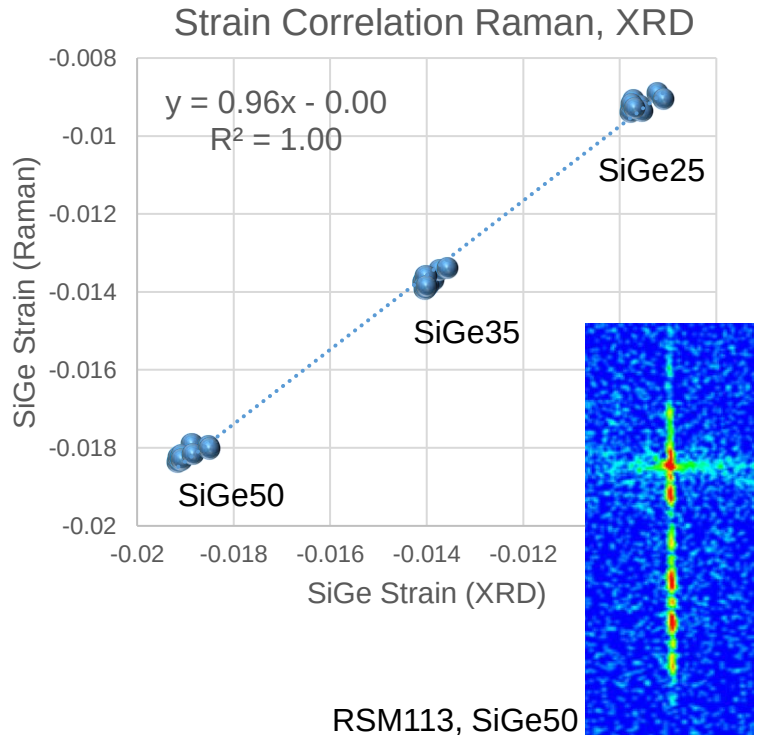
- Material characterization on fully integrated wafers
- Laser wavelength and polarization control important
- Translation from phonon mode position to physical properties required
  → “y-axis calibration”



$$\omega_{Si-Si} = 520.2 - 62.0x - 815\varepsilon$$

$$\omega_{Si-Ge} = 400.5 + 14.2x - 576\varepsilon$$

Phonon modes shift with composition (x) and strain (ε)

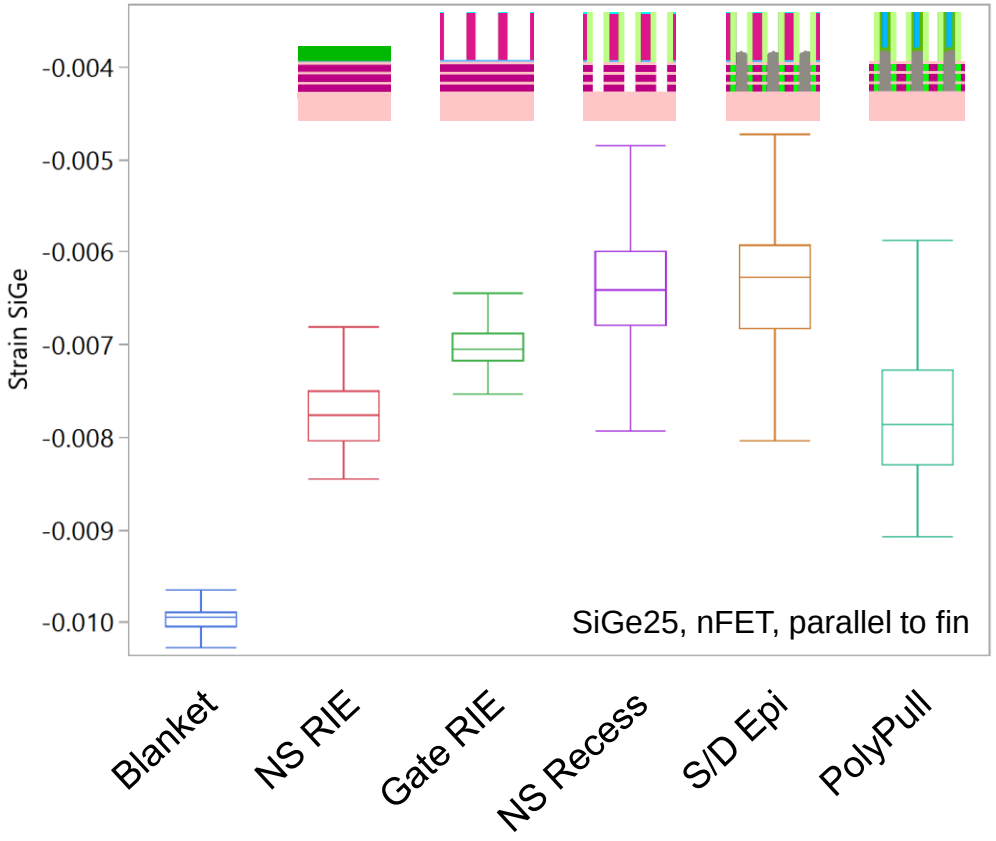


excellent correlation to reference

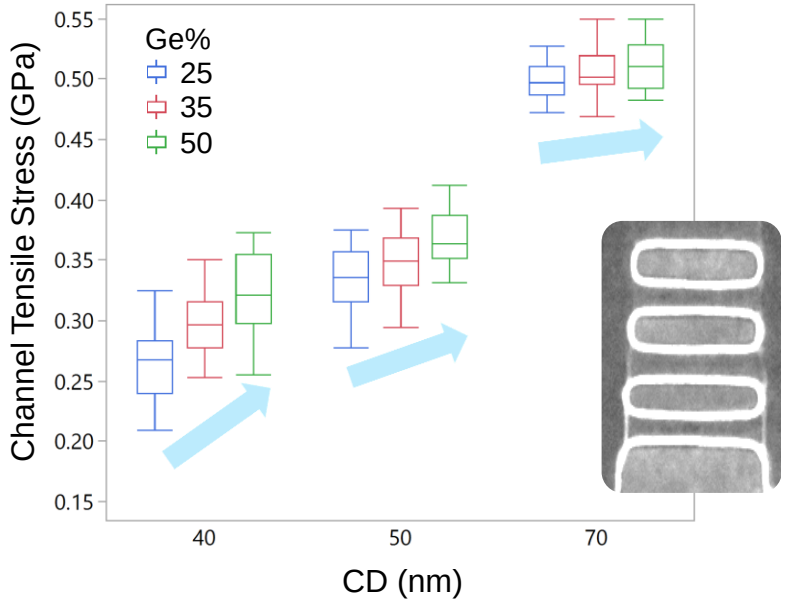
Schmidt et al., JM3 021203 (2022).

Raman Spectroscopy

SiGe Nanosheet Strain Evolution Through FEOL Processing



channel stress after release
as a function of sacrificial SiGe



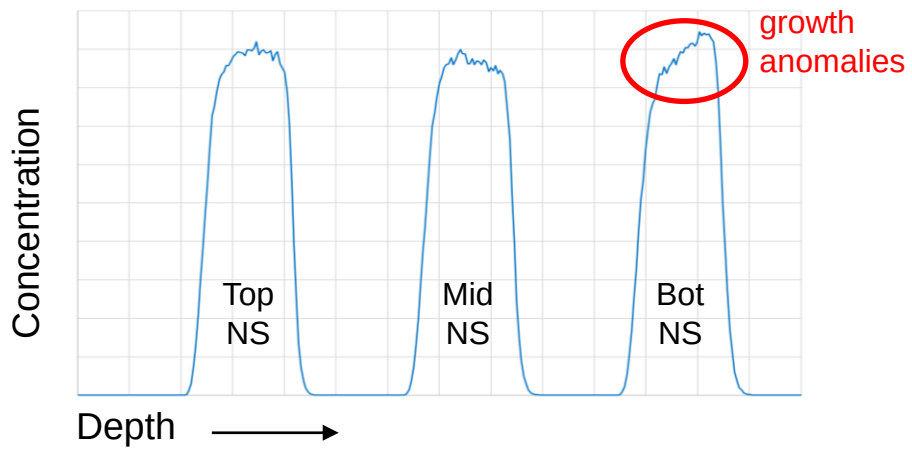
non-destructive Si channel stress characterization

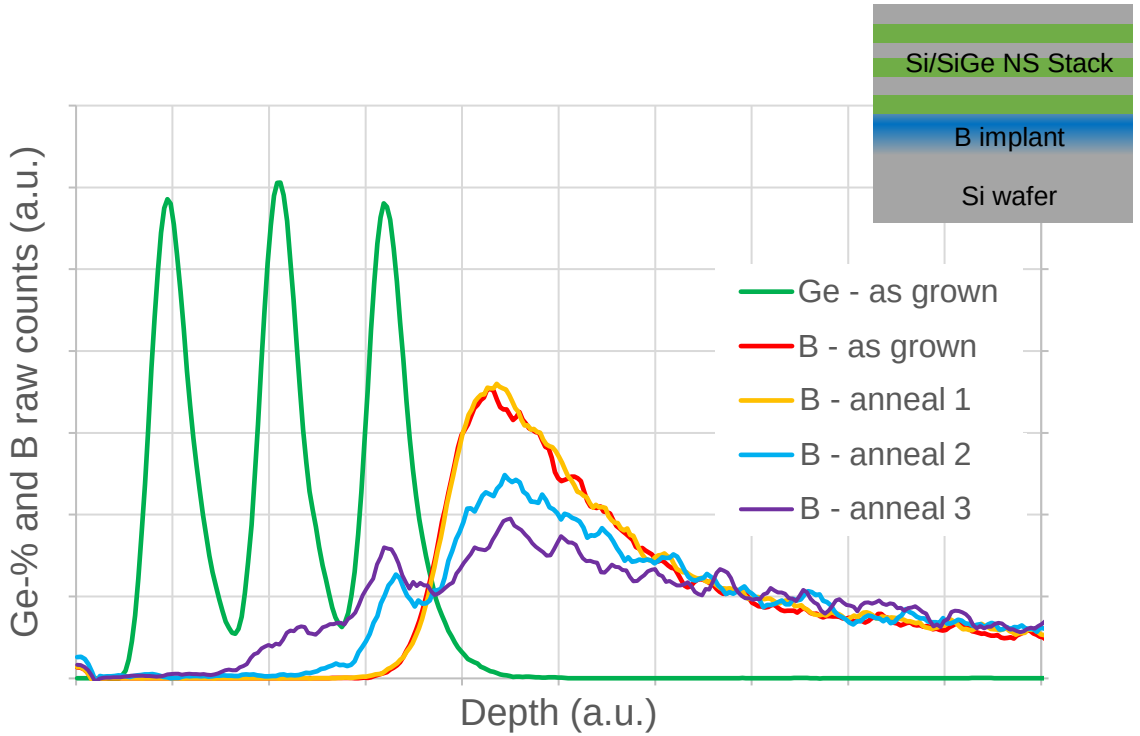
Schmidt et al., JM3 021203 (2022).

Secondary Ion Mass Spectroscopy (SIMS)

Fully automated in-line SIMS available

- composition/concentration profiles
- process development/monitoring
- fast turn-around times
- keep wafers moving (“non-destructive”)

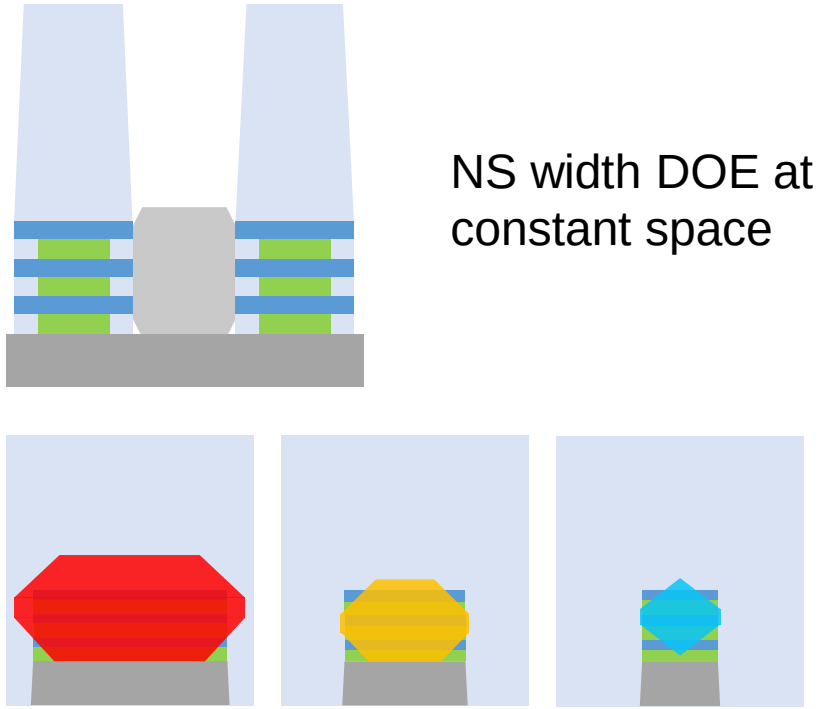




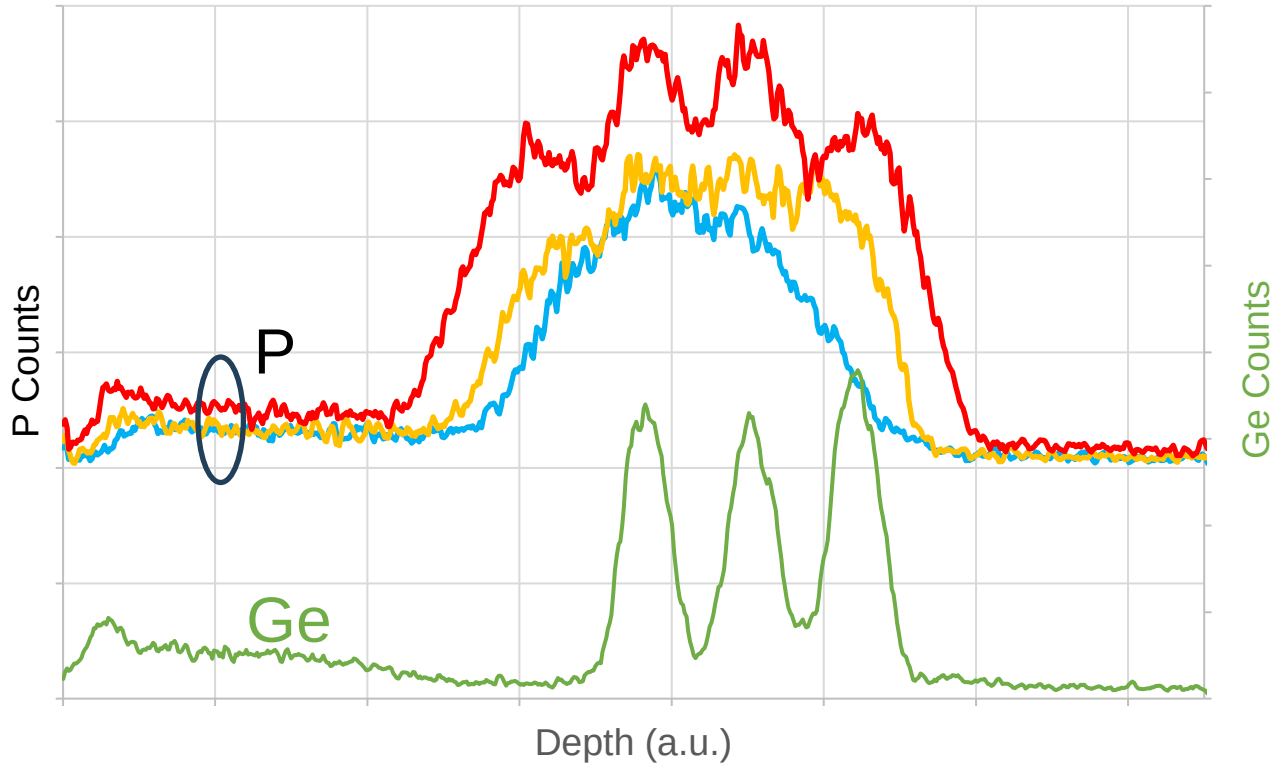
- wafer measured and cycled through anneal steps
- fast and accurate evaluation of process temperature budget

Schoeche, Schmidt et al., SPIE ALP 1295508 (2024).

SIMS on Structure – nFET Nanosheet Architecture



NS width DOE at constant space



P profile and epitaxy height including overburden and failure modes

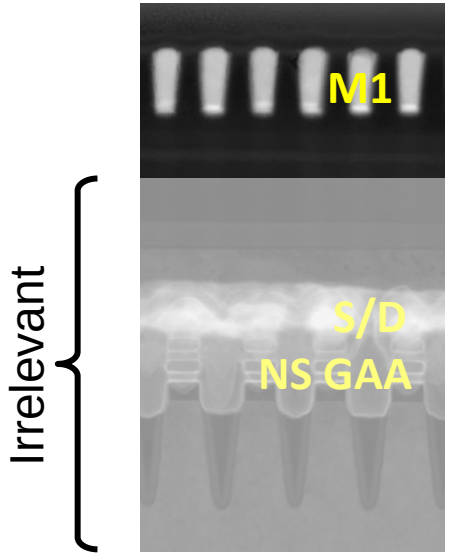
Quantitative analysis can be enabled by utilizing structural information obtained by scatterometry

Schoeche, Schmidt et al., SPIE ALP 1295508 (2024).

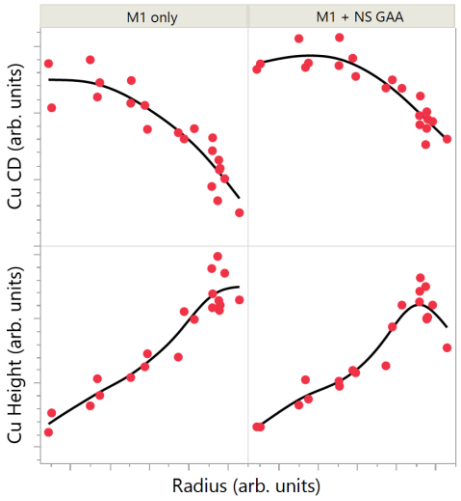
Spectral Interferometry and Vertical Traveling Scatterometry (VTS)

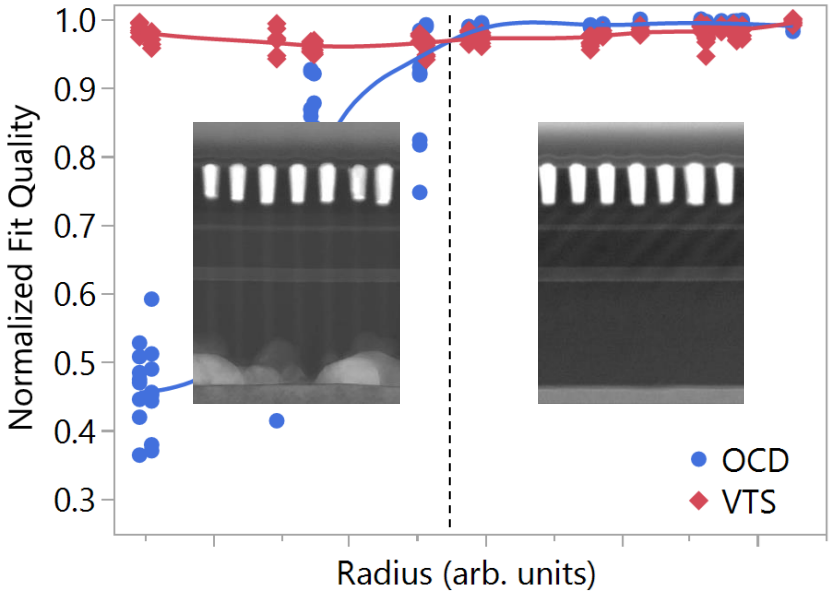
In-die metrology desired: "measure where it matters"

- measure absolute phase and filter depth information
- enables selective measurement of the top layer(s)



same VTS model





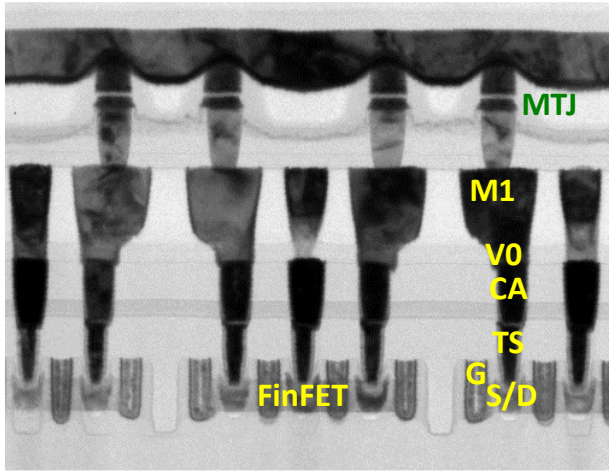
- OCD model showed location-dependent differences
- TEM confirmed defects

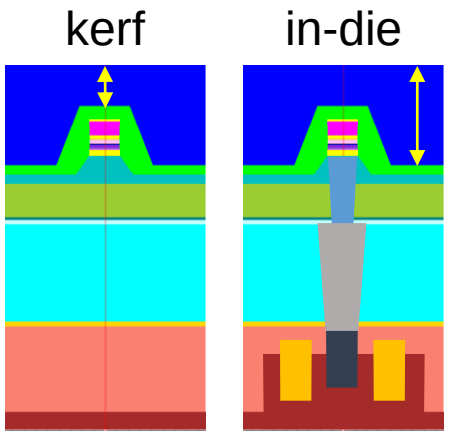
VTS model reports M1 metrics independent of underlayers → agnostic to FEOL process changes

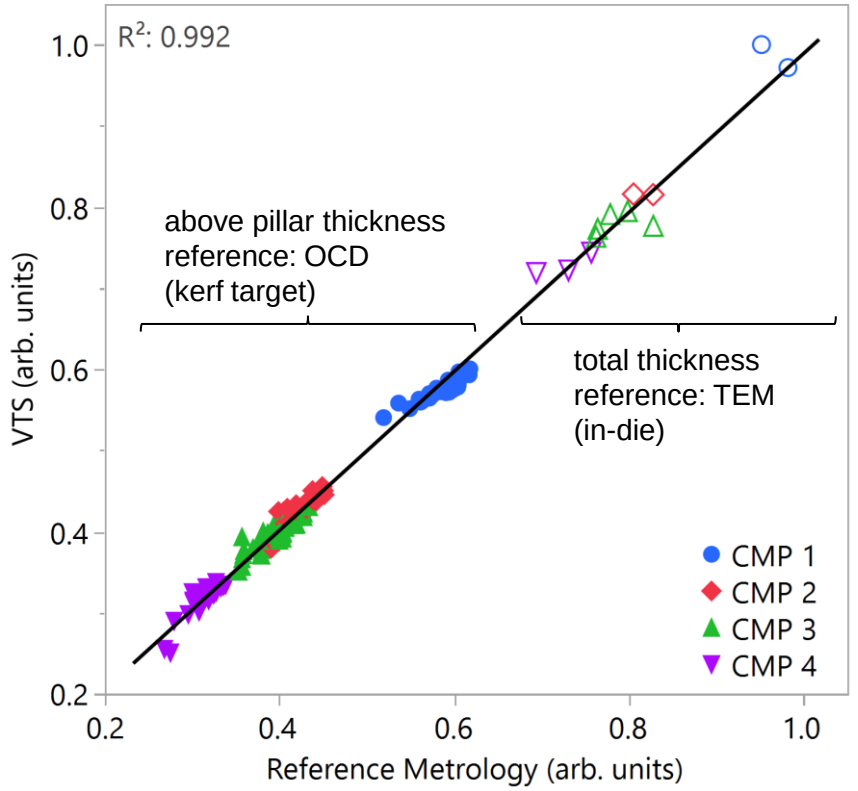
→ successfully filtered spectra

Schmidt et al., JM3 031203 (2023).

Vertical Traveling Scatterometry (VTS) for embedded MRAM







Integration scheme requires ILD CMP prior to M2 patterning

- ILD thickness strongly macro/density dependent
- in-die ILD measurements desired to avoid defects

➢ **VTS enables in-die metrology solution without the need for a complex optical model**

Schmidt et al., JM3 031203 (2023).

HIGH-NA EUV METRO CHALLENGE

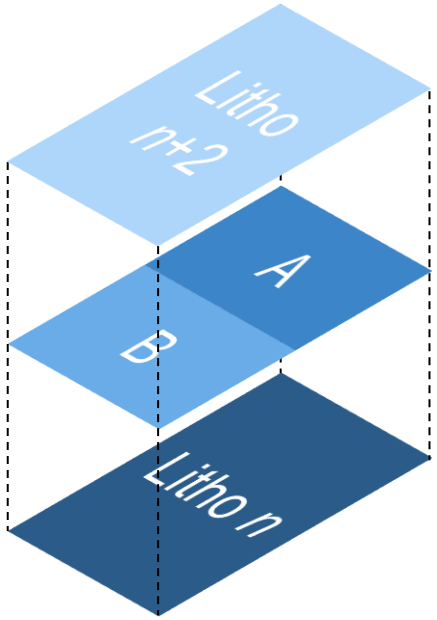
Advanced Overlay Metrology Needs

Large Chip Scenario

Litho *n*+2
"full-field"

Litho *n*+1
High-NA
"half-field"

Litho *n*
"full-field"



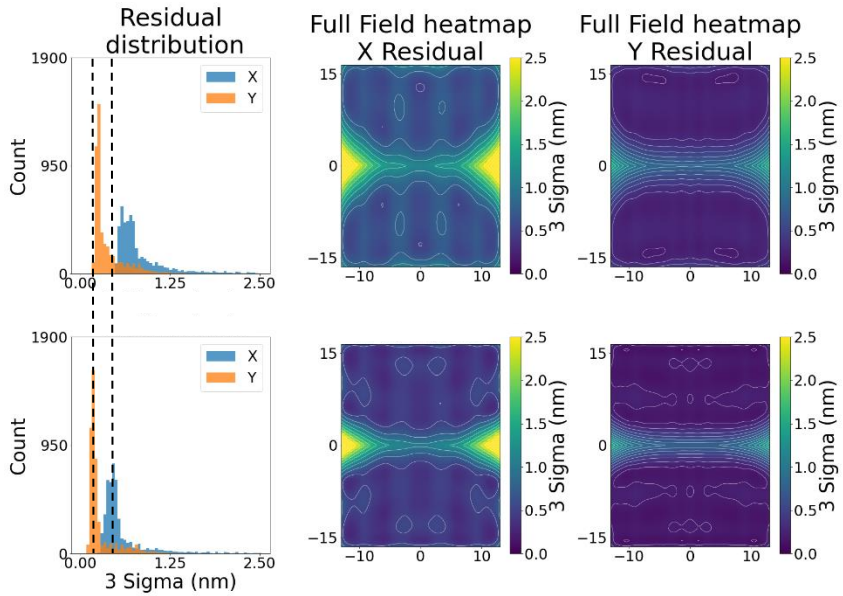
High-NA requires
two different reticles

Low-NA and High-NA mix-and-match printing will introduce new overlay error components

- inter-field control critical, requires enhanced overlay algorithms
- additional overlay targets required, may be in active area
  → smaller targets, faster metrology

19 parameter overlay model

57 parameter overlay model



field boundary is high overlay risk area
→ stitch overlay critical

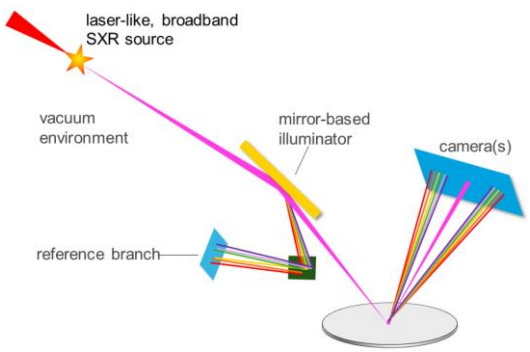
Lallement, Schmidt et al., SPIE ALP 124940S (2023).

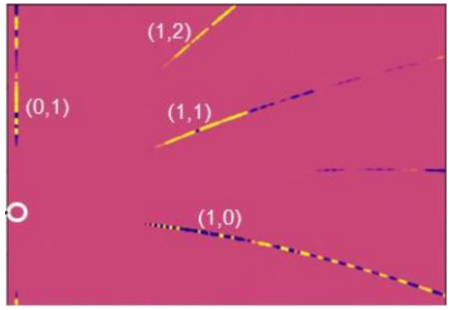
NEXT-GENERATION FAB TOOLS

EUV and X-ray Scatterometry Developments

Shorter wavelengths lead to increased sensitivity

Soft X-ray Scatterometry

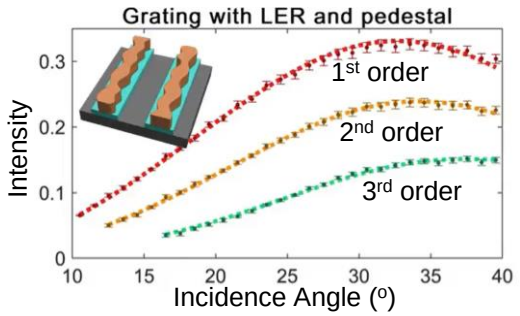




Porter et al., SPIE 12496 (2023).

- Rich diffraction signals
- Critical dimensions metrology and overlay
- Further source developments required
- Modeling can become very complex

Bright x-ray sources required!

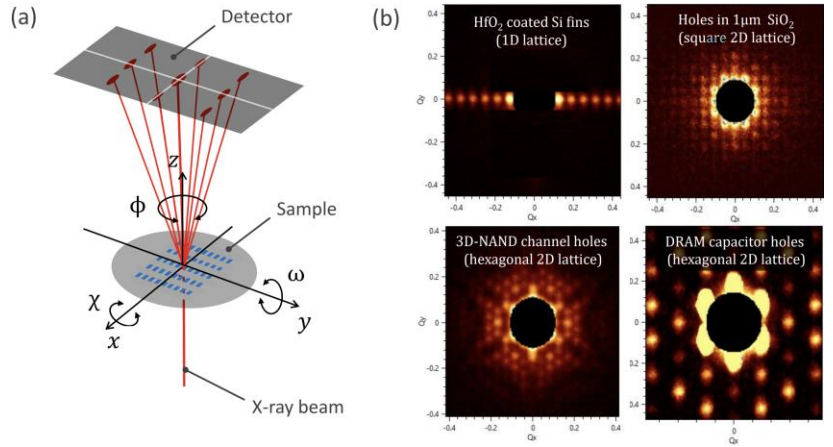


EUV Reflectometry

- Higher orders carry information about LER

Esashi et al., SPIE 12496 (2023).

T-SAXS tools commercially available – large spot size limits applicability in logic



Wormington et al., SPIE 11611 (2021).

A new lithography source might be handy for metrology!

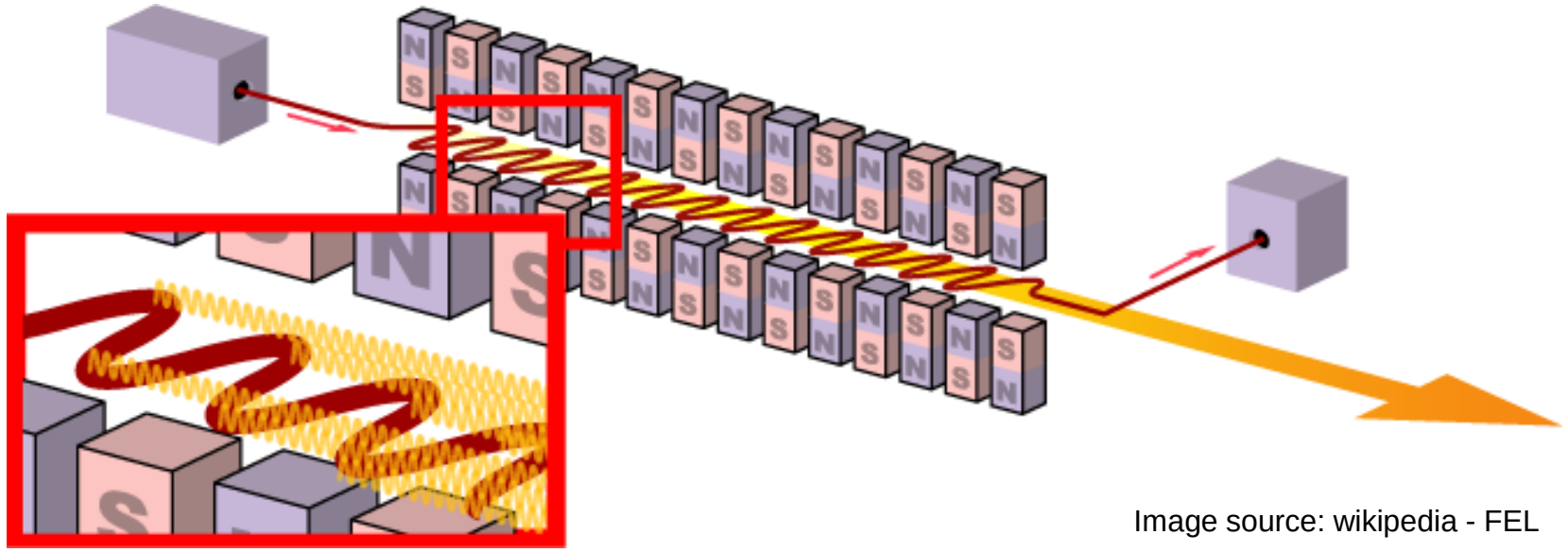
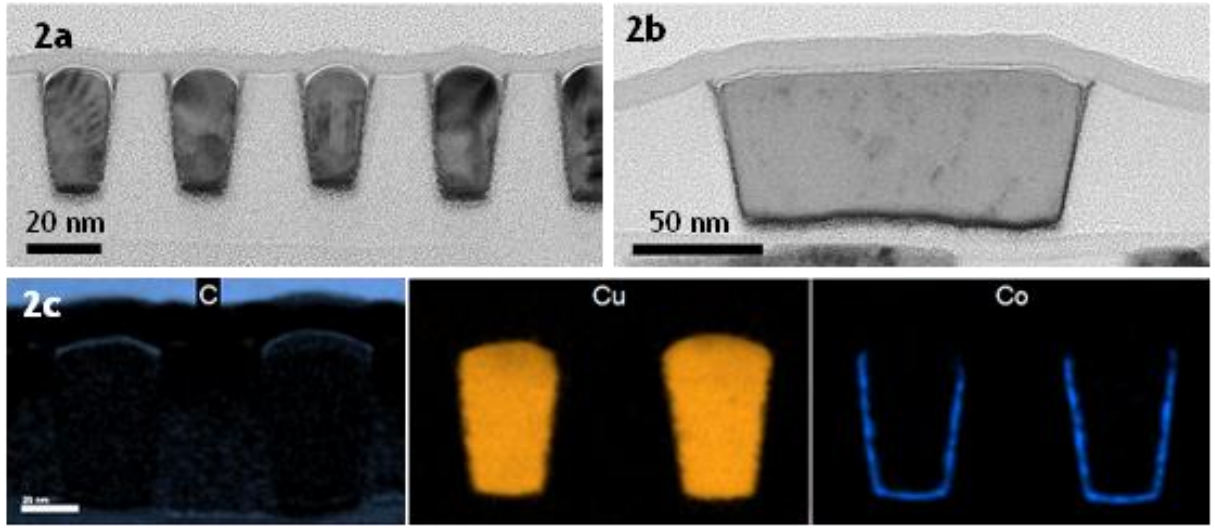


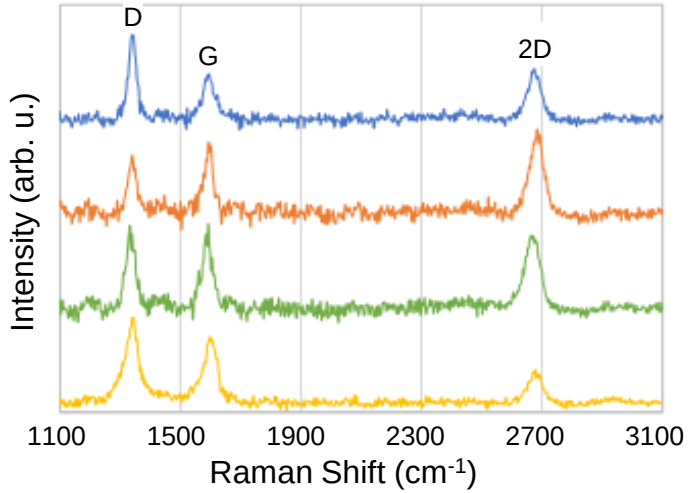
Image source: wikipedia - FEL

Free Electron Lasers (FELs) are being looked at as a next-generation lithography source

→ high brightness and high energy source may enable new in-line metrology capabilities!

What's Next: 2D Materials Characterization

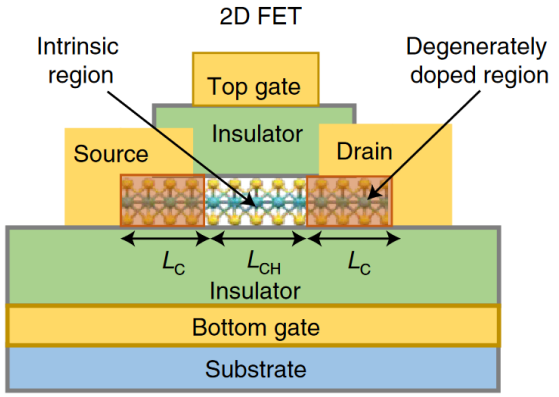


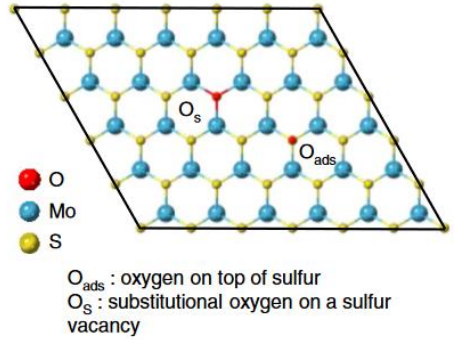


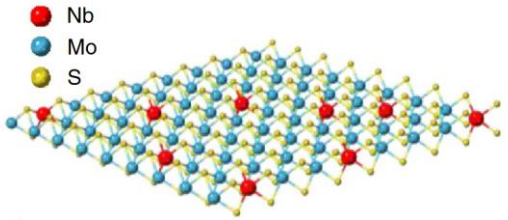
Graphene cap formation on 300 mm wafers

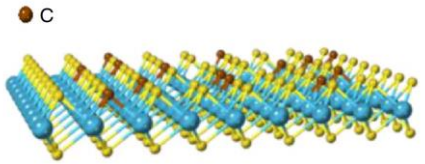
Nogami et al. IEDM 2021

Transistors with two-dimensional channels









Electrical | Chemical | Optical | Structural

Das et al. Nature Electronics 4, 786 (2021)

Overview of 2D Materials Characterization Methods

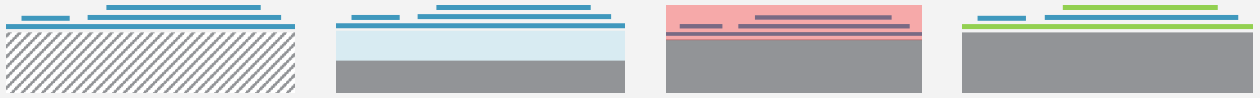
iDPC	STS KPFM C-AFM			EBAC EBIC	Hall bar vdP M4PP	Electrical
EELS EDX	TERS AFM-IR	FTIR THz-TDS	XPS RBS ToF -SIMS	Auger mapping		Chemical
	PiFM s-SNOM	PL SRDS				Optical
NBED HRTEM	STM AFM	Raman	XRD XRR	ECCI BSE-SEM		Structural

TEM **SPM** **Spectroscopy** **X-Rays - Ions** **SEM** **Electrical**

Defects (growth)

Processing

Interfaces &
devices stacks



Which ones are the next in-line tools

Celano, Schmidt, Beitia, Orji, Davydov, Obeng, Nanoscale Advances (2024). https://doi.org/10.1039/D3NA01148H

Takeaways

Increased process complexity continues to drive metrology needs

→ significantly more metrology required, more demanding requirements

Pitch scaling, backside power, monolithic integration, chiplet technology

→ all have specific demands but require fast, sensitive, and dense metrology

Broad in-line metrology portfolio already available

→ further developments of existing techniques and new lab-to-fab introductions required

- **Metrology is a process enabler, not just yield enhancer**
- **Decreased measurement uncertainty translates to improved device performance**

The metrology future is bright!

Acknowledgements

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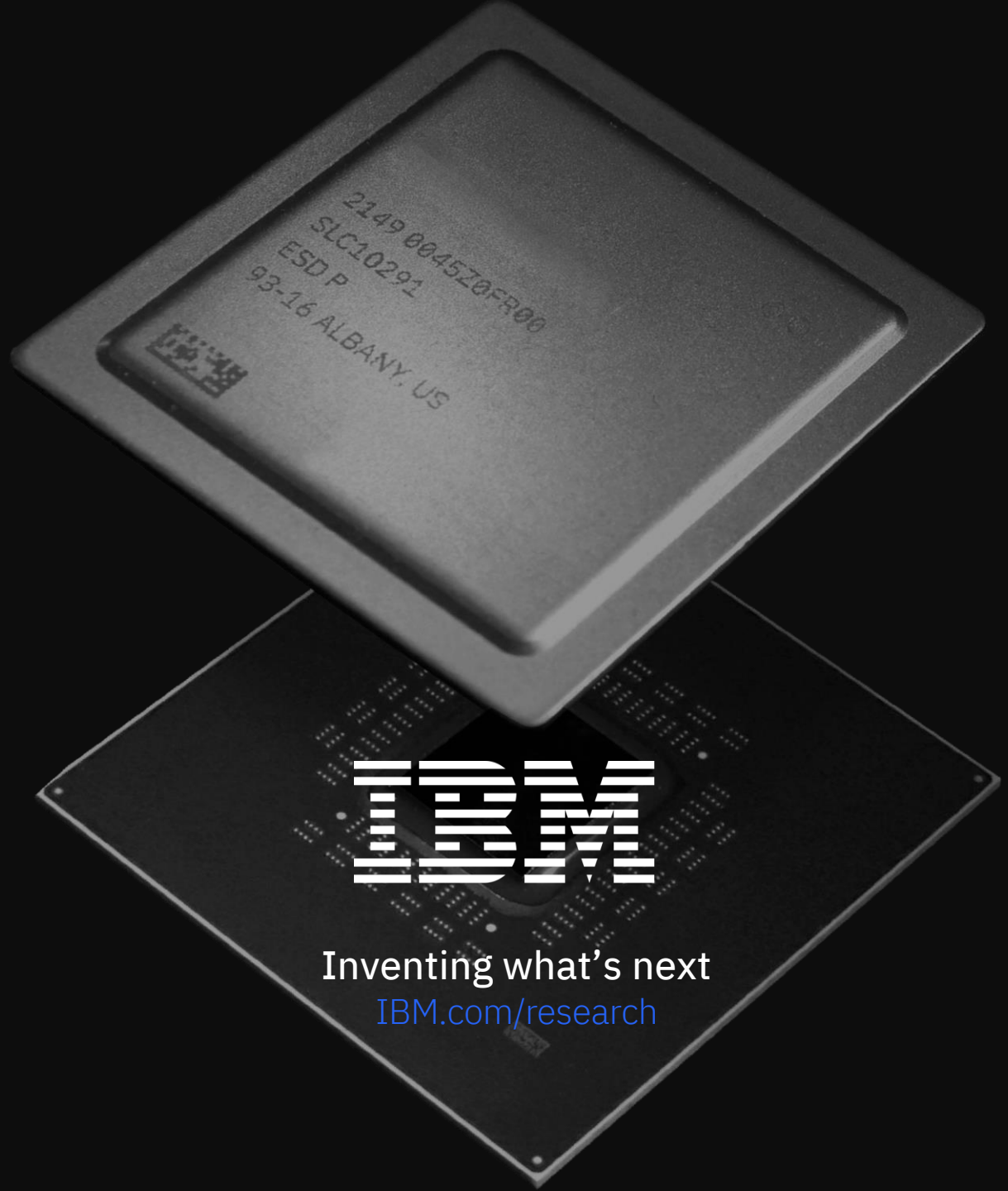
Alliance and Ecosystem Partners at Albany, NY

Thank You for your Attention!



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