

Advanced Packaging

Next Generation Metrologies & Fault Detection Methods

Pooya Tadayon
Intel Fellow, Director of Assembly & Test Pathfinding

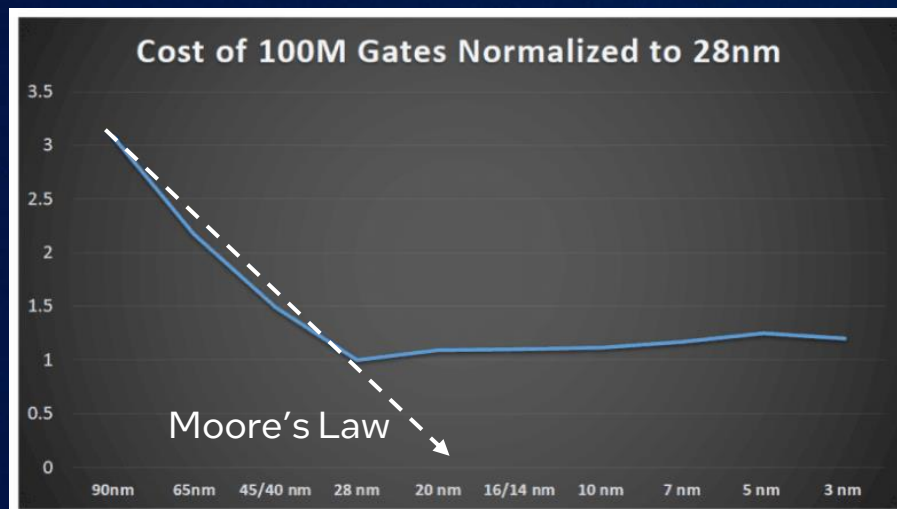
The Intel logo, consisting of the word "intel" in a white, lowercase, sans-serif font, is positioned in the bottom right corner of the slide. It is set against a solid blue rectangular background.

Executive Summary

- The era of 3D integration and advanced packaging is upon us, but the ecosystem is not ready
- Fine pitch features in advanced 3D packaging require metrologies to detect defects at all levels – surface and buried
- Innovative solutions are needed to enable non-destructive, sub-micron resolution, and high-speed metrologies

Advanced Packaging Technology Drivers

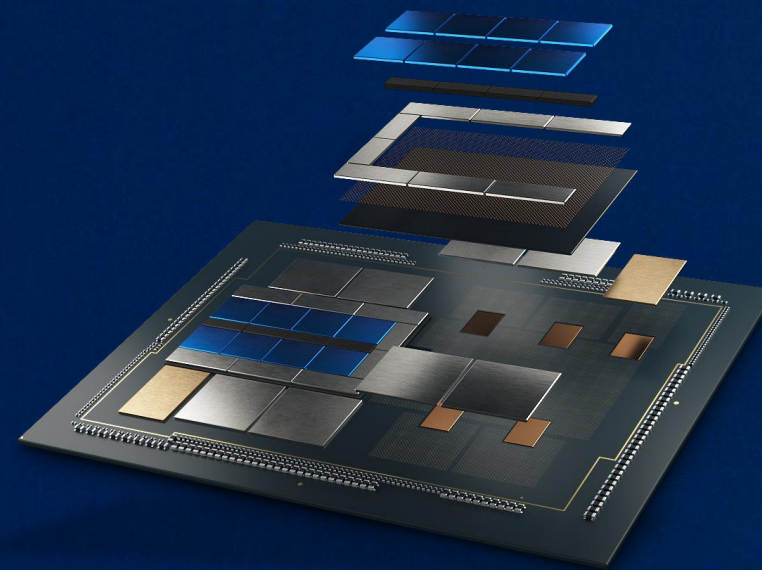
COST



Source: Google, IEDM23, SC1.6

Higher wafer cost drives
disaggregation

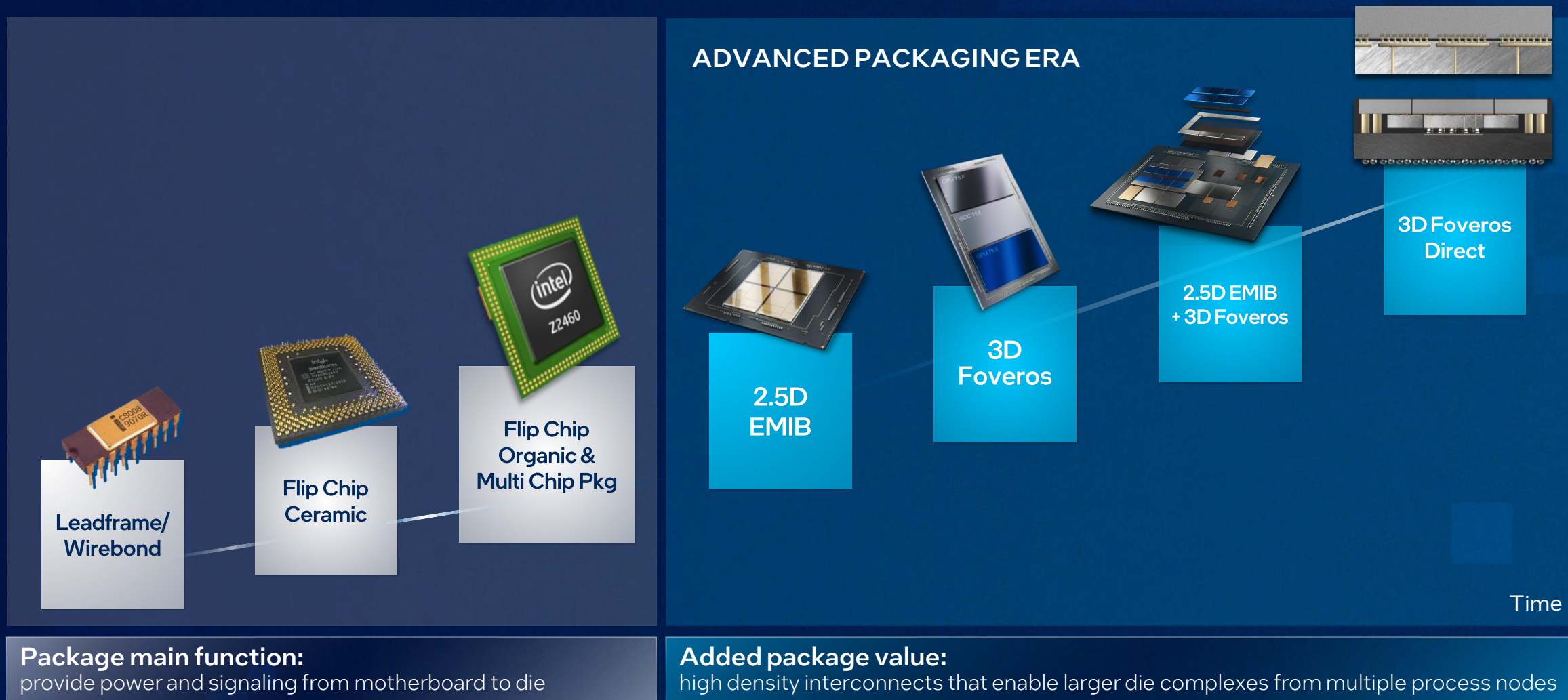
PERFORMANCE/SCALING



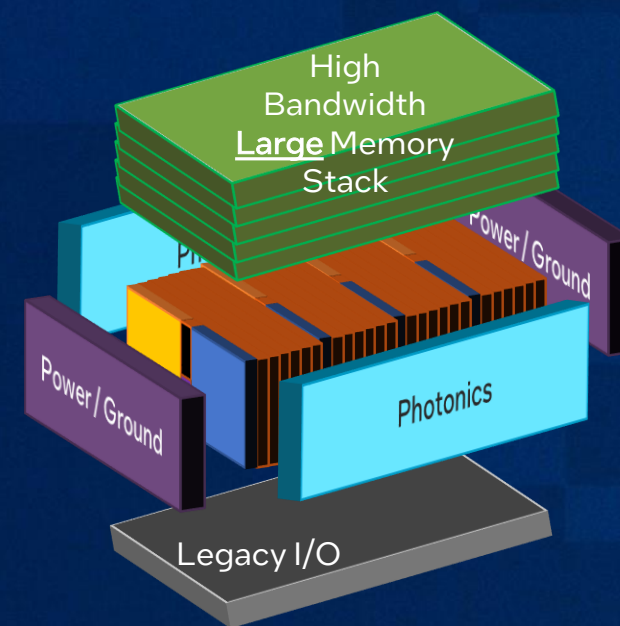
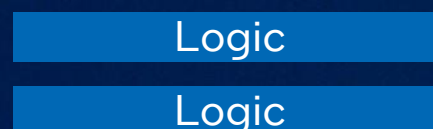
Need for complex sizes that
exceed the reticle limit

Advanced packaging is required to re-aggregate chiplets and build complexes larger than the reticle limit

Evolution of Advanced Packaging



Evolution of 3D Packaging



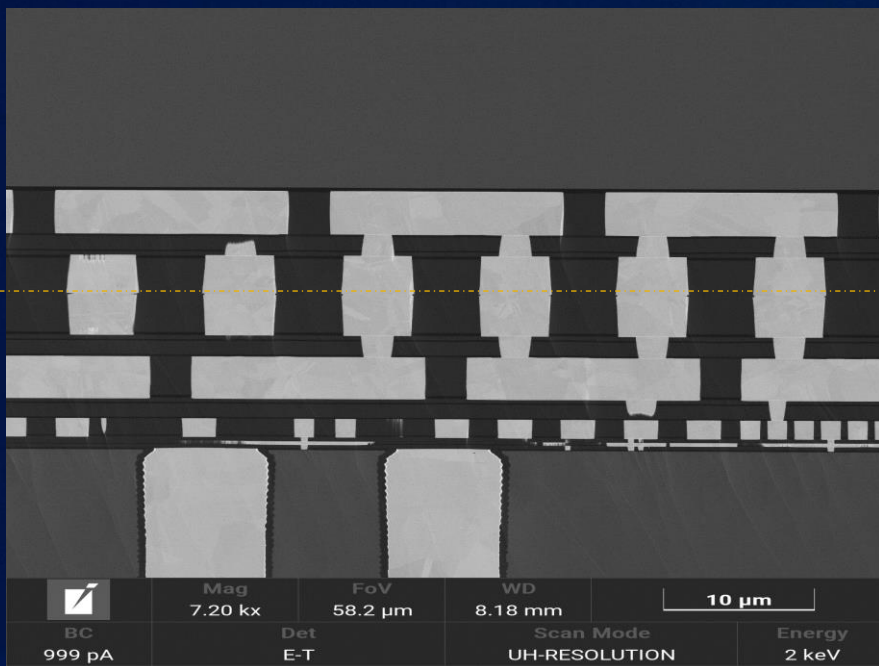
3D today
"planar"

3D future
"cube"

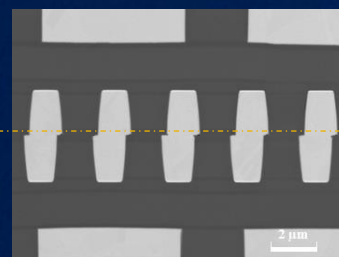
3D stacking will evolve to enable more complex and integrated devices

Key Trend: Pitch Scaling

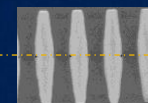
9 um pitch



3 um pitch



1 um pitch



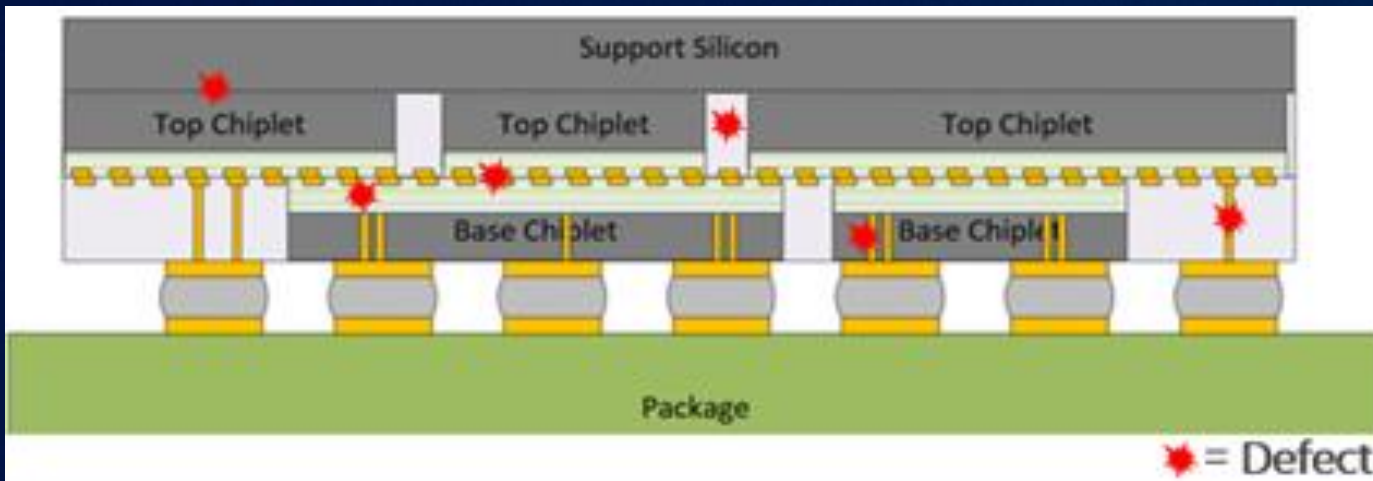
0.4 um pitch



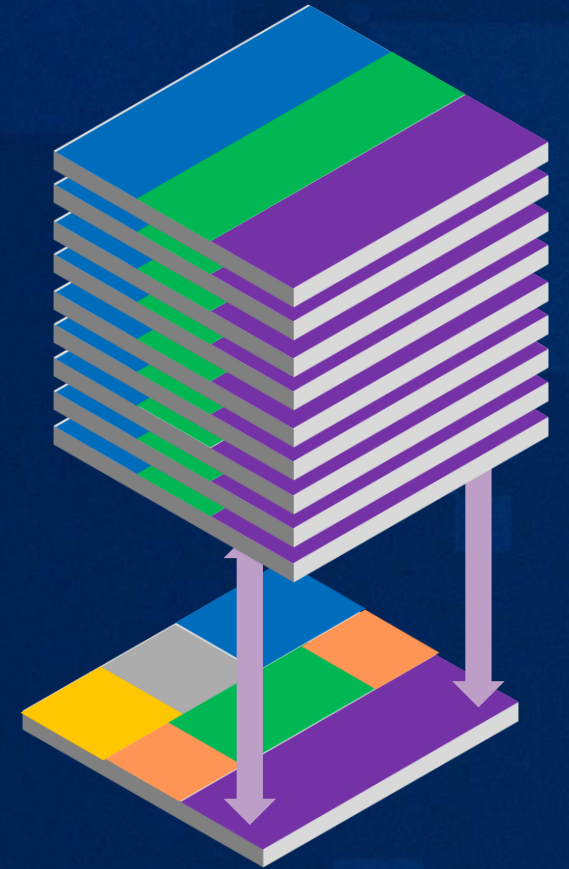
time

Cu-Cu hybrid bonding enables aggressive pitch scaling to ≤ 1 um

Key Challenges: Defect Isolation in Stacks

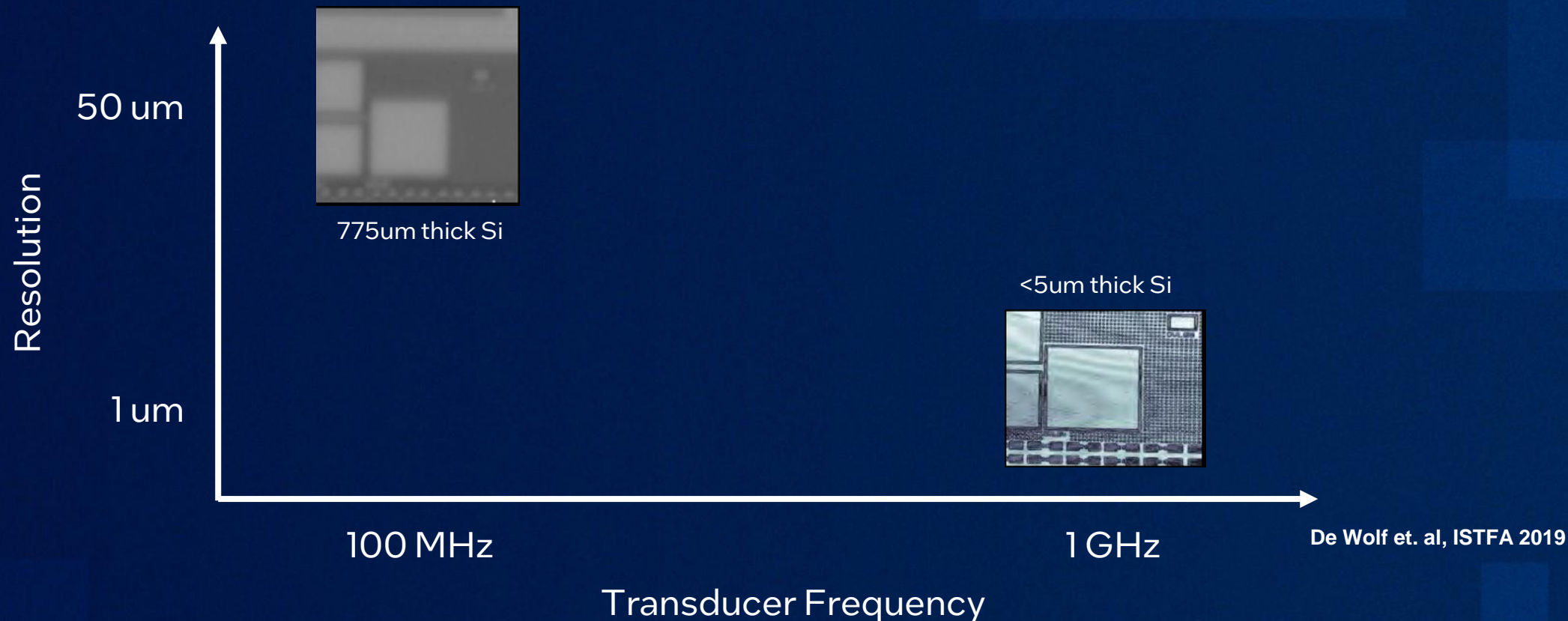


>>10 die
stack



As devices become more complex with reduced dimensions, more advanced defect isolation methods are required to pinpoint location of defects in buried structures

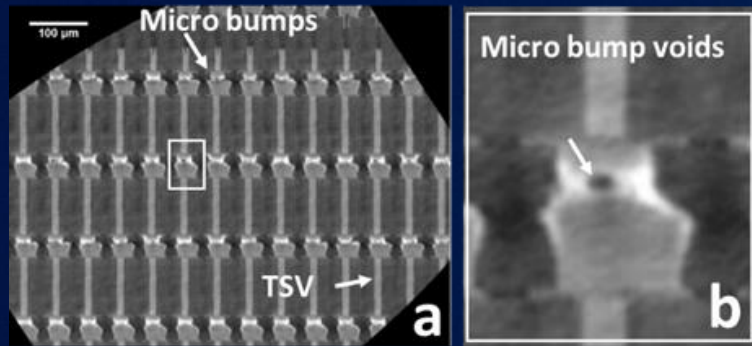
Key Challenges: High Resolution CSAM



CSAM is a critical metrology, but higher resolution requires sample prep/die thinning that is not always possible with 3D stacked structures

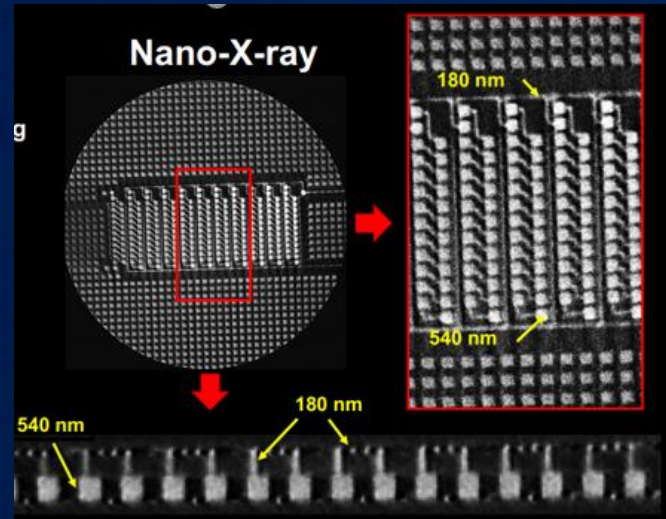
Key Challenges: High Resolution Imaging

Typical 3D X-ray for interconnect defects; no sample prep is needed



Cheryl Hartfield et. al. DOI: 10.1109/IPFA.2018.8452551

Nano 3D X-ray with $<1\mu\text{m}$ res.; sample preparation is needed



Christian Schmidt, Lorenz Lechner, Ingrid DeWolf, Soon-Wook Kim, Eric Beyn ECTC 2018

Sample prep and long scanning time needed to reach high resolution for fine pitch features will slow down yield learnings and impact time to market

Need innovation in imaging to quickly detect subtle defects buried under multiple interfaces non-destructively

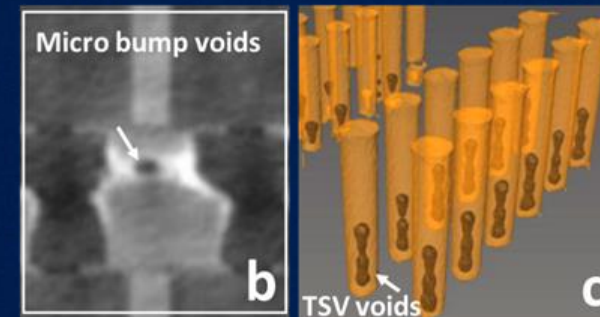
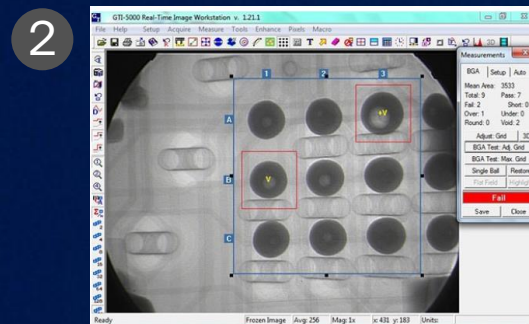
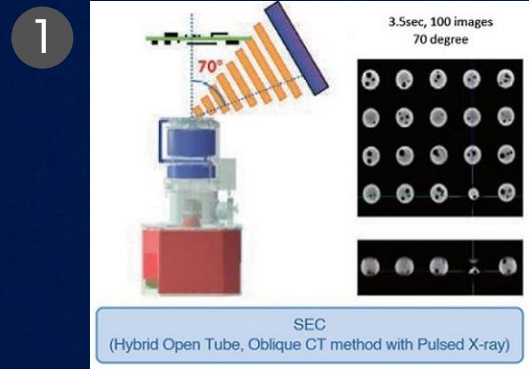
Key Challenges: High Resolution Imaging

Low resolution

Fast/Automated

High resolution

Slow/Manual

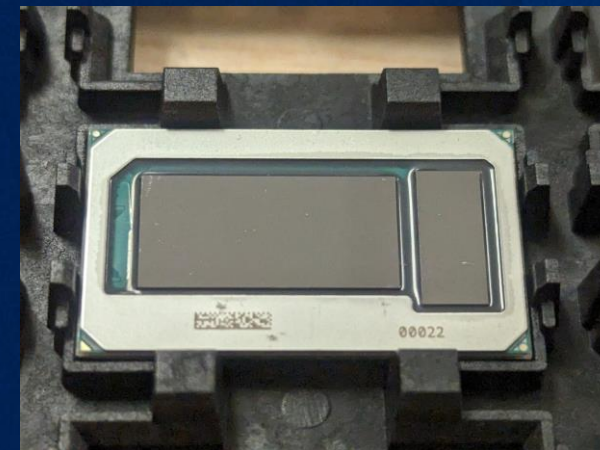
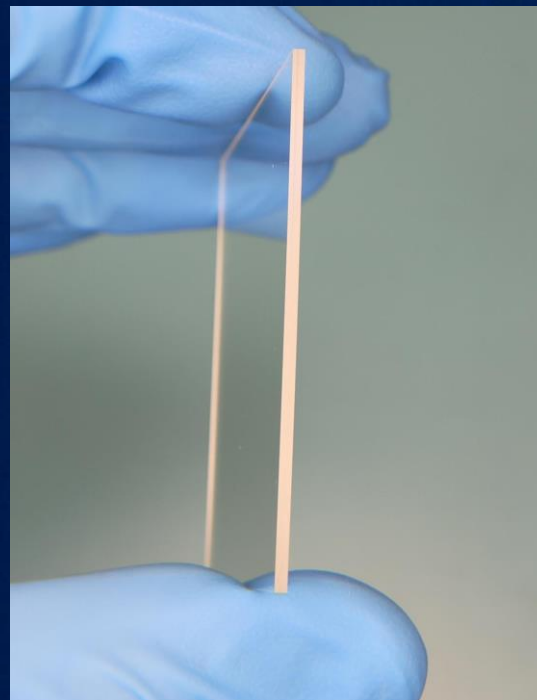
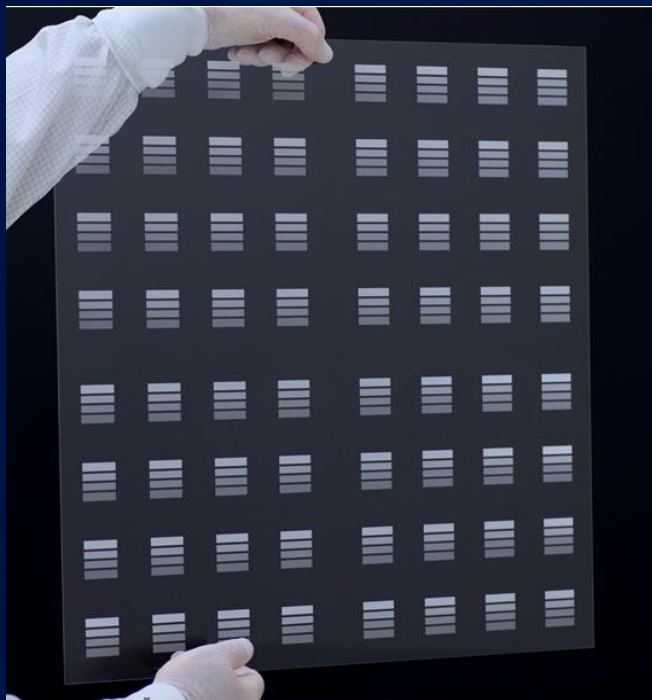


1. https://smtnet.com/news/index.cfm?fuseaction=view_news&company_id=54743&news_id=24997

2. <https://www.glenbrooktech.com/x-ray-inspection-system-rentals/bga-inspection/>

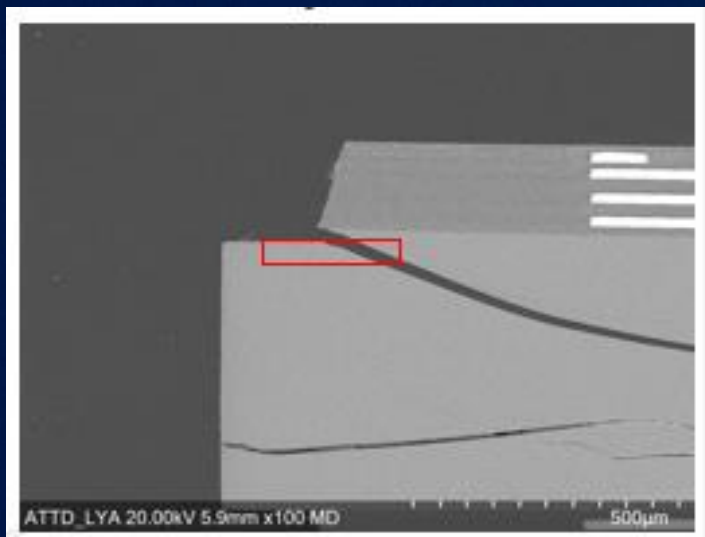
3. Yan Li and Deepak Goyal, "3D Microelectronic Packaging: From Architectures to Applications", 2nd edition, Springer, 2021, ISSN 1437-0387

Trends: Glass Substrates

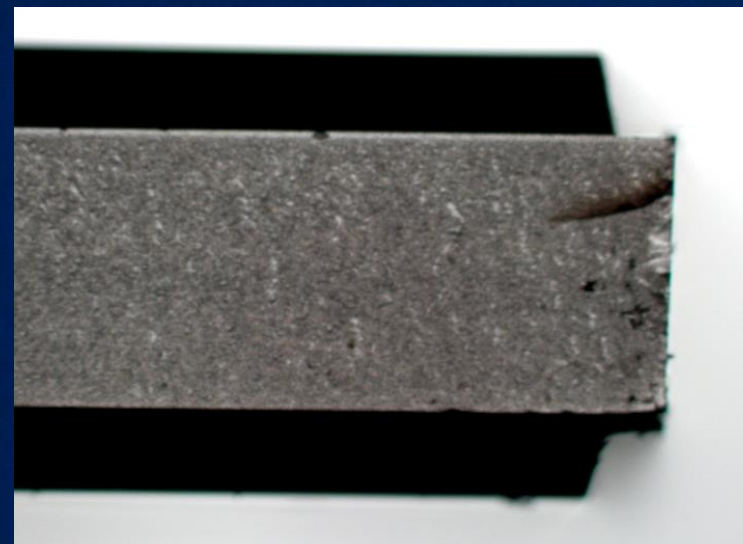


Glass offers improved material properties resulting in better dimensional stability and ability to scale

Key Challenges: Crack Detection



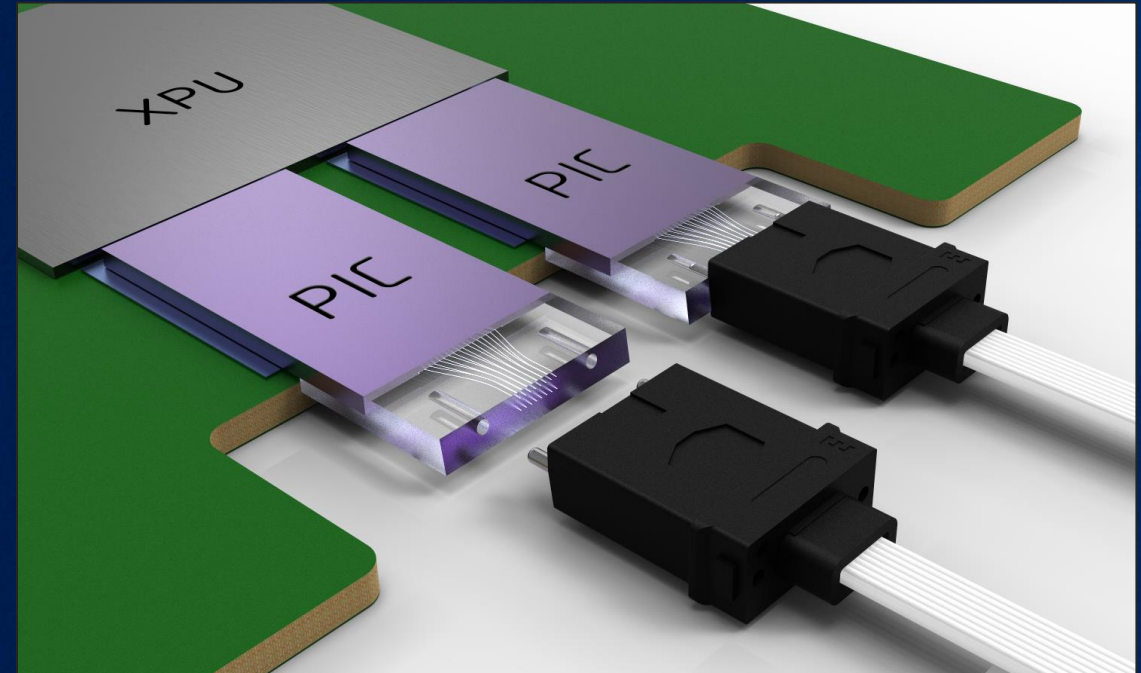
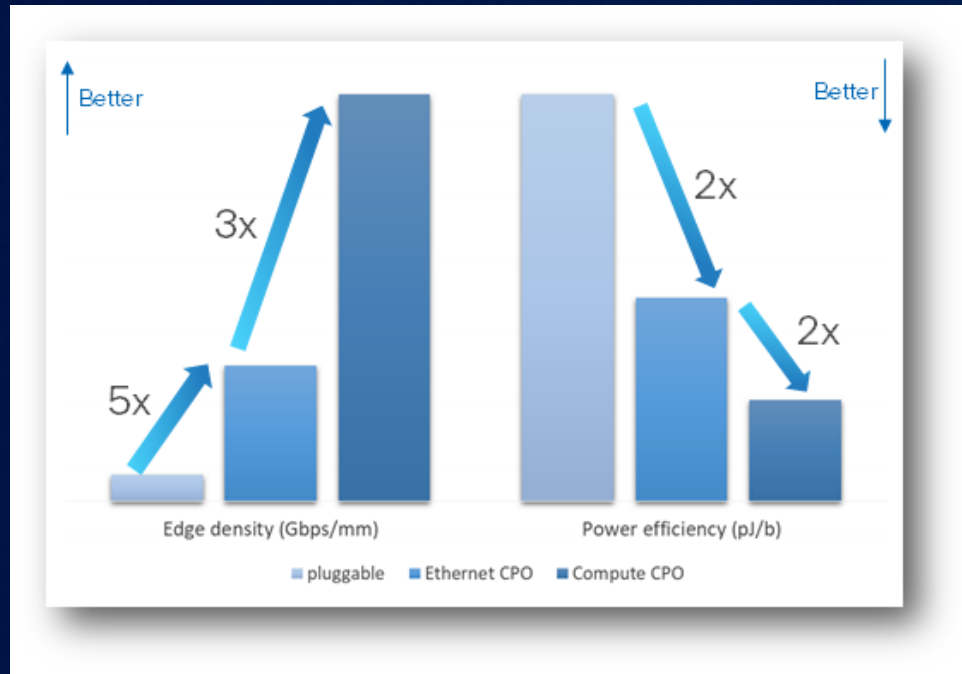
Edge defects due to singulation



Cracks that can become gross fails if undetected

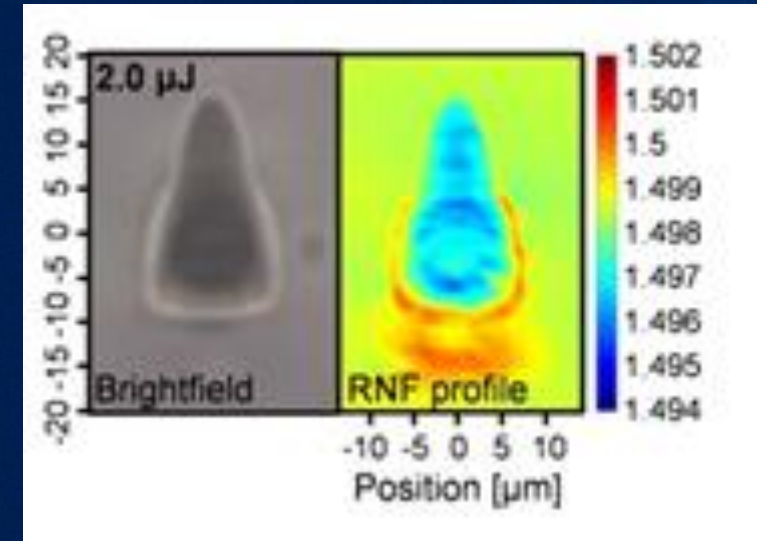
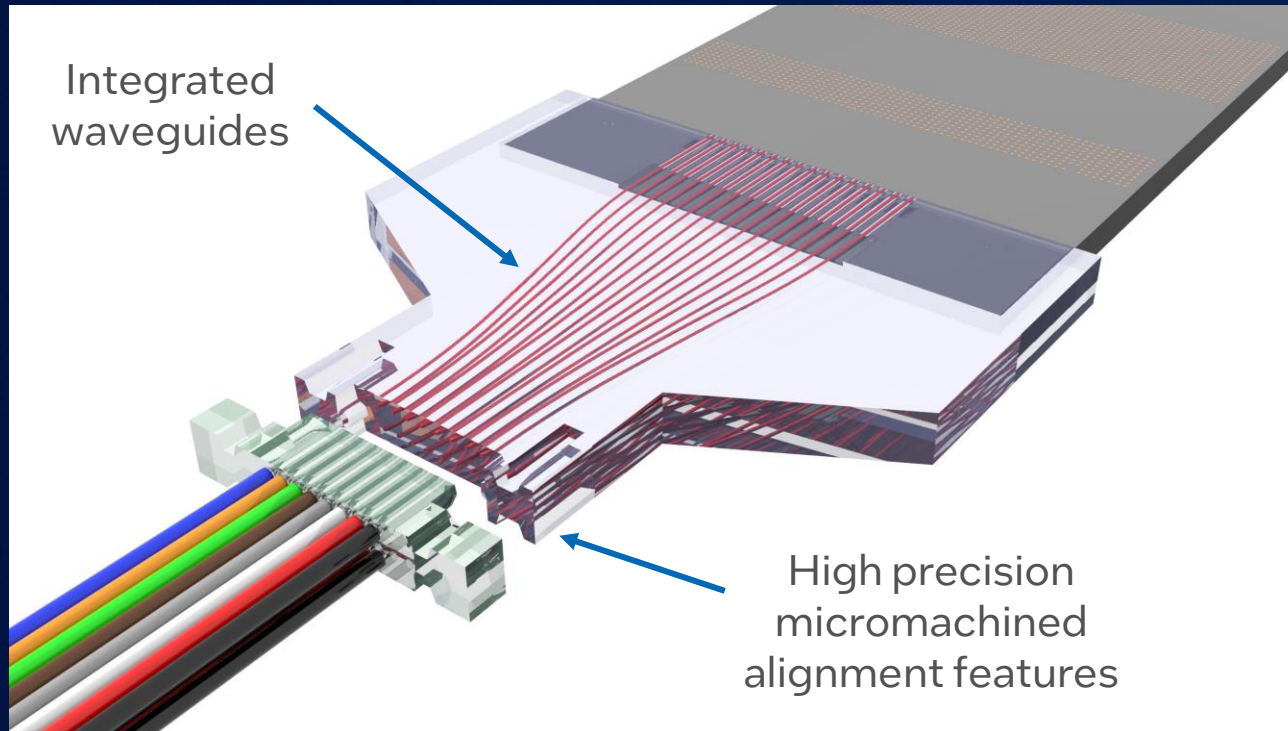
New in-line metrologies required to quickly detect micron-level cracks in glass substrates

Trends: Co-Packaged Optics



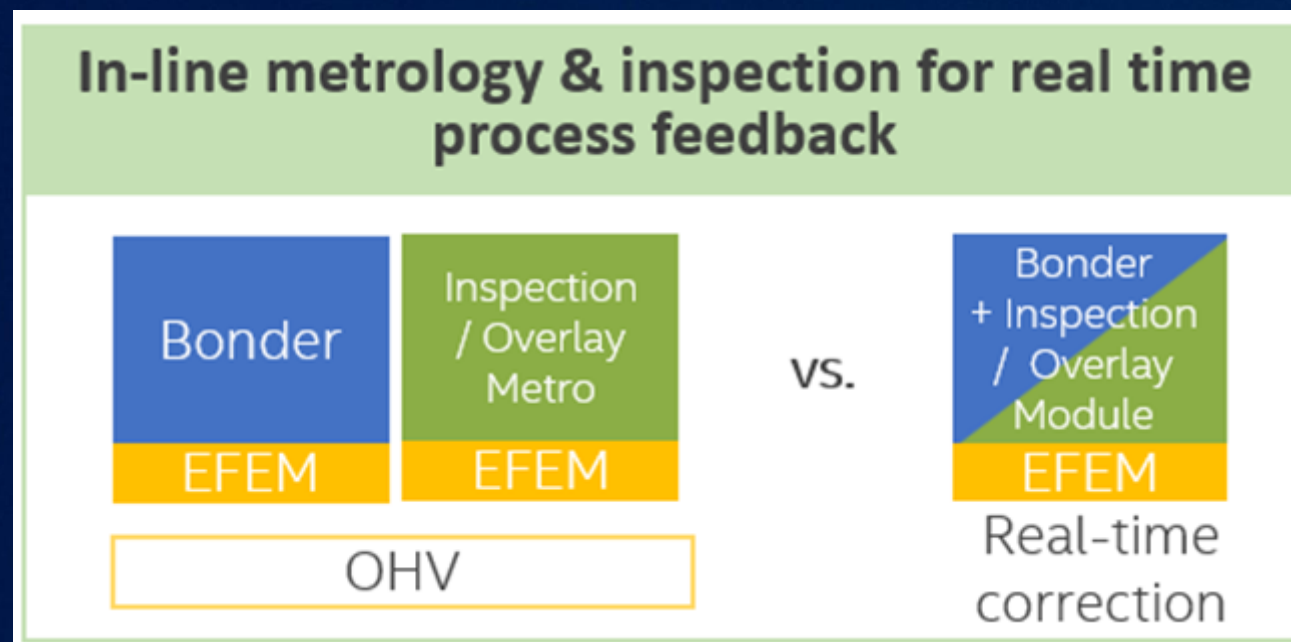
Glass bridge with integrated waveguides is key to enabling a high-volume compatible pluggable solution

Key Challenges: Metrology



Non-destructive methods for 3D mapping of optical waveguides in glass + high accuracy measurement of fine features on a transparent substrate

Key Challenges: Metrology



Need higher level of integration of metrologies inside process tools for real-time process feedback and control

Executive Summary

- The era of 3D integration and advanced packaging is upon us, but the ecosystem is not ready
- Fine pitch features in advanced 3D packaging require metrologies to detect defects at all levels – surface and buried
- Innovative solutions are needed to enable non-destructive, sub-micron resolution, and high-speed metrologies



All product and service plans, and roadmaps are subject to change without notice. Any forecasts of products, services or technologies needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Code names are often used by Intel to identify products, services or technologies that are in development and usage may change over time. Product, service and technology performance varies by use, configuration and other factors. No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. Learn more at www.Intel.com/PerformanceIndex and www.Intel.com/ProcessInnovation.

Reference to research results, including comparisons to products, services or technology performance are estimates and do not imply availability. The products and services described may contain defects or errors which may cause deviation from published specifications. Current characterized errata are available on request. Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade. Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings releases, annual report on form 10-K and other SEC filings at www.intc.com.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others. This document contains information on products and technologies in development.