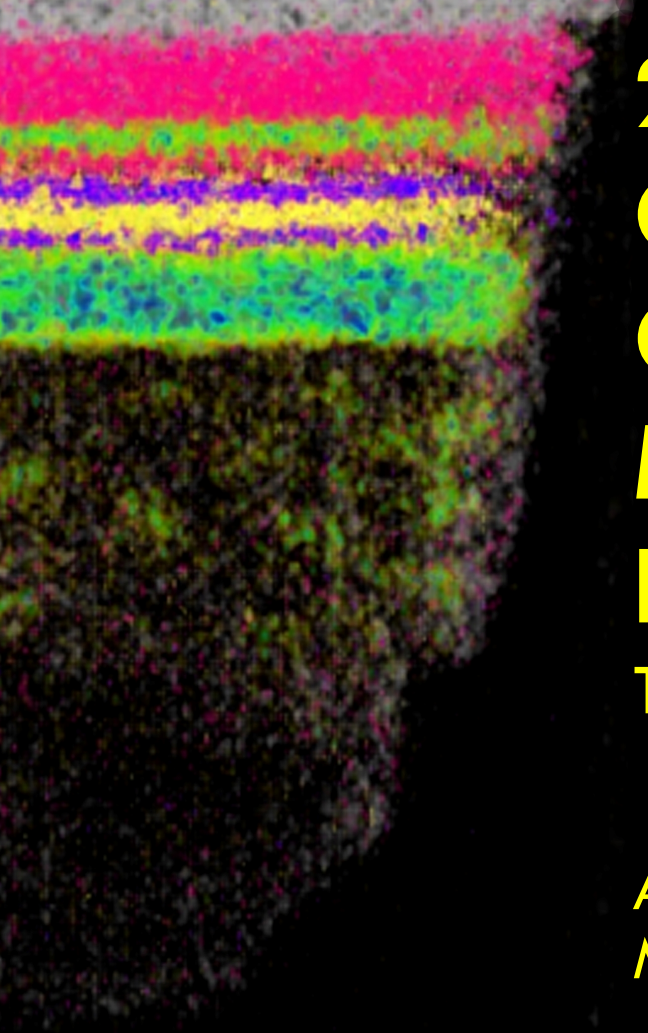


2019 INTERNATIONAL CONFERENCE ON FRONTIERS OF CHARACTERIZATION AND METROLOGY FOR NANOELECTRONICS

THE 12TH CONFERENCE IN THE SERIES!

APRIL 2-4, 2019
MONTEREY, CALIFORNIA

DAVID G. SEILER, FCMN CO-CHAIR
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, GAITHERSBURG, MD

ON BEHALF OF

ALL OUR CO-CHAIRS AND COMMITTEE MEMBERS **WELCOME**

FCMN COMMITTEE

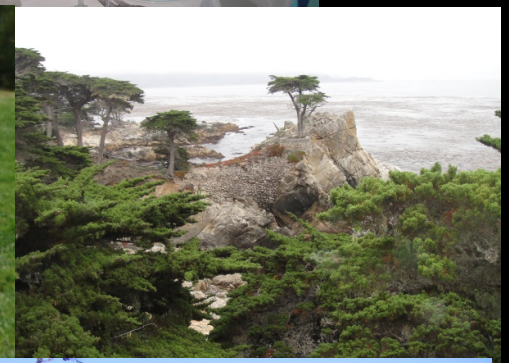
- **Co-Chairs**
  - David Seiler, NIST
  - Alain Diebold, CNSE, SUNY Polytechnic Institute
  - Zhiyong Ma, Intel
  - Paul van der Heide, IMEC
- **Committee Members**
  - Carols Beitia, CEA-Leti
  - Michael Current, Current Scientific
  - David Gundlach, NIST
  - Ajey Jacob, Global Foundries
  - Markus Kuhn, Intel
  - JJ Lee, TSMC
  - Alex Liddle, NIST
  - Ulrich Mantz, Zeiss
  - Bob McDonald, formerly of Intel (Treasurer)
  - Shinichi Ogawa,AIST
  - Erik Secula, NIST
  - Usha Varshney, NSF
  - Ehrenfried Zschech, Fraunhofer Institute for Ceramic Technologies and Systems

WHAT A DELIGHT TO BE IN MONTEREY AGAIN!













PARTNERS

- American Physical Society Physics
- American Vacuum Society
- Imec
- National Institute of Standards and Technology
- National Science Foundation

SPONSORS

- **Platinum** - Intel

- **Silver** - American Elements

2019 FCMN EXHIBITORS

- Active Layer Parametrics Inc.
- Bruker
- Cameca
- Covalent Metrology Services Inc.
- FRT of America
- Gatan Inc.
- NanoAndMore USA
- Nextron
- Park Systems
- Qzabre
- Semilab USA
- Sigray, Inc.

ORGANIZATIONS REPRESENTED (UPDATED MARCH 27)

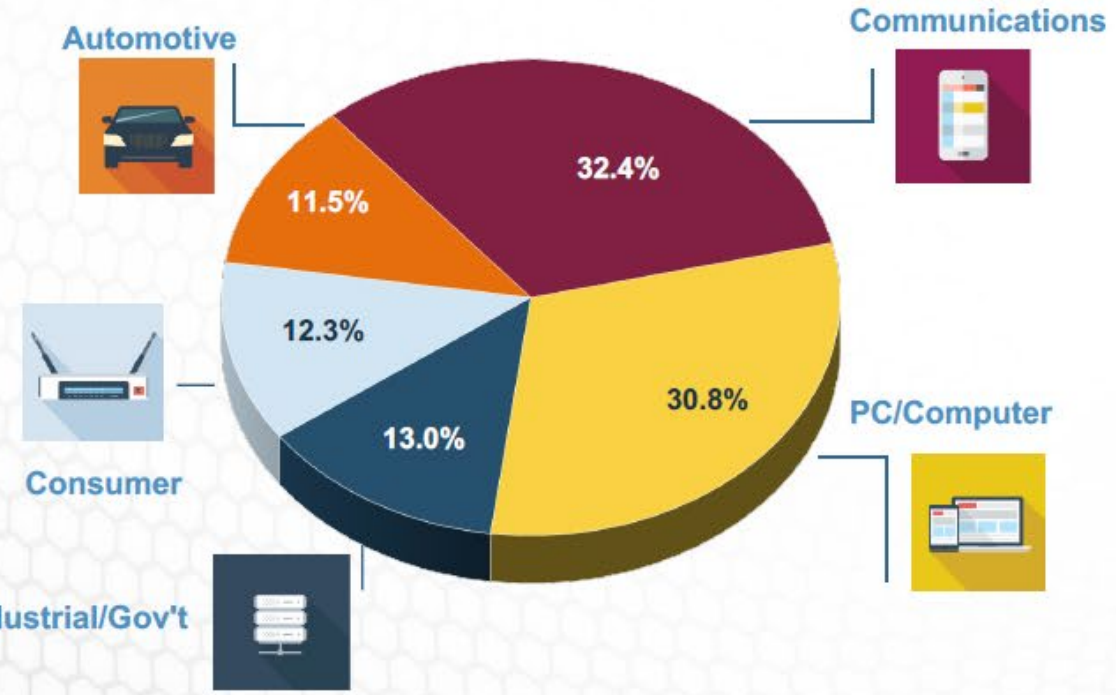
3M
Active Layer Parametrics
Advantest
AIST
AkzoNobel
Applied Materials
ASML
Attolight
Bruker
Cameca Instr
CAPRES
Carl Zeiss
CEA LETI
CoreTech Integrated
Covalent Metrology
Current Scientific
Cypress
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EAG Laboratories
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Extension Media/Solid State technologies
Fractilia, LLC
Fraunhofer Institute (IKTS)
FRT of America
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Global Foundries
Hamamatsu Corp.
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Hermes Microvision (an ASML Co.)
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IBM
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JEOL
KLA-Tencor
KMLabs
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Lam research
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Marian University
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Nanometrics
Nextron Corporation
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Nova Measuring Inst.
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Orsay Physics
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Samsung Electronics
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Seagate
Semilab
Sigray, Inc.
Sony
SUNY Polytechnic
Technical Univ. Denmark
Technosystem NT
Thermo Fisher Scientific
TNO
Tokyo Electron Limited
Toray Research Center
Toshiba Corp.
Univ of Cal Berkeley
VLSI Research
WaferMasters
Waviks

SECTION 2: GLOBAL MARKET

GLOBAL SEMICONDUCTOR SALES ARE DRIVEN BY PRODUCTS ULTIMATELY PURCHASED BY CONSUMERS

The vast majority of semiconductor demand is driven by products ultimately purchased by consumers – be they PC's for home use or communication devices such as smartphones. Increasingly, consumer demand is driven in emerging markets including those in Asia, Latin America, Eastern Europe and Africa.

2018 Total Global Semiconductor Market: $469 Billion
Percent of Semiconductor Demand, by End Use



Note: Gov't accounts for 1% of the Industrial/Gov't category, and military end-use is included in Gov't.
Sources: World Semiconductor Trade Statistics (WSTS).

SECTION 2: GLOBAL MARKET

GLOBAL SEMICONDUCTOR SALES ARE DIVERSIFIED BY TYPE OF PRODUCT SOLD

Semiconductor technology has rapidly evolved as the industry develops more advanced product and process technologies for applications in end-use industries. In recent years, the largest segments of the worldwide semiconductor industry have been memory, logic, analog, and MPU. In 2018, these products accounted for 80 percent of semiconductor industry sales.

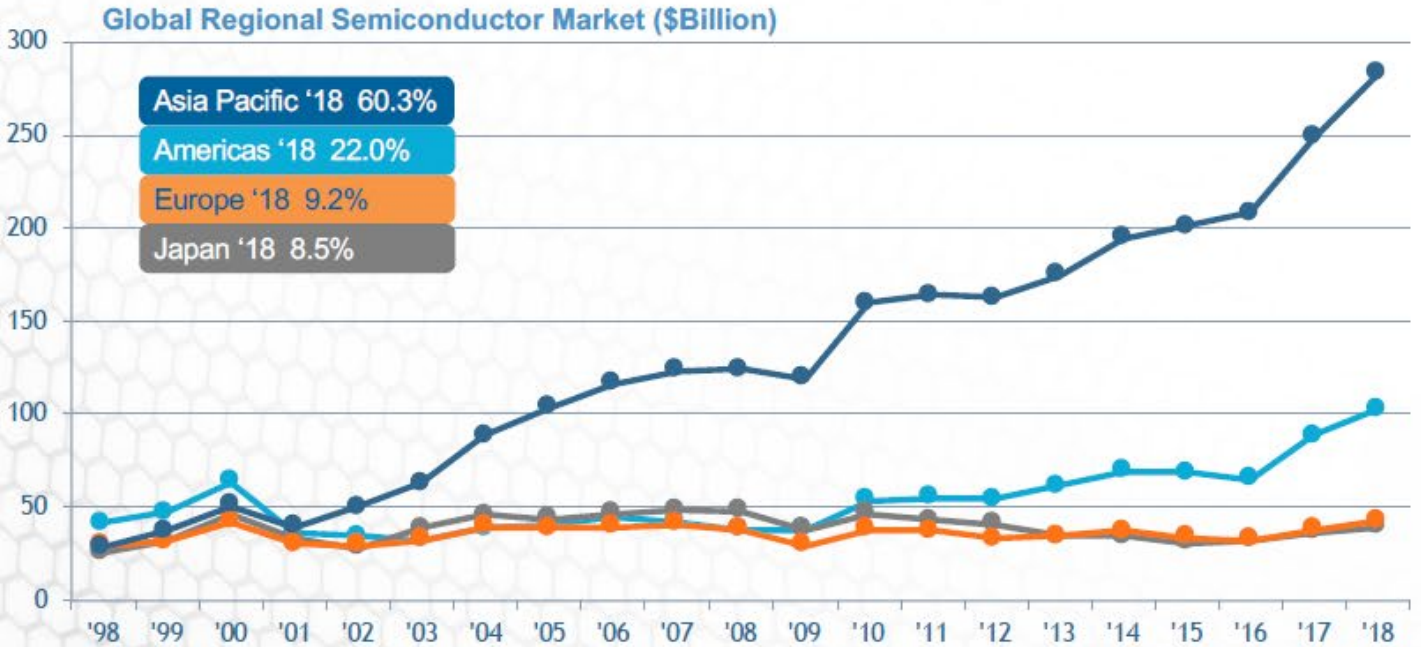


Source: World Semiconductor Trade Statistics (WSTS) and SIA Estimates.

SECTION 2: GLOBAL MARKET

TODAY, ASIA PACIFIC IS BY FAR THE LARGEST REGIONAL SEMICONDUCTOR MARKET

In 2001, the Asia Pacific market surpassed all other regional markets in sales, as electronic equipment production shifted to the region. It has multiplied in size since then - from $39.8 billion to over $282 billion in 2018. By far, the largest country market within the Asia Pacific region is China, which accounted for 56 percent of the Asia Pacific market and 34 percent of the total global market. This data reflects sales of semiconductors to electronic equipment makers only – final electronic products containing semiconductors are then shipped for consumption around the world.



Source: World Semiconductor Trade Statistics (WSTS) and SIA Estimates.

SNAPSHOT REMINDER FROM THE 2015 CONFERENCE

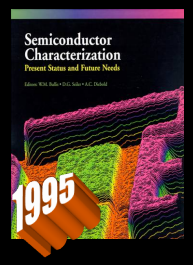
- **Pervasiveness of Metrology**
  - State of the art chip manufacturing technology nodes are approaching 2000 steps
  - Metrology and inspection steps consume a large share of these steps
    - ~50% of all steps and generally growing
  - ~25% to 33% of all the tools in the fab are metrology/defects toolsets
  - Significant fab floor space is needed for just metrology/inspection
  - CDSEM/film thickness toolsets are typically the most numerous tools in all fabs
- **Shrink puts pressure on Measurement Uncertainty**
  - Atomic level accuracy, matching and precision challenge
- **EUV Light Source and Masks**
  - New capabilities will be needed for mask defect inspection.
- **Difficult for a single metrology technique to measure all critical parameters sufficiently on 3D**
  - ***Hybrid Metrology*** emerging to fill-in gaps where individual techniques are lagging



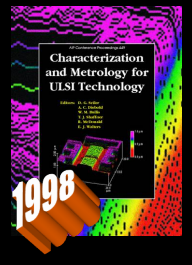
"Techno-Economics Pressure in Semiconductor Value Chain May Impact Consumers and Global Economy – What Is Our Solution?," Suresh Venkatesan, Global Foundries, 2015 FCMN

FOCAL POINT FOR FRONTIERS OF SEMICONDUCTOR NANOELECTRONICS METROLOGY

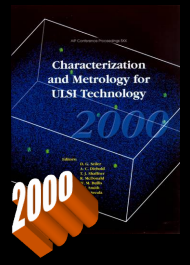
Proceedings Document Metrology Advances



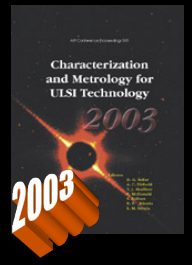
> 280 attendees



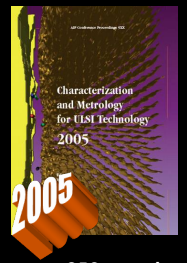
> 295 attendees



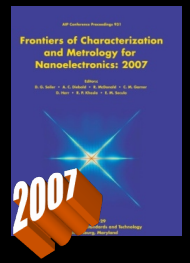
> 235 attendees



> 200 attendees



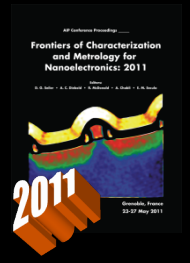
> 250 attendees



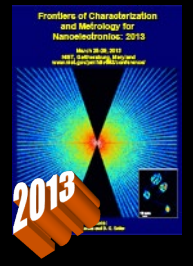
> 230 attendees



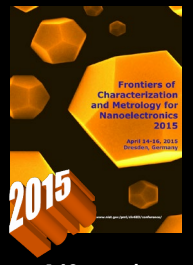
> 175 attendees



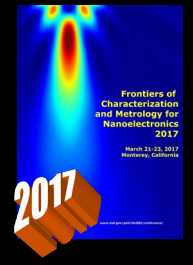
> 145 attendees



> 165 attendees



> 140 attendees



> 190 attendees

Some Keynote Speakers



Craig Barrett, formerly President, Intel



Mark Melliar-Smith, formerly President and CEO of SEMATECH



Dennis Buss, VP, Silicon Tech. Development, Texas Instruments



Bob Helms, formerly President and CEO of SEMATECH



Michael Polcari, President and CEO of SEMATECH



Mark Durcan, COO of Micron



Tze-Chiang (T.C.) Chen, IBM Fellow and VP, Science & Technology



Michel Brillouet, Senior Advisor, CEA-LETI



Mike Mayberry, VP, Intel



Klaus von Klitzing, Max-Planck-Institut FKF

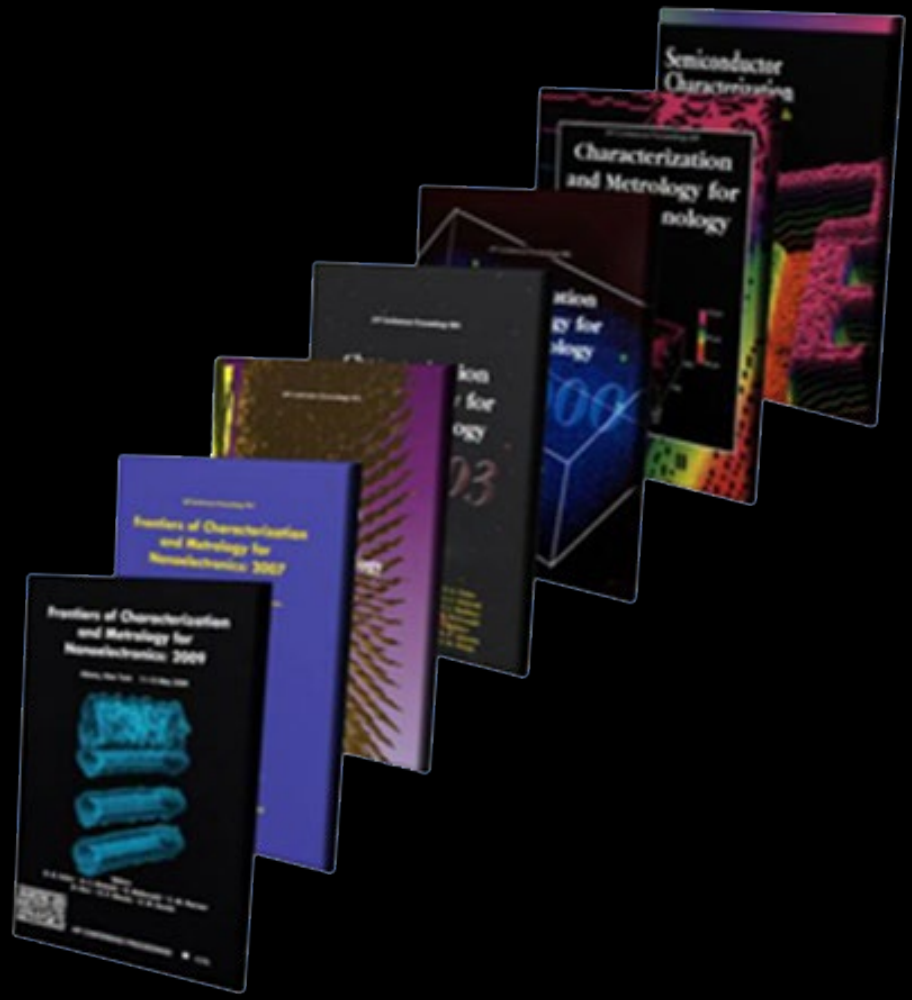


G. Dan Hutcheson, CEO VLSI Research Inc.

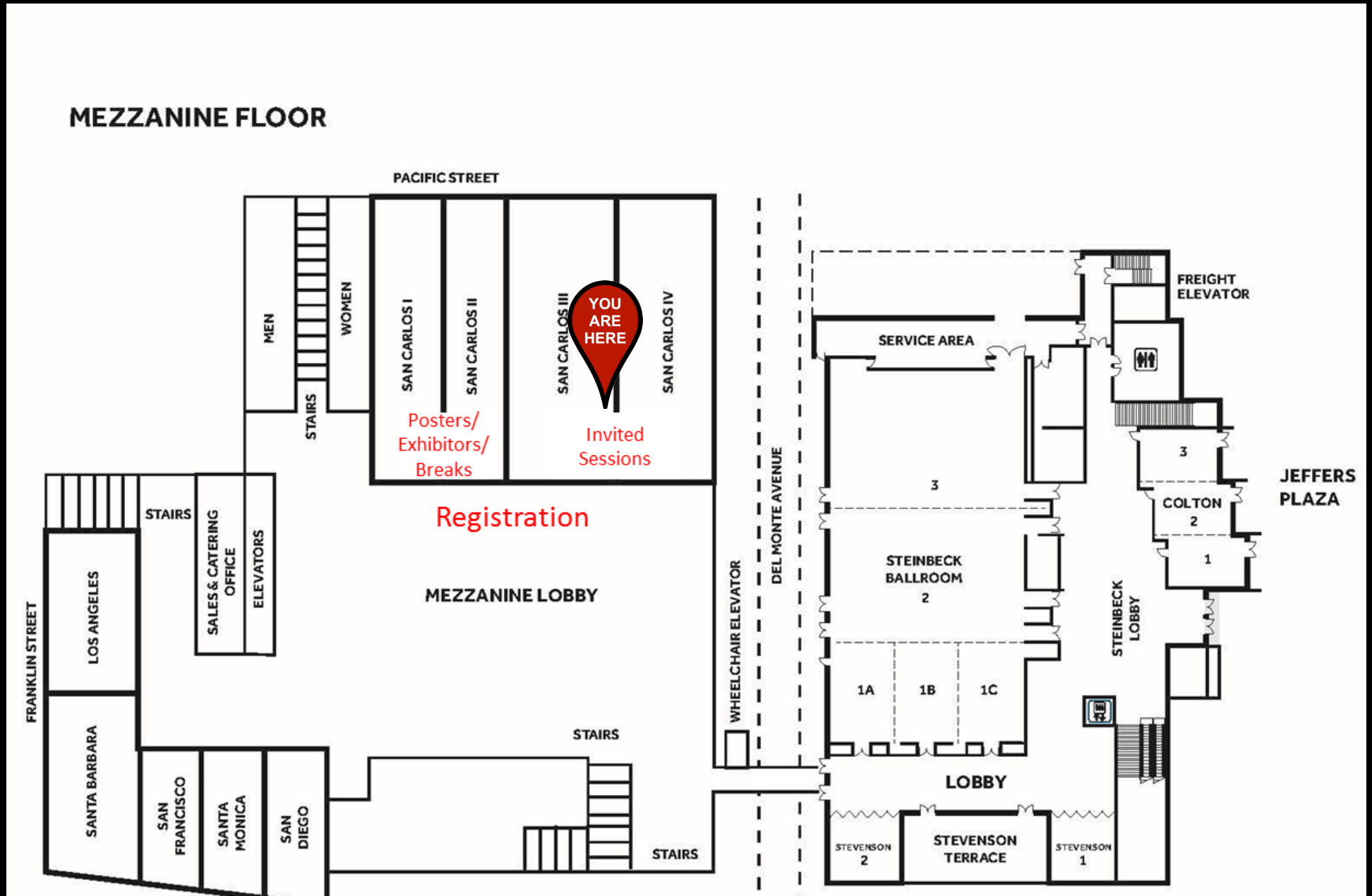
ARCHIVED PAPERS AND TALKS FREE ON-LINE!

- Proceedings papers from 1998-2009 are available free of charge, thanks to an agreement between the National Institute of Standards and Technology (NIST) and the American Institute of Physics (AIP)
- Presentation slides from most of the invited talks from 2000-2017 are available
- Most posters from the 2013-2017 conferences are available

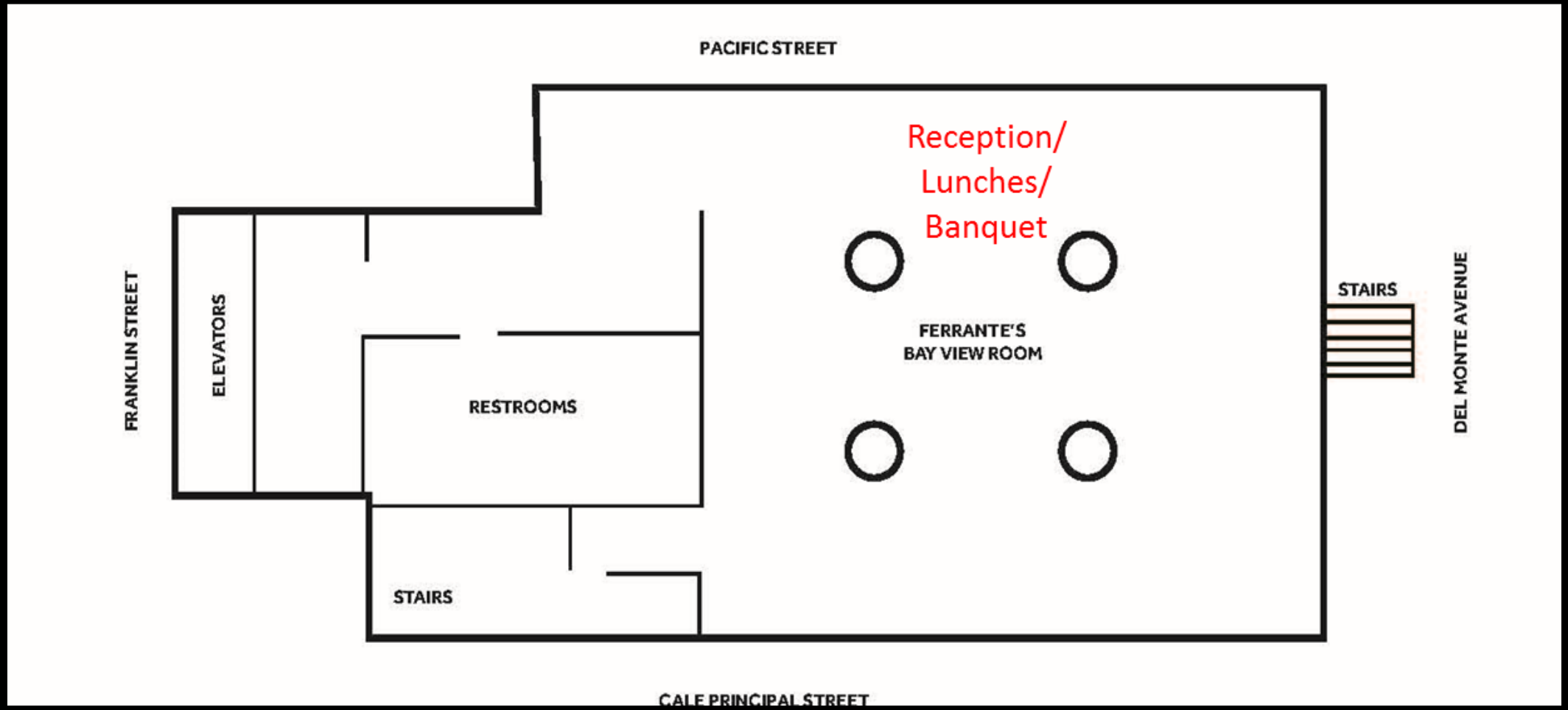
- www.nist.gov/pml/div683/conference/archives.cfm



CONFERENCE FACILITIES – 2ND FLOOR



CONFERENCE FACILITIES – 10TH FLOOR



CONFERENCE WIFI

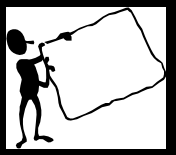


SPECIAL NOTES

- **Talks on-line**
  - We will ask each speaker for permission after the event.



- **Posters are up through out the conference**
  - Numbers are posted above each poster. Authors are responsible for displaying and removing (by the end of Thursday) their posters.



- **Lunch/Banquet Tickets**
  - **If there are any lunch/event tickets you will not use, please leave them at the registration table.**



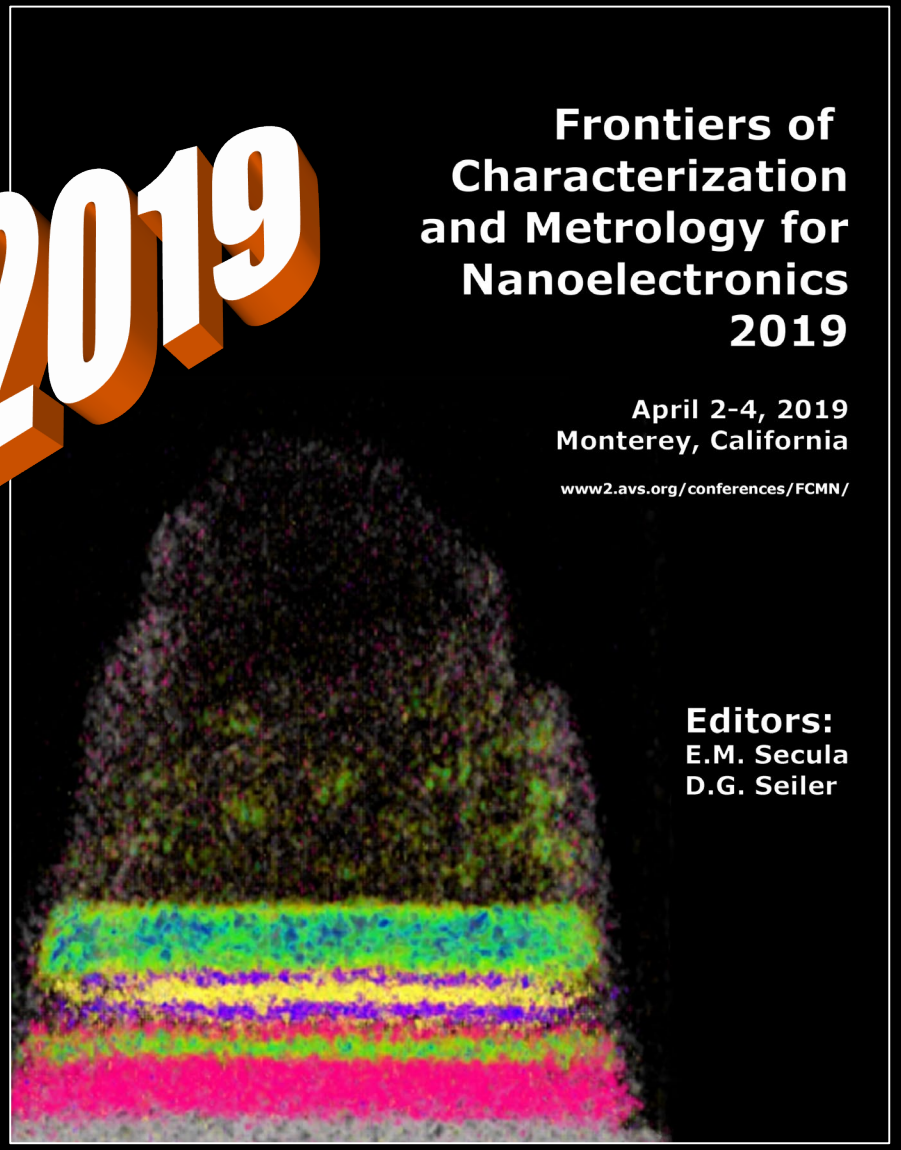
- **Silence Phones**



- **Emergency Exits**



- **Conference Survey**
  - **A survey will be sent out after the event. Your feedback is important and appreciated!**





Ian Young, Senior Fellow
Intel



Gurtej Sandhu, Senior Fellow
and Vice President, Micron



Carl Williams, Acting Director of
Physical Measurement Laboratory, NIST



Dan Hutcheson, CEO,
VLSI Research Inc.

SCHEDULE: TUESDAY MORNING, APRIL 2

Keynote (Session Chair: David Seiler, NIST)

- 9:00 AM Gurtej Sandhu, Senior Fellow and Vice President, Micron
  Frontiers in Memory Technology and Metrology Drivers
- 9:45 AM Ian Young, Senior Fellow, Intel
  Beyond CMOS Computing: Prospects and Best Bets
- 10:30 AM Coffee Break and Poster/Exhibit Viewing
- 11:00 AM Carl Williams, Acting Director, Physical Measurement Laboratory, NIST
  Impact of Quantum Information Science on the Future of Nanoelectronics

AI, Machine Learning and Hybrid Metrology (Session Chair: Markus Kuhn, Intel)

- 11:45 AM Phillip Leray, Imec
  Machine Learning Application for Metrology and Process Control
- 12:15 PM Lunch and Poster/Exhibit Viewing

SCHEDULE: AFTERNOON, TUESDAY, APRIL 2

AI, Machine Learning and Hybrid Metrology (Session Chair: Markus Kuhn, Intel)

- 1:45 PM Sergei Kalinin, Oakridge
  Deep Learning in Atomically Resolved Imaging: from Learning Physics to Atom by Atom Fabrication
- 2:15 PM Shay Wolfling, Nova
  AI and Machine Learning for Advanced Semiconductor Metrology and Process Control

Microscopy (Session Chair: Alain Diebold, CNSE, SUNY Polytechnic Institute)

- 2:45 PM Paul van der Heide, Imec
  What Does Near-line TEM Bring to the Table for the CMOS Manufacturing Industry
- 3:15 PM Coffee Break and Poster/Exhibit Viewing
- 3:45 PM Anne Delobbe, Tescan Orsay
  When Ion or Electron Channeling meets Crystal Orientation Mapping
- 4:15 PM Rudolf Tromp, IBM
  Low Energy Electron Resist Exposures
- 4:45 PM Wilfried Vandervorst, Imec
  Accurate and Precise Analysis of Nanoscale Semiconductor Devices with Atomprobe Tomography: a Physicist's Dream or an Analyst's Nightmare?
- 5:15 PM Poster Session (with Drinks and Hor d'oeuvres)
- 6:45 PM Banquet at Hotel

SCHEDULE: MORNING, WEDNESDAY, APRIL 3

Magnetics/Spintronics (Session Chair: Paul van der Heide, Imec)

- 8:30 AM Daniel Worledge, IBM
  Metrology for the Manufacturing Needs of MRAM
- 9:00 AM Kang Wang, UCLA
  Topological Quantum Computing: Metrology Needs
- 9:30 AM Yuji Otsuka, Toray Research Center
  Three-Dimensional Structural and Compositional Analysis of MTJ by STEM/EDX Tomography
- 10:00 AM Coffee Break and Poster/Exhibit Viewing

Metrology for Patterning (Session Chair: Alain Diebold, CNSE, SUNY Polytechnic Institute)

- 10:30 AM Alok Vaid, GLOBALFOUNDRIES
  Critical Dimension, Thickness, and Emerging Metrology Solutions for Three Dimensional Transistors and Multi-step Patterning
- 11:00 AM John Sturtevant, Mentor Graphics
  Interlayer Edge Placement Hotspots: Quantifying and Expanding Combined CD/Overlay Process Window
- 11:30 AM Andy Antonelli, Nanometrics
  Optical Critical Dimension Metrology in Memory and Logic
- 12:00 PM Arie den Boef, ASML
  Holistic Metrology Approaches for Improved Device Overlay and Edge Placement Error
- 12:30 PM Lunch and Poster/Exhibit Viewing

SCHEDULE: AFTERNOON, WEDNESDAY, APRIL 3

7-10 nm Metrology and Defect Inspection (Session Chair: Tuyen Tran, Intel)

- 2:00 PM Yalin Xiong, KLA-Tencor
  Broadband Optical Inspection Technology for Emerging Process Inflections
- 2:30 PM Ofer Adan, AMAT
  Extending Electron Beam Technology Further/Deeper into the Metrology Space for 7nm or Below Process Development and Manufacturing
- 3:00 PM Oliver Patterson, HMI
  Advancement on Massively Parallel Electron Beam Inspection Technology for 7nm or Below Process Development and Manufacturing
- 3:30 PM Coffee Break and Poster/Exhibit Viewing

Nanoscale and Interfacial Compositional Characterization and Metrology (Session Chair: Markus Kuhn, Intel)

- 4:00 PM Wenbing Yun, Sigray
  Micro X-ray Fluorescence for Integrated Dopants and Thin Film Analysis
- 4:30 PM Ying Zhou, Intel
  Integrated Process Learnings with Hybrid Characterization
- 5:00 PM Sung Park, Molecular Vista
  PIFM Nanoscale Chemical Probe for Novel Patterning Applications
- 5:30 PM Poster Session (with Drinks and Hor d'oeuvres)

SCHEDULE: MORNING, THURSDAY, APRIL 4

Metrology for Advanced Packaging (Session Chair: Ehrenfried Zschech, Fraunhofer IKTS Dresden)

- 8:30 AM Christian Schmidt, NVIDIA
  Existing and Future Characterization Needs
- 9:00 AM Ehrenfried Zschech, Fraunhofer IKTS Dresden
  Really Nondestructive High-resolution X-ray Tomography for Advanced Packaging Applications
- 9:30 AM Ravikiran Attota, NIST
  Nondestructive and Economical Dimensional Metrology of Deep Structures
- 10:00 AM Coffee Break and Poster/Exhibit Viewing

Emerging Characterization and Metrology (Session Chairs: Usha Varsney, NSF, and Paul van der Heide, Imec)

- 10:30 AM Brennan Peterson, KMLabs
  Current Status and Future Possibilities of HHG Sources for Characterization/Metrology in the Semiconductor Industry
- 11:00 AM David Larson, Ametek
  Atom Probe Tomography: Toward Improved Productivity and Correlative Analysis in the Semiconductor Industry
- 11:30 AM Thomas Mueller, Bruker
  Current Status and Future Prospects for SPM for Supporting the Semiconductor Industry
- 12:00 PM Alexis Franquet, Imec
  Hybrid SIMS: How the Orbitrap Mass Analyzer Can Improve the Self-Focusing SIMS Concept for Advanced Semiconductor Structures
- 12:30 PM Lunch and Poster/Exhibit Viewing

SCHEDULE: AFTERNOON, THURSDAY, APRIL 4

General (Session Chair: Alain Diebold, CNSE, SUNY Polytechnic Institute)

- 2:00 PM George Orji, NIST
  Metrology Requirements for Next Generation of Semiconductor Devices

TCAD (Session Chair: Michael Current, Current Scientific)

- 2:30 PM Valeriy Sukharev, Siemens/Mentor Graphics
  Electromigration Power Grid Checking – Novel Design and Reliability Metrology

Metrology for Silicon Photonics and Sensors (Session Chair: Alex Liddle, NIST)

- 3:00 PM Vladimir Aksyuk, NIST
  Scanning Probe Technology to Make Local, Non-Contact Measurements of Photonic Circuits
- 3:30 PM G. Dan Hutcheson, VLSI Research, Inc.
  Moore's Law in a Neuromorphic World
- 4:00 PM Conference End

FCMN LOCATIONS

- 1995, 1998, 2000, 2007, 2013: NIST, Gaithersburg, MD
- 2003: J.J. Pickle Research Campus, Univ. of Texas, Austin, TX
- 2005: Univ. of Texas at Dallas, Richardson, TX
- 2009: College of Nanoscale Science and Engineering, SUNY, Albany, NY
- 2011: MINATEC Campus, Grenoble, France (CEA-Leti)
- 2015: Dresden, Germany (Fraunhofer)
- 2017, 2019: Monterey, California