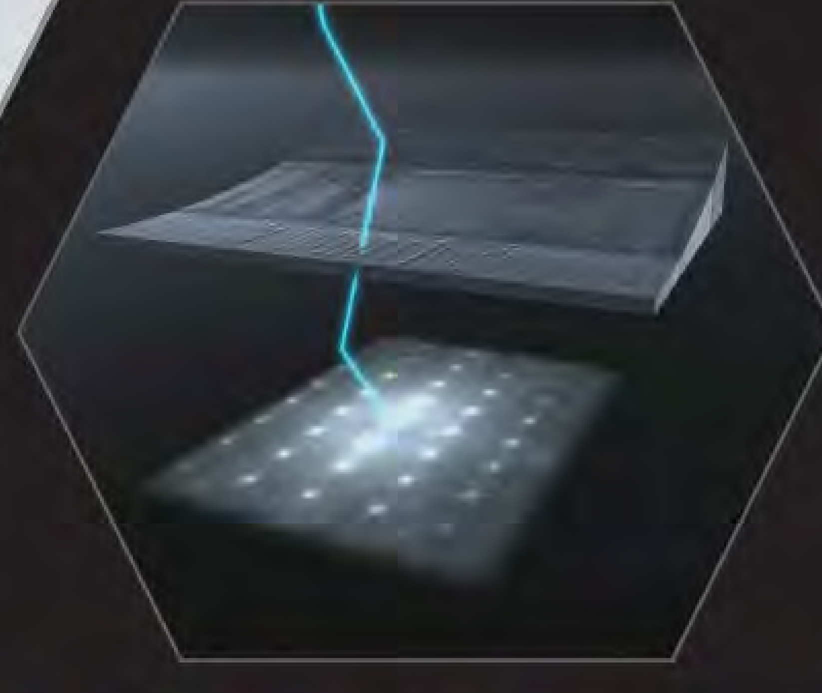
Frontiers of Characterization and Metrology for Nanoelectronics 2026

March 16-19, 2026
Monterey, California

fcmn2026.avs.org



Committee Co-Chairs

J. Alexander Liddle
Canon Nanotechnologies, Inc.

Alain Diebold
University at Albany

Markus Kuhn
Rigaku

Jin Zhang
Lam Research

Paul van der Heide
imec

Committee Members

- Ofer Adan, Applied Materials
- Jean-Paul Barnes, CEA-Leti
- Alan Brodie, KLA-Tencor
- Steve Consiglio, TEL Technology Center
- Michael Current, Current Scientific
- Troy Morrison, Thermo Fisher
- Ye Feng, Intel
- Eugen Foca, Zeiss
- Christina Hacker, NIST
- Ajey Jacob, University of Southern California
- Eunpa Kim, Samsung
- Shunsuke Koshihara, Hitachi High-Tech Corporation
- Byoungho Lee, Hitachi High-Tech Corporation
- Baohua Niu, Intel
- Shinichi Ogawa, AIST
- David Seiler
- Ehrenfried Zschech, BTU Cottbus

Cover Caption: Dedicated beam precession coils in the Tescan TENSOR analytical STEM microscope (left) facilitate acquisition of high quality 4D-STEM datasets (right) which provide reliable quantitative phase-orientation analysis of polymorphic materials (bottom), such as HZO thin films used in many semiconductor devices.

2026 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Welcome to the 2026 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN). This conference brings together scientists and engineers from around the world who are engaged in advancing the characterization technologies essential to nanoelectronic materials and device research, development, integration, and manufacturing.

FCMN embraces the full breadth of characterization and metrology approaches, including chemical, physical, electrical, magnetic, optical, *in situ*, and real-time control and monitoring techniques. As the semiconductor industry continues to evolve at a rapid pace, the conference highlights key challenges and presents critical reviews of state-of-the-art materials and structural characterization as well as nearline and inline metrology methods. Topics span hardware innovations, data analysis, and the growing impact of artificial intelligence and machine learning, reflecting the industry's push toward ever-smaller dimensions alongside increasing device and system diversity.

We hope that the invited presentations, contributed posters, and informal discussions will stimulate practical insights, inspire breakthrough ideas in research and development, and foster meaningful connections among colleagues, enabling new collaborations and global interactions.

We are delighted to welcome Robert Chau (AMD), Gowri Kamarthy (Lam Research), and Dan Hutcheson (TechInsights) as keynote speakers for the conference. In addition, more than thirty invited talks will provide compelling overviews across the technical sessions. Poster presentations will complement these sessions by showcasing the latest advances in nanoelectronics metrology.

The 2026 FCMN marks the 15th installment of this biennial conference series dedicated to metrology for the semiconductor industry. The conference continues its tradition of emphasizing cutting-edge developments in characterization and metrology that are shaping the future of the nanoelectronics revolution. Proceedings from many previous conferences were published by the American Institute of Physics and, along with numerous archived presentation slides, are freely available online at www.nist.gov/pml/fcmn-publications-and-talks.

For the fifth consecutive conference, we are pleased to host FCMN in Monterey, California. Monterey is a scenic coastal city, rising from the pristine waters of Monterey Bay to pine-forested hillsides with sweeping ocean views. We hope you enjoy both the conference and your time in this beautiful setting.

It is our sincere hope that you find the 2026 FCMN both stimulating and rewarding!

With best wishes from the Committee Co-Chairs,

J. Alexander Liddle, Canon Nanotechnologies;

Alain Diebold, University at Albany;

Markus Kuhn, Rigaku

Jin Zhang, Lam Research; and

Paul van der Heide, imec

Purpose and Goals

The FCMN brings together scientists and engineers interested in all aspects of the characterization technology needed for nanoelectronic materials and device research, development, integration, and manufacturing. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed in the semiconductor industry for advancing silicon nanoelectronics and beyond.

Contributed Posters

One of the major emphases of this conference is on the contributed posters. These extended poster abstracts, refereed by the committee, represent significant contributions to the frontier of state-of-the-art materials and device characterization.

Poster authors are responsible for setting up their displays, being present for the poster sessions on Tuesday and Wednesday afternoon, and removing their displays by the end of the conference on Thursday.

Poster Sessions

The poster sessions with complimentary snacks and beverages are scheduled for 5:30 PM on Tuesday and 4:30 PM on Wednesday in San Carlos I and II at the Monterey Marriott.

Banquet

A dinner banquet will be held on Tuesday, March 17th, at 7:00 PM in the Ferrante's Bay View Room on the 10th floor of the Monterey Marriott.

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Solutions for Semiconductor Inspection and Analysis

Application of TEM-Based CD Measurement in Advanced Semiconductor Processes - TEM-LINKAGE

Specimen Transfer Workflow using the Double Tilt Cartridge

200kV S/TEM
JEM-ACE200F

FIB-SEM
JIB-PS500i

FIB-SEM holder

TEM specimen holder

Double tilt holder

Download the Semiconductor Note

TEM image

20 nm

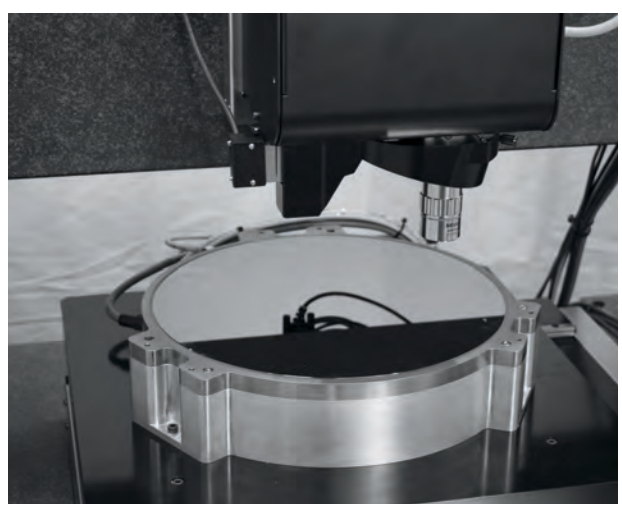
HAADF-STEM image

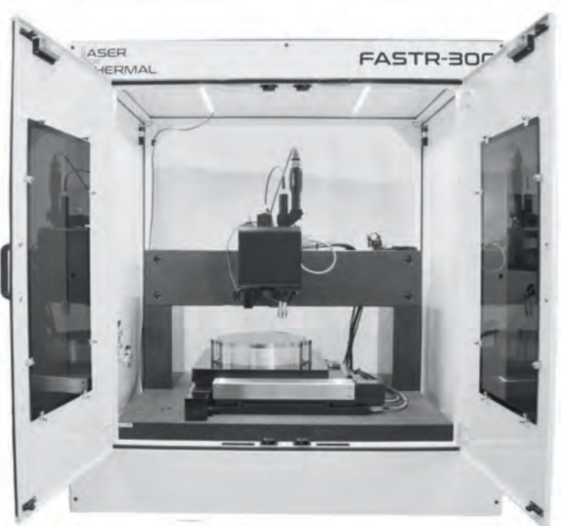
10 nm

The figures above show a HAADF-STEM image of a Fin Field-Effect Transistor (FinFET) and a TEM image of a flash memory, both acquired using the JEM-ACE200F. Multi Image Tool developed by SYSTEM IN FRONTIER INC. is used for the measurement, enabling operators to create customized measurement recipes.

FASTR 300

Thermal Metrology Across 300 mm Wafers





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18.5 nm depth

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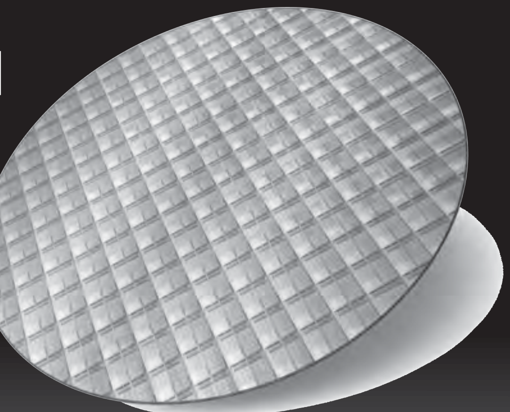
Molecular Vista

UNLOCK PRECISION IN SEMICONDUCTOR SURFACE ANALYSIS



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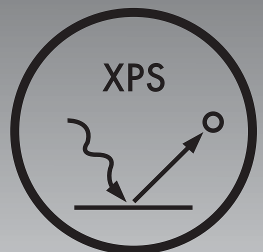
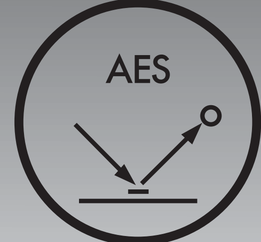


X-ray Photoelectron Spectroscopy (XPS)

Quantitative elemental and chemical state analysis for ultra-thin films and surfaces.



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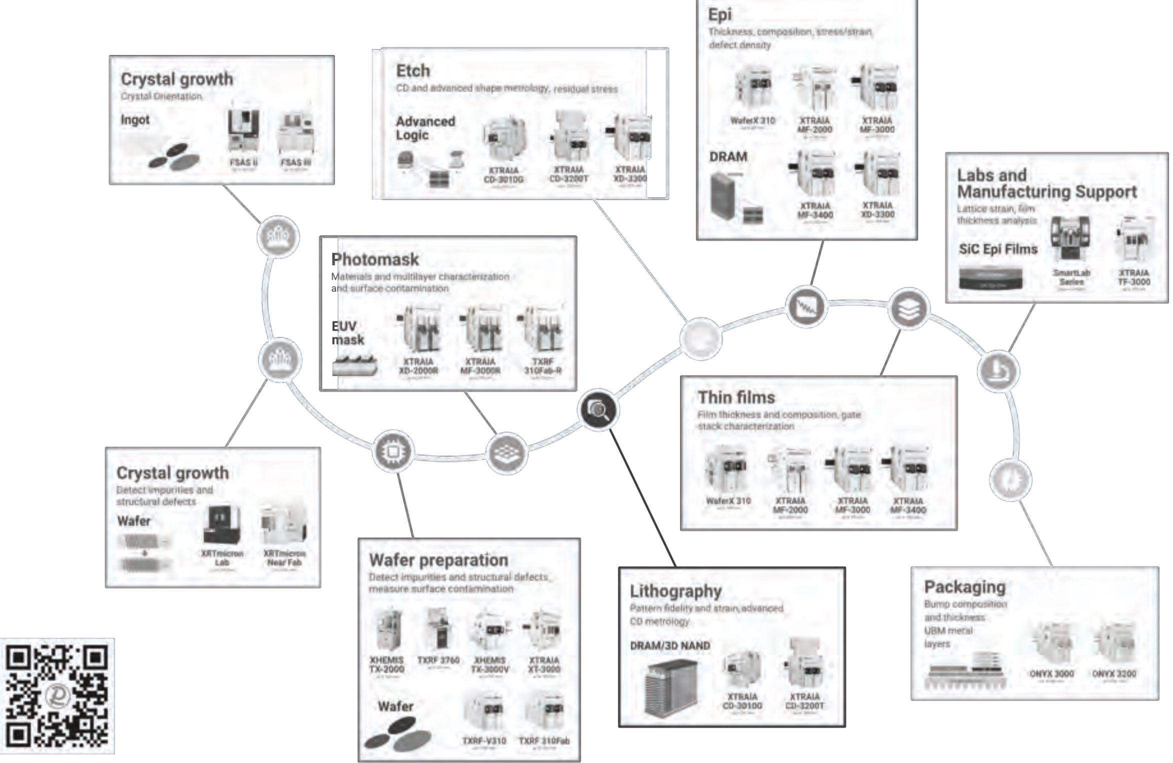
Advancing Characterization From Lab to Fab



Metrology Across the Nanoelectronics Value Chain

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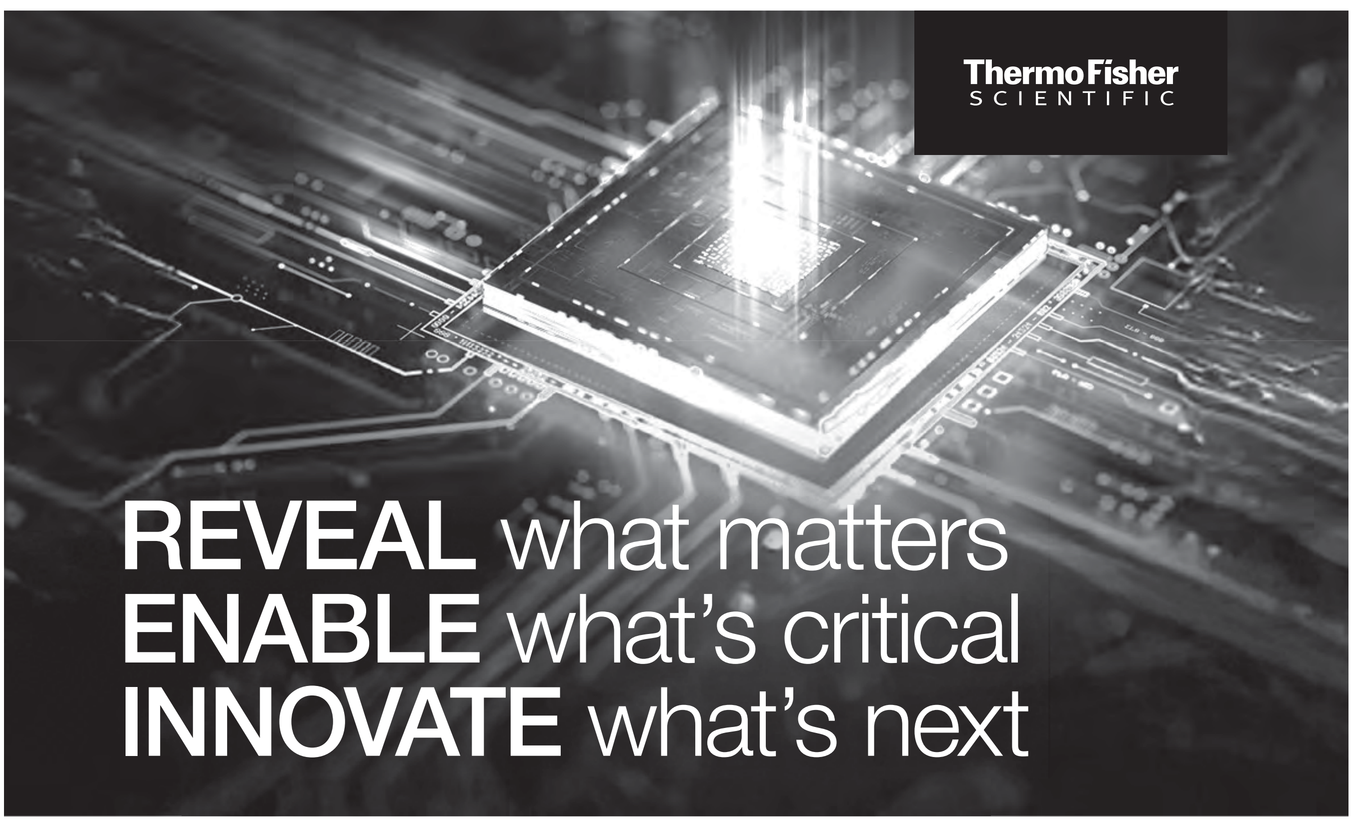

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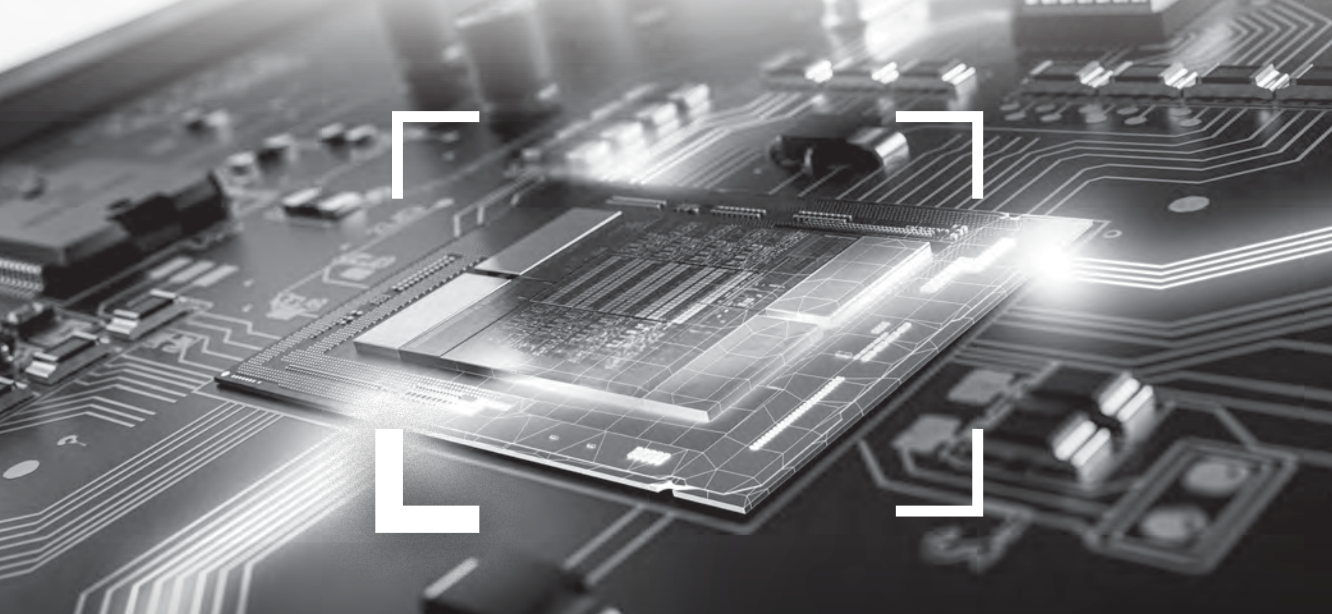

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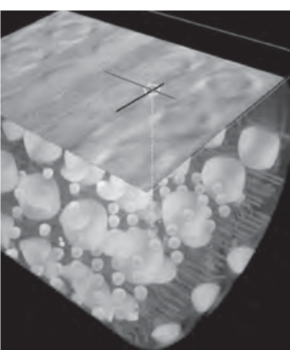
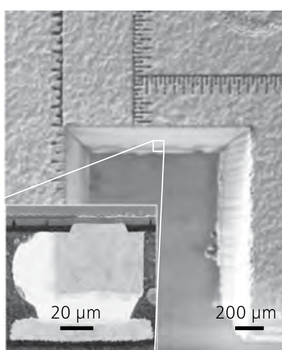


Submicron 3D visualization of package interconnects and defects

ZEISS Crossbeam LaserFIB
From macro to nano in femtoseconds



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ZEISS GeminiSEM Field-emission SEM
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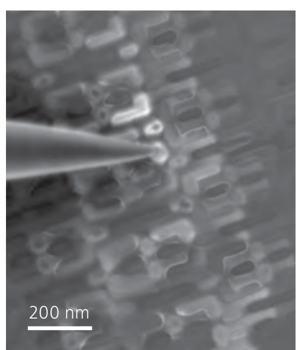

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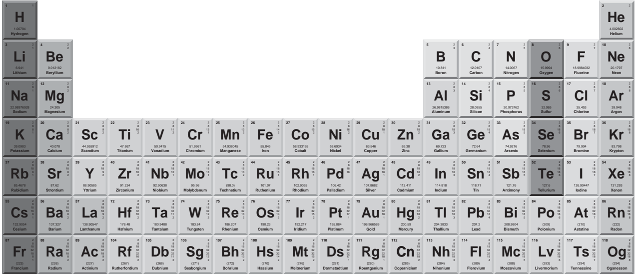

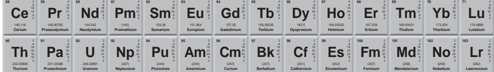

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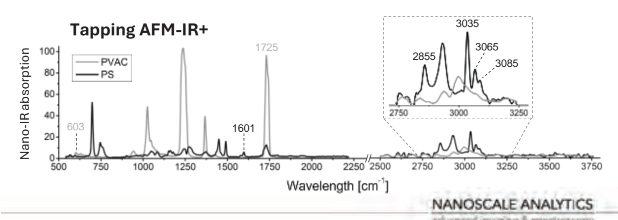

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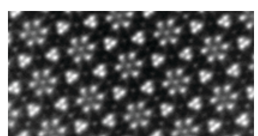

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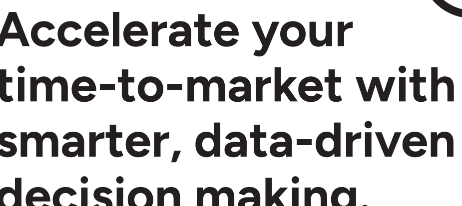

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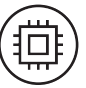

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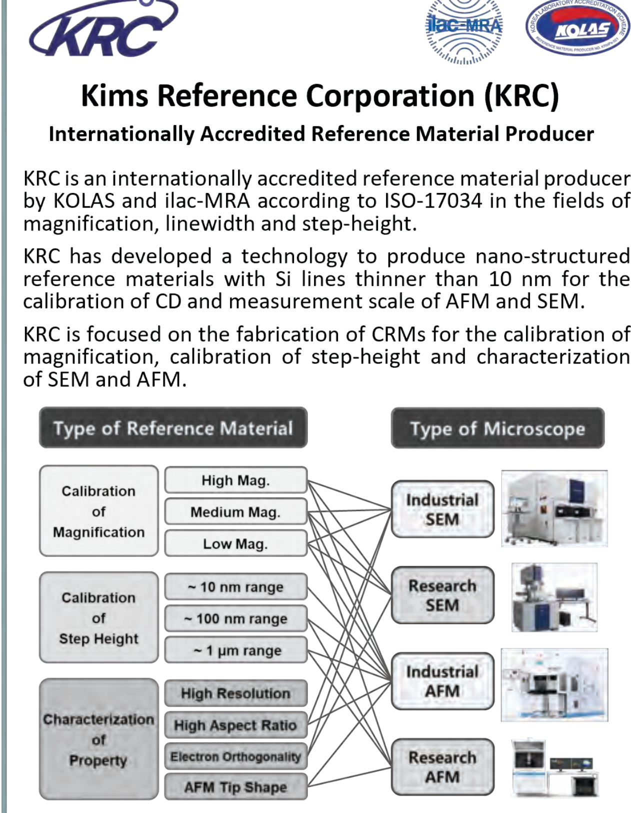

Program at a Glance

	Morning	AM Sessions	PM Sessions	Evening
Tuesday March 17th	**7:00** Registration / Attendee Check-in	**9:00** Conference Opening **9:15** Plenary I **10:00** Industry Trends	**1:30** Materials Characterization I **3:00** Materials Characterization II **5:00** Inline Metrologies I	**5:30** Poster Session **7:00** Banquet
Wednesday March 18th	**7:45** Registration / Attendee Check-in	**8:30** Inline Metrologies I **9:30** Inline Metrologies II	**1:00** Automation **3:00** Virtual Metrology & Correlative Approaches	**4:30** Poster Session
Thursday March 19th	**8:00** Registration / Attendee Check-in	**8:30** Plenary II **9:15 AM** Advanced Packaging **11:15** EUV and Beyond EUV	**1:30** Novel methods to support novel CMOS memory and logic R&D **1:30** Novel methods to support beyond CMOS device R&D **4:30** Plenary III	

Monday, March 16

Tutorial Session I: Metrology Techniques

2:00-4:00 PM

Presenters: Alain Diebold, University of Albany; Paul van der Heide, imec

Tutorial Session II: Advanced Packaging

2:00-4:00 PM

Ofer Adan, Applied Materials

Tutorial Session III: XPS

4:30-6:30 PM

Paul van der Heide, imec

Tutorial Session IV: TEM/STEM

4:30-6:30 PM

Michael Gribelyuk, IBM

Reception and Registration

7:00 – 9:00 PM

Monterey Marriott

Tuesday, March 17

Registration:

7:00 AM – 8:30 AM

Conference Opening

9:00 AM

J. Alexander Liddle (Canon Nanotechnologies) Conference Co-Chair

P1. Plenary I

Session Chairs: J. Alexander Liddle (Canon Nanotechnologies) and Markus Kuhn (Rigaku)

9:15 AM 29

Robert Chau (AMD) *Semiconductor and Packaging Innovations for Continued Compute and AI Advancement in the Next Decade*

10:00 AM

Coffee Break and Poster/Exhibit Viewing

2. Industry Trends

Session Chairs: Ofer Adan (Applied Materials) and Jaehyun Kim (SK Hynix)

10:30 AM..30
Todd Stievater (NRL) *Passive Photonic Integrated Circuit Metrology*

11:00 AM..32
Philip Wong (Stanford) *Beyond the Exit of the Device Miniaturization Tunnel*

11:30 AM..35
Alain Diebold (CNSE, U.Albany) *Mueller Matrix Spectroscopic Ellipsometry based Scatterometry of Nanosheet Structures for GAA Transistors using a Hybrid Metrology Approach*

12:00 PM – 1:30 PM
Lunch and Poster/Exhibit Viewing

3. Materials Characterization I

Session Chairs: Paul van der Heide (imec) and Eunpa Kim (Samsung)

1:30 PM..38
Andrei Kolmakov (NIST) *Plasma XPS: a New Operando Metrology for Semiconductor Process Development and Control*

2:00 PM..42
Koichiro Saga (SONY) *Influence of metallic contamination on CMOS image sensors and analytical techniques*

2:30 PM..45
Cassandra Philips (Bruker) *Novel Applications of Nanoscale IR Spectroscopy Coupled with AFM for Semiconductor Metrology*

3:00 PM
Coffee Break and Poster/Exhibit Viewing

4. Materials Characterization II

Session Chairs: Paul van der Heide (imec) and Troy Morrison (ThermoFisher)

3:30 PM..48
Alex Merkulov (imec) *Improving the carbon detection limit with Secondary Ion Mass Spectrometry (SIMS)*

4:00 PM..49
Umberto Celano (ASU) *Who Needs Electrical Back-Contacts After All?*

4:30 PM..53
Daniel Němeček (Tescan) *Advances in 4D-STEM for Applications in Phase Analysis and Strain Engineering*

5. Inline Metrologies I

Session Chairs: Alain Diebold (University of Albany) and Jin Zhang (Lam Research)

5:00 PM...56
Bryan Barnes (NIST) *Harnessing the extreme ultraviolet for critical dimension metrology*

Poster Session

5:30 PM
Banquet at Hotel

Wednesday, March 18

Registration:

7:45 – 8:30 AM

6. Inline Metrologies I

Session Chairs: Alain Diebold (University of Albany) and Jin Zhang (Lam Research)

8:30 AM 59
Patrick Naulleau (EUV Tech) *Hybrid Metrology for Hot Spot Prediction in Post-Etch Patterning*

9:00 AM 60
Jin Zhang (Lam Research) *Advancing Metrology for High Aspect Ratio Structures: Lam Research's Journey with CDSAXS*

7. Inline Metrologies II

Session Chairs: Alain Diebold (University of Albany) and Steve Consiglio (TEL)

9:30 AM 61
Sarah Okada (Nova) *Impact Assessment of In-line SIMS Utilization on Logic Device Performance*

10:00 AM
Coffee Break and Poster/Exhibit Viewing

10:30 AM...62
Andy Humphris (Infinitesima) *High Speed AFM as an Enabling Technology for Next Generation Semiconductor Devices*

11:00 AM...63
Kengo Goto (Hitachi) *Multibeam inspection tool development for detecting below 10 nm physical defects*

11:30 – 1:00 PM
Lunch and Poster/Exhibit Viewing

8. Automation

Session Chairs: Byoungho Lee (Hitachi High-Tech Corporation) and Ofer Adan (Applied Materials)

1:00 PM..66
Sanjay Yedur (Thermo Fisher Scientific) *Workflow Automation For High Volume TEM Data Production*

1:30 PM..69
Ehrenfried Zschech (BTU Cottbus) *Combined Acoustic and X-Ray Microscopy for Advanced Packaging Metrology and Defect Inspection*

2:00 PM..72
YoungSeok Kim (Samsung) *Spectrum-to-structure Hybrid Metrology: SEM Referenced Model Guided M/L of 3D Profiling from SE and Xray Signals*

2:30 PM
Coffee Break and Poster/Exhibit Viewing

9. Virtual Metrology & Correlative Approaches

Session Chairs: Christina Hacker (NIST) and Eugen Foca (Zeiss)

3:00 PM..73
Maxime Besacier (Laboratoire des Technologies de la Microélectronique) *Hybrid Metrology Assisted by Machine Learning at Nanometer Scale*

3:30 PM..76
Arvinder Sandhu (ASU) *A Compact X-ray Light Source for Characterization and Metrology*

4:00 PM..78
Meghali Chopra (Sandbox Semiconductor) *Hybrid Metrology for Hot Spot Prediction in Post-Etch Patterning*

4:30 – 6:00 PM
Poster Session (with Drinks and Hors d'oeuvres)

Thursday, March 19

Registration:

7:00 AM – 8:30 AM

P2. Plenary II

Session Chairs: J. Alexander Liddle (Canon Nanotechnologies) and Jin Zhang (Lam Research)

8:30 AM 81
Gowri Kamarthy (CVP, Lam Research) *Frontiers in Semiconductor Devices with 3D Integrations – Opportunities for process and metrology*

10. Advanced Packaging

Session Chairs: Baohua Niu (Intel) and Alan Brodie (KLA)

9:15 AM 82

April Shuyan Zhang (TEL) *Addressing Metrology Challenges in Hybrid Bonding: An Overview of Tokyo Electron's X-ray Imaging Program Focused on Overlay and Defects*

9:45 AM 85

Julius Hallstedt (Excillum) *From Wafer to Package: High Performance X-Ray Sources Driving Semiconductor Progress*

10:15 AM

Coffee Break and Poster/Exhibit Viewing

10:45 AM..88

Aviram Tam (Applied Materials) TBD

11. EUV and Beyond EUV

Session Chairs: Ye Feng (Intel) and Shinichi Ogawa (AIST)

11:15 AM..89

Takeo Watanabe (Hyogo University) *Metrology for EUV Lithography at NewSUBARU Synchrotron Light Facility*

11:45 AM..91

Doug Resnick (Canon Nanotechnologies) *Metrology Requirements for Nanoimprint Lithography*

12:15 PM

Lunch and Poster/Exhibit Viewing

12. Novel methods to support novel CMOS memory and logic R&D

Session Chairs: Jin Zhang (Lam Research) and Ehrenfried Zscech (Malab)

1:30 PM..94

John Gaskins (Laser Thermal) *Cross-Validated Anisotropic Thermal Conductivity Metrology of AlN Films*

2:00 PM..97

Jim Chambers (Nvidia) *Failure Analysis in the AI Era: Ensuring Reliability at Scale*

2:30 PM..98

Lars Mester (Attocube) *Nano-optical imaging and spectroscopy of semicon materials – an s-SNOM & nano-IR overview*

3:00 PM

Coffee Break

13. Novel methods to support beyond CMOS device R&D

Session Chairs: Paul van der Heide (imec) and Jean-Paul Barnes (CEA-Leti)

3:30 PM..101
Mathieu Munsch (Qnami) *Nanoscale Quantum Sensing for Spintronics and Electronics*

4:00 PM..103
Stuart Parkin (PTB) *TBD*

P3. Plenary III

Session Chairs: J. Alexander Liddle (Canon Nanotechnologies) and Alain Diebold

4:30 PM..104
Dan Hutcheson (TechInsights) *Moore's Law is dead. Long live Moore's Law*

5:15 PM
Conference End

Poster Presentations

001, Metrology and Inspection for Advanced DRAM Production Using Second-Harmonic Generation 105
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Semiconductor and Packaging Innovations for Continued Compute and AI Advancement in the Next Decade

Robert Chau

AMD

Going forward continued improvement in AI DATA CENTER and EDGE performance and energy efficiency will rely on holistic innovation and co-optimization across the full stack of technologies from materials, devices, process modules, advanced packaging, heterogeneous integration, circuit design, architectures, algorithms, software, and applications. Advancement will require not only material, device and interconnect technology innovations but also DTCO (design-technology co-optimization) as well as STCO (system-technology co-optimization). This presentation will focus on the semiconductor technology and 3D heterogeneous systems integration aspects of the technology stack for continued Compute and AI advancement in the next decade, plus the integration of advanced characterization and metrology methods coupled with AI and machine learning in the early R&D phase to accelerate innovations progress.

Passive Photonic Integrated Circuit Metrology

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1 Introduction

We describe a new, high-precision technique to extract key parameters for accurate modeling and tracking of photonic integrated circuit (PIC) components and devices. The method is based on the measurement of effective index obtained via broadband waveguide Mach-Zehnder interference spectra[1], followed by inverse analysis based on nonlinear least-squares fitting. Unlike ellipsometry, our waveguide Mach-Zehnder interferometry (MZI) technique is carried out using waveguides co-fabricated with all other PIC components, such that all process steps are captured in the measured spectra. Unlike electron microscopy, waveguide interferometry is non-destructive and requires no additional processing. The inverse analysis requires the automated use of a mode solver, since no analytic effective index solution exists for a rectangular or trapeziodal waveguide core.

Fitting multiple effective index spectra yields both geometric parameters (the waveguide core width and thickness) and optical parameters (refractive index of the core and cladding) [2, 3]. The waveguide geometry can be found to a precision of less than 1 nm. The refractive index is typically fit to a Sellmeier equation to yield index values from the visible to the C-band, depending on the material transparency window, with a precision better than 0.1%. Heating the waveguide can be used to find the core and cladding thermo-optic coefficients over a similarly broad wavelength range.

2 SiN Example

In Fig. 1(a) we show the results of our fitting for a silicon nitride (SiN) waveguide. The data points are the measured effective indices, and the lines are the converged fits. The agreement is excellent, as indicated by a mean-square error (MSE) of 1.4×10^{-7}. The associated parameters from the fitting are shown in Fig. 1(b), in which the fitted optical parameters for the core and cladding are shown as refractive index using the Sellmeier functions.

3 Conclusions

We also discuss broadband loss measurements in waveguides, for which we are devising similar inverse fitting methods to extract material (absorption) and geometric (sidewall roughness) sources of loss. Current efforts are focused on expanding the number of parameters included in the waveguide model, such as angled sidewalls, or material birefringence. We are also examining new materials, such as Al_2O_3 and AlN. With waveguide interferometry, wafer-scale variability can be measured and tracked, simultaneously giving designers statistical information for robust component design, and foundries information about tool and process performance. As more materials are added to standard photonic fabrication processes, accurate knowledge of the as-fabricated optical and geometric properties of the materials is essential to successful circuit design.

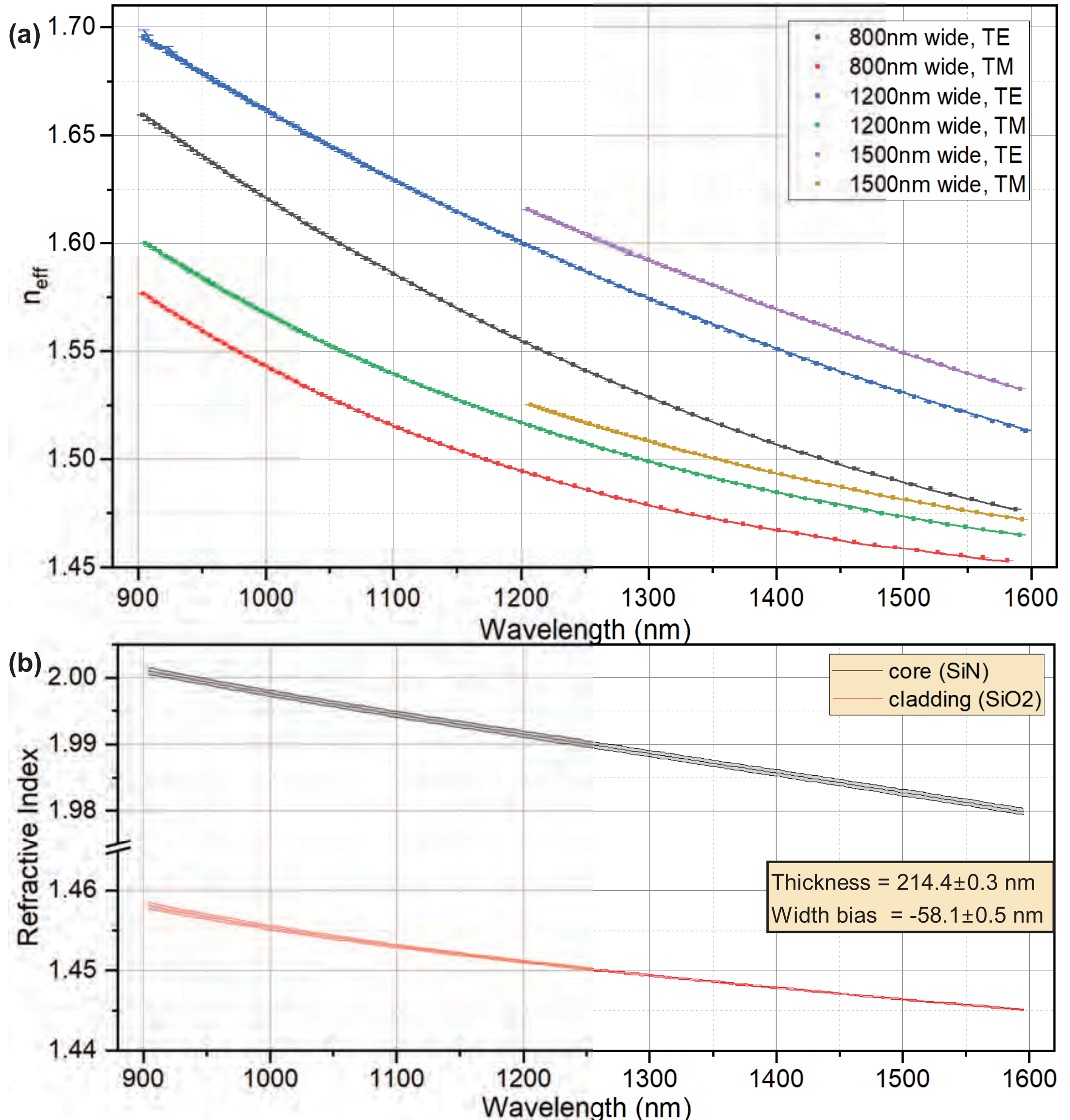

Figure 1: **(a)**: The measured and fit effective indices for a SiN waveguide. **(b)**: The associated parameters found from this fit. Shaded regions and reported errors represent 1-sigma fit error.

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Beyond the Exit of the Device Miniaturization Tunnel

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INTRODUCTION

For the past fifty years, researchers of semiconductor technology have felt like walking inside a tunnel. There was a single path forward – two-dimensional down-scaling of device sizes, also referred to as 2D miniaturization. With device features approaching atomic scale, semiconductor technology has reached the exit of this tunnel. The future is bright at the exit of the tunnel as there are many possible paths that create new opportunities for architectures that are extremely difficult (or even impossible) to implement using existing technology approaches that rely mainly on 2D miniaturization. It is no longer possible to draw a clear boundary between design and fabrication. Many innovations across the entire system stack – from architectures to circuits, devices, fabrication processes, and materials – will provide large multiplicative benefits at the system level. And there will be a change in the supplier-integrator and fabless-foundry ecosystems that have been in place for over 30 years.

Specifically, AI computation benefits tremendously simply by having more on-chip memory capacity. To derive the highest energy efficiency, not only the chip architecture needs to be application domain specific, but the memory technologies must also be application domain-specific to capture the highest benefits while incurring the lowest impact on latency, bandwidth and cost. As an example, I will describe the use of ultra-low leakage transistors ($< 10^{-18}$ A/µm) with large band gap oxide semiconductor materials to build gain cell memory. Gain cell memory has only two transistors and can be built in a 3D stack (thus small cell size and high density) that can complement SRAM to provide larger on-chip memory capacity [1]. More importantly, these memory technologies can be integrated on Si logic chips to arrive at a computing system that integrates multiple heterogeneous device technologies in a 3D monolithic, stacked, assembled integrated circuit: 3D MOSAIC [2]. These Differentiated Access Memory (DAM) systems will require us to revisit and re-examine computing at all levels, from the design of new memory technologies to high-level algorithms.

OXIDE SEMICONDUCTOR GAIN CELL MEMORY

Domain-specific computing systems require cross-compute-stack optimization, with a particular focus on memory access, which often limits overall system performance (broadly defined). Understanding and optimizing memory based on specific applications is crucial [3]. The two-transistor (2T) oxide semiconductor gain cell on-chip memory presents a promising solution to the "memory wall" problem by offering high density and minimizing off-chip DRAM accesses. Oxide Semiconductor (OS) transistors with ultra-low leakage expand the design space by providing longer retention times, albeit at the cost of speed [1]. Traditionally, retention has been managed through refresh operations. Yet, exposing retention to software and mapping it to data lifetime can become a powerful design parameter in balancing speed, power, and density.

Diverse gain cell configurations (Si-Si, OS-OS, OS-Si) and OS FET device designs enable fine-grained control over retention, speed, density, and power consumption. These variants are demonstrated on fabricated N40 CMOS+X monolithic 3D integration chip and N5 PDK simulation at the array level. Hybrid gain cell (OS-Si) demonstrates 3× density and 95% frequency compared to high-density (HD) SRAM. Furthermore, integrating gain cells with non-

volatile memories (e.g., RRAM) unlocks synergistic system-level benefits from device-circuit-architecture co-design, embodying the “1+1>2” philosophy where diverse memory technologies collaboratively enhance system functionality through integration.

This talk will cover gain cell device physics and design from the ground up, including:

1. Physics understanding and modeling of oxide semiconductor transistors [4]
2. Device design guidelines and integration with CMOS [1][5]
3. Scaling up in array size and scaling down to advanced technology nodes [5]
4. Memory macro compiler that accelerates memory circuits design [6]
5. Device-System Co-design of RRAM and Gain Cell memory integrated on Si CMOS [7]

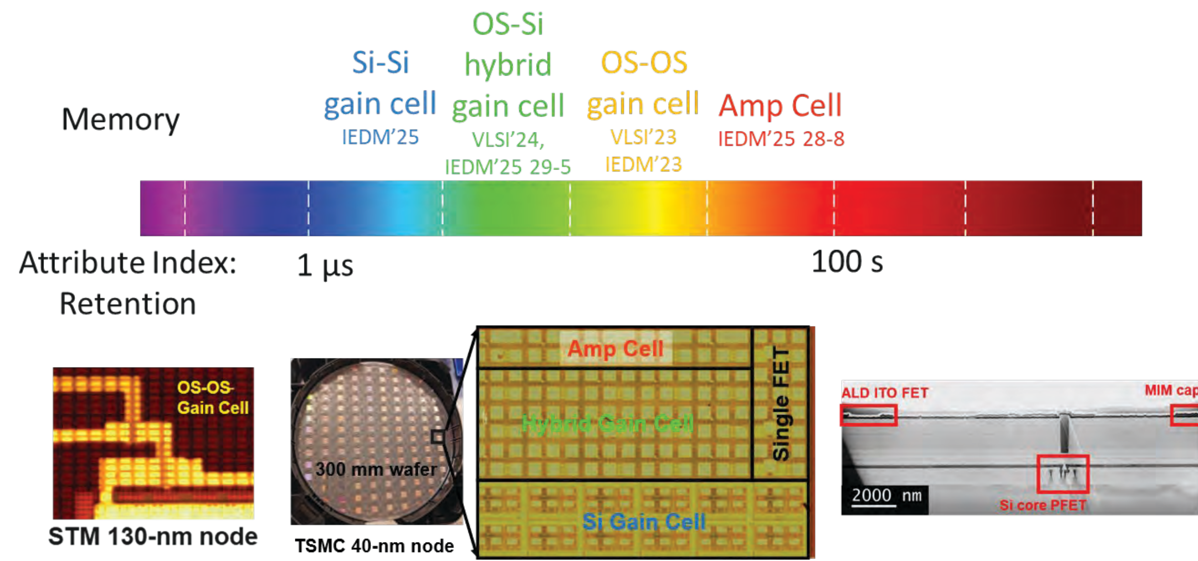

FIGURE 1. The wide range of retention times offered by various gain cell configurations (Si-Si, OS-OS, OS-Si) provides an extensive design space for different applications.

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KEYWORDS

Gain cell, oxide semiconductor, scaling, 3D integration, AI computation

Mueller Matrix Spectroscopic Ellipsometry based Scatterometry of Nanosheet Structures for GAA Transistors using a Hybrid Metrology Approach

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INTRODUCTION

Optical scatterometry has proved to be a robust means of monitoring the feature shape and dimensions of semiconductor structures. Along with specialized scanning electron microscopes known as CD-SEMs, used for critical dimension measurements, optical critical dimension scatterometry (OCD) provides manufacturing process control for the most advanced transistor and capacitor structures found in microprocessors and metrology integrated circuits. This talk provides an overview of Mueller Matrix spectroscopic ellipsometry (MMSE) and its application to OCD. New Si/Si(1-x)Ge(x) superlattice nanosheet, gate-all-around transistor structures continue to challenge metrology. In this talk, a Nanowire Test Structure (NWTS) provides a test vehicle for demonstrating MMSE-OCD. The use of X-Ray diffraction and scanning transmission electron microscopy (STEM) imaging and energy dispersive X-ray (EDS) analysis to verify feature shape and dimensions will be discussed. In addition, we show the usefulness of HR-XRD for determining layer thickness from scribe lines is useful for enabling OCD models. Verification of structures using feature shape and dimension data from STEM is also discussed.

EXPERIMENTAL

The NWTS was fabricated from wafers having 8-Si/Si(1-x)Ge(x) layer superlattices, and the structure is shown in Figure 1. The NWTS has oval holes fabricated using standard contact hole processes. An un-patterned wafer, and 3 NWTS wafers were used in this study. The NWTS before cavity etch is referred to as 0E, the NWTS wafer having a cavity etch is referred to as 10E, and the NWTS wafer having the longest etch is labeled as 20E. $\omega - 2\theta$ X-ray diffraction was used to characterize the Si and Si(1-x)Ge(x) film thickness and Ge concentration of all 8 superlattice layers for all samples. The $\omega - 2\theta$ measurements for patterned wafers were measured in the scribe-lines. The average film thickness values for patterned wafers were used in the OCD model. Figure 2 shows the change in layer thickness across the center of the un-patterned wafer based on HRXRD measurements. The Mueller matrix spectroscopic ellipsometry data was obtained in the patterned die. Cross-sectional STEM images were obtained on samples coated with Hf oxide in the cleanroom. The cavity etch was characterized by XRF measurement of Ge concentration for E0, E10, and E20 coated samples.

RESULTS AND CONCLUSION

The amount of cavity etch was determined using OCD and compared to cross-sectional STEM and XRF measurements. The across-wafer uniformity of the E20 cavity etch is shown in Figure 3. This work also shows that XRF can be used to monitor the amount of cavity etch.

ACKNOWLEDGEMENTS

The author gratefully acknowledges the effort of Ezra Mel Pasikatan (graduate student), Andy Antonelli and Nick Keller for scatterometry (ONTO), and Markus Kuhn and Satoshi Murakami for assistance with X-Ray characterization (Rigaku), and Subhadeep Kal, Matthew Rednor, Kandabara Tapily, Dave Hetzer, and Mark Schaefer for providing the samples and sample preparation for STEM (TEL). We also acknowledge Kevin Misic for STEM measurements.

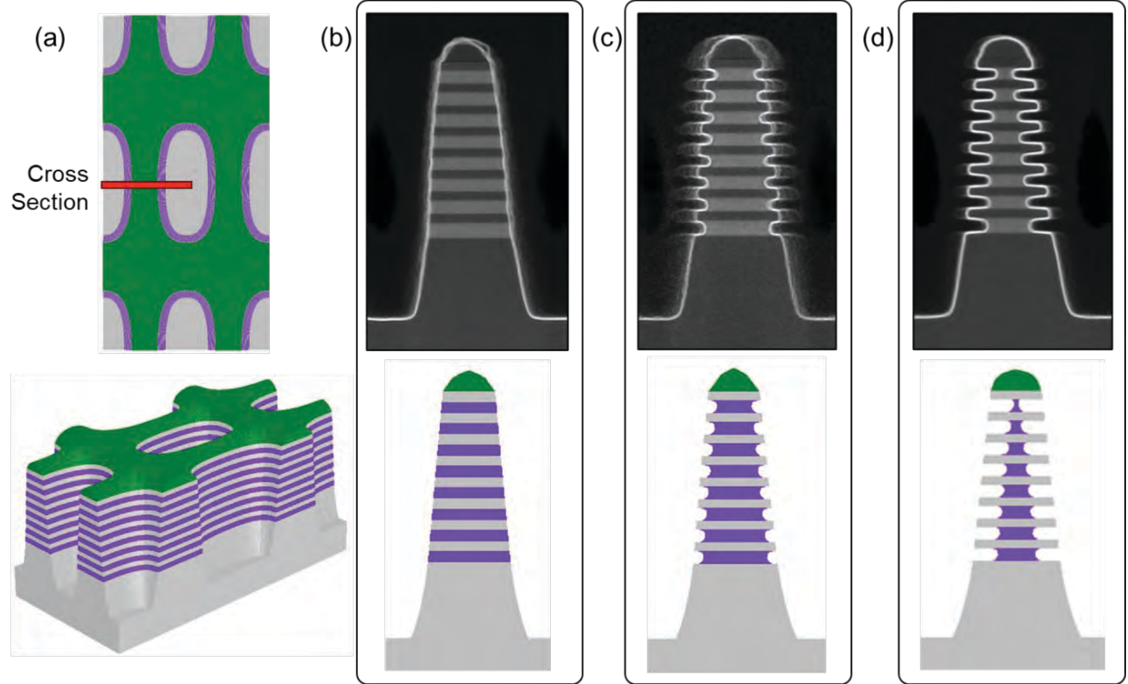

FIGURE 1. The Nanowire Test Structure (NWTS) samples fabricated using the 8x Si/$Si_{1-x}Ge_x$ superlattice are shown. (a) The OCD model structure is shown in top down and side view projections. HAADF STEM cross-sections of the NWTS are shown for the NWTS with no cavity etch in (b) 0E HAADF STEM image (top) and 0E OCD model y-slice (bottom). The two cavity etch samples are shown in (c) 10E HAADF STEM image (top) and 10E OCD model y-slice (bottom) (c) 20E HAADF STEM image (top) and 20E OCD model y-slice (bottom). The silicon is shown in gray, the silicon germanium alloy in purple, and the silicon nitride in green. Figure from Reference 1.

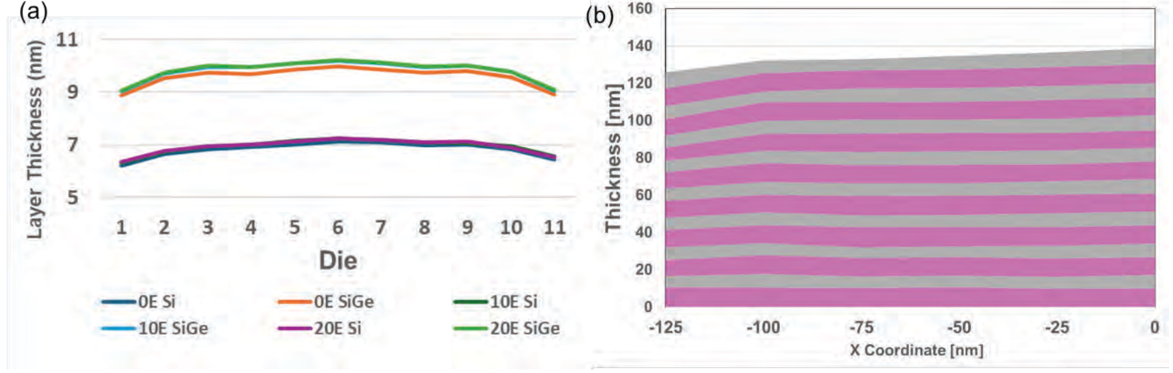

FIGURE 2. The across wafer HRXRD characterization of film thickness is summarized to show the film thickness variation. (a)Average film thickness across the wafer for 0E, 10E, and 20E samples determined using small spot ω-2θ X-Ray Diffraction analysis of scribe lines close to the associated die. (b) A cross-sectional view of film thickness variation from the edge to the middle of the wafer using HRXRD

film thickness values for the un-patterned film sample. Large area HRXRD measurements were taken in the position where Dies 1 through 6 would be patterned. Figure from Reference 1.

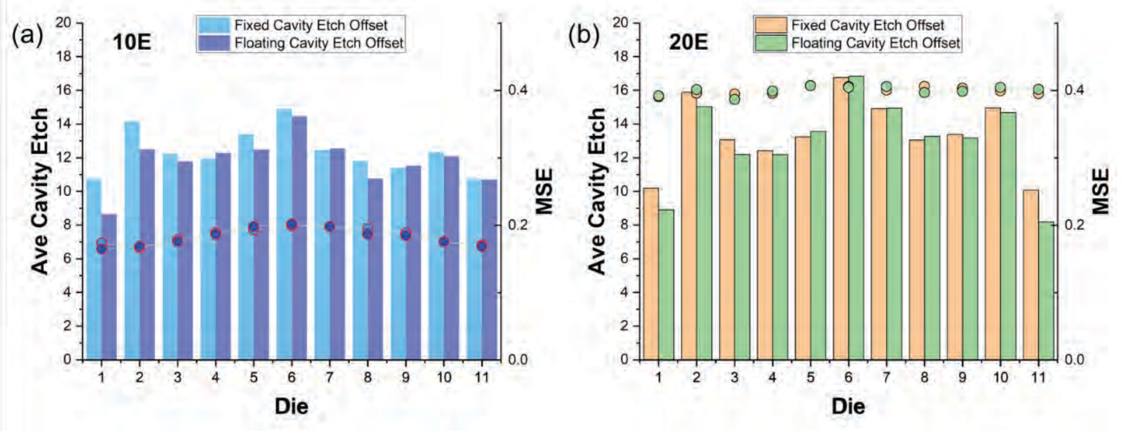

Figure 16: Across wafer cavity etch values for cavity etched samples 10E (a) and 20E (b) shown using filled circles. Both (a) and (b) show the mean square error on the right y axis. This data shows that the average cavity etch value is not strongly impacted by the variation in average superlattice layer thickness across the wafer as shown in Figure 15. The 11 parameter model was used to determine cavity etch for this figure. Figure from Reference 1.

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KEYWORDS

Transmission electron microscopy, X-ray diffraction, X-ray fluorescence, Nanosheet transistorss, Optical metrology, Scatterometry

Plasma XPS: a New Operando Metrology for Semiconductor Process Development and Control

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INTRODUCTION

Plasma-based processing plays a central role in advanced manufacturing, particularly in semiconductor fabrication, where plasma etching, sputtering, plasma-enhanced atomic layer deposition (PEALD), and chemical vapor deposition (PECVD) are key technologies to engineer interfaces with atomic-layer thickness and chemical precision. Conventional ultra-high vacuum (UHV) X-ray photoelectron spectroscopy (XPS) is one of the powerful surface analysis tools. However, its inability to analyze plasma-induced surface reactions in real time under relevant processing pressures has left a critical metrological gap.

Addressing this longstanding limitation and need, we report here on the pilot tests and developments of a plasma-compatible ambient pressure X-ray photoelectron spectroscopy (plasma-XPS) platform as a real-time diagnostic tool for *operando* characterization of surface transformations, plasma-induced reactions, and metastable chemical states relevant to the aforementioned plasma processing technologies employed in semiconductor fabrication. Using model metallic and dielectric substrates, we demonstrate the capabilities of the metrology to follow plasma-driven oxidation/reduction reactions and the identification of transient surface intermediates. We discuss key challenges, including plasma-induced charging, peak broadening, binding energy (BE) shifts, and propose both interpretive frameworks and experimental solutions.

We also demonstrate the ability of metrology to monitor real-time gas phase XPS spectra in plasmas and found that plasma can induce BE shifts and satellite formations that are strongly influenced by plasma parameters (e.g., plasma potential, composition, pressure). The latter offers opportunities for XPS-based real-time electrical and compositional plasma diagnostics. All the above establish plasma-XPS as a prospective metrology platform for advancing process development and control in plasma-assisted manufacturing as well as in materials science.

EXPERIMENT

Plasma-XPS measurements were performed at the Center for Functional Nanomaterials at Brookhaven National Laboratory, equipped with a commercial lab-based ambient pressure (AP) XPS system [1] (Figure 1). The reaction chamber is equipped with a custom-made capacitively coupled AC plasma reactor operated within 5 Pa to 500 Pa pressure range. The reactor is separated from the multi-stage differentially pumped electron spectrometer by a small cone aperture to enable XPS data collection at elevated plasma pressures. A monochromatized Al Kα X-ray source (hν = 1,486.6 eV) was used for photoelectron excitation. Ultrathin X-ray transparent SiN membrane separates X-ray source from the reactor chamber. The second APXPS differential pumping stage is equipped with a quadrupole mass spectrometer for residual gas analysis (RGA) of the reaction chamber during plasma experiments. UV-vis optical spectrometer was used for general plasma diagnostics.

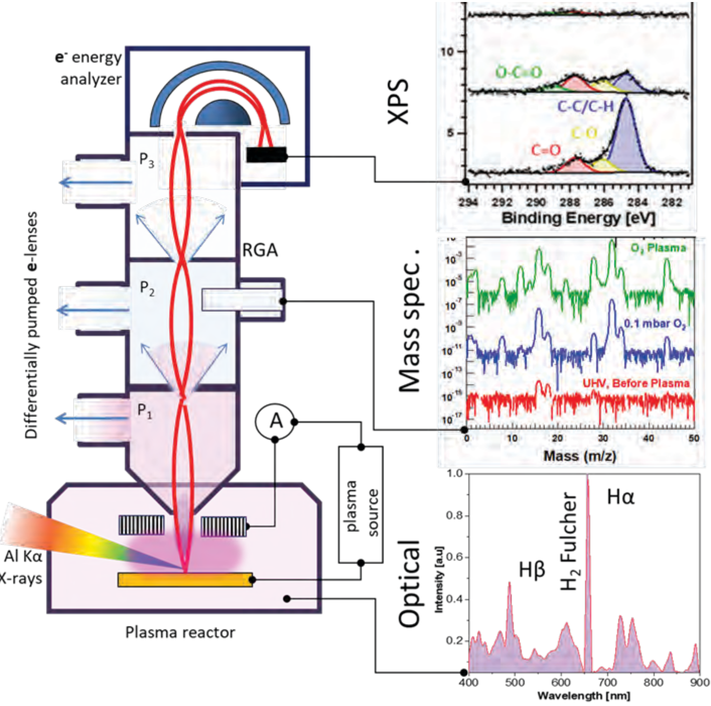

FIGURE 1. The principle schematics of the plasma-XPS method (left) and surface/gas phase characterization channels (right) that include XPS, mass spectroscopy, UV-vis optical diagnostics and electrical probes (not shown).

APPLICATION EXAMPLES

Surface Oxidation, Reduction During Reactive Plasmas Exposure

Using a clean metal as model system, we demonstrated the dynamic capabilities of plasma-XPS in tracking surface oxidation and reduction cycles in real time under sequential O_2 and H_2 reactive plasma treatments. Notably, the metal surfaces exhibited reversible oxide formation and removal, as well as metastable states formation. This real-time capability demonstrates a substantial advance over conventional before/after XPS methodologies

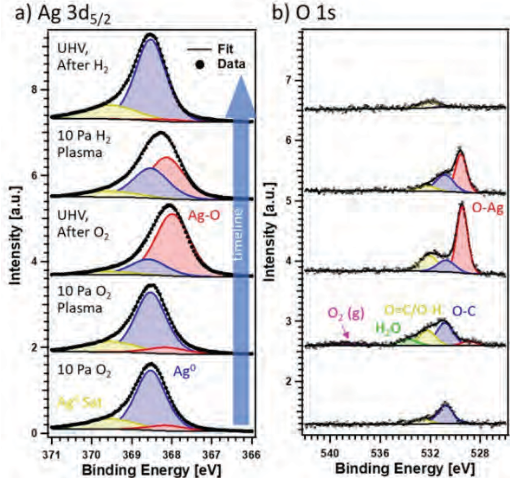

Figure 2. XPS of the oxidation and reduction of Ag(111) sequence from the bottom to the top rows: bottom: exposed to 10 Pa O_2; second: during 10 Pa O_2 plasma treatment; after quenching O_2 plasma but still with overpressure of O_2 (third); during 10 Pa H_2 plasma treatment (fourth row), and after quenching H_2 plasma still with overpressure of H_2

(top) for the Ag 3d (a) and O 1s (c) core levels. Note that the O 1s gas phase contribution O_2 (g) can be detected (see below).

Gas Phase XPS Spectra and Plasma Diagnostics

The integration of gas-phase XPS and RGA enables simultaneous detection of volatile plasma-induced products such as CO and CO_2, (Figure 3 a, b) confirming that significant plasma-induced chamber wall reactions occur during plasma ignition [2]. These wall effects, if not accounted for, can misrepresent surface-specific chemistry. The evidence highlights the importance of correlated gas- and surface-phase diagnostics in future plasma-surface studies. We also show that the gas phase XPS spectra of even inert gases can be drastically affected by the AC plasma. The formation of plasma-induced satellites (Figure 3 c) with few eV BE shifts to higher energy and large peaks broadening appear due to the presence of the positive oscillating plasma potential at the probing volume. Overall, gas phase plasma-XPS can be used not only for plasma compositional but also for electrical diagnostics via the local measurements of the plasma potential as BE shift [3].

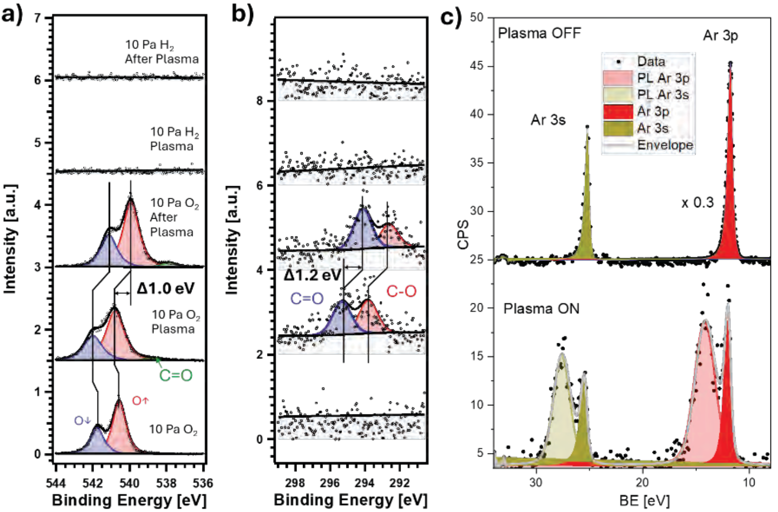

FIGURE 3. Gas phase XPS of both the O 1s (a) and C 1s (b) core levels for initial backfilling of molecular O_2 in the analysis chamber (bottom row), followed by plasma ignition (second raw from the bottom) and quenching with the same chamber environment (third row). Then the chamber is purged and backfilled with the same pressure of H_2 gas, followed by H_2 plasma ignition (fourth row from the bottom). c) Ar 3p, 3s, spectra collected with 500 Pa Ar plasma ON (bottom curve) and plasma OFF (top curve) conditions.

CONCLUSIONS

In summary, plasma-XPS metrology presents a powerful analytical approach that enables real-time, spatially and chemically resolved studies of surfaces and gas phases under reactive plasma conditions. It offers a transformative path forward for advancing our understanding of plasma-surface interactions and for developing new process control strategies across a broad spectrum of high-tech applications—from microelectronics to energy and biomedical technologies.

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KEYWORDS

Plasma-XPS, operando, process development and control, reactive intermediates, in situ, plasma diagnostics

Influence of metallic contamination on CMOS image sensors and analytical techniques

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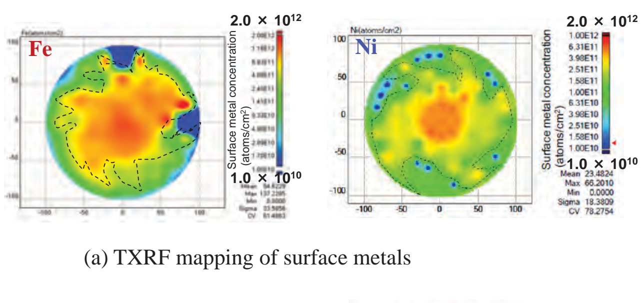
Sony Semiconductor Solutions Corporation

INTRODUCTION

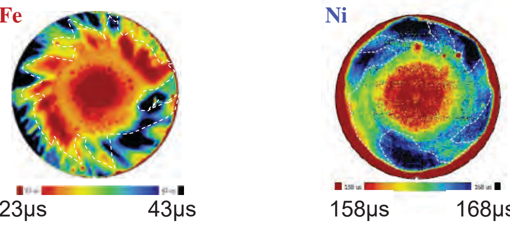
Metallic contamination and crystal defects in the photodiode cause the dark current in CMOS image sensors. Metal impurities must be strictly controlled in the wafer processing. High sensitivity metallic contamination detection techniques are required for metallic contamination control. Better understanding the penetration, diffusion, and gettering behaviors of metal impurities. In this presentation, we have extensively reviewed the influence of metallic contamination on CMOS image sensors and their detection and analysis techniques.

CARRIER RECOMBINATION CENTERS IN SILICON

It is important to know if metal impurities penetrating silicon are electrically active or not. If the metal impurities generate recombination centers in the mid gap, they deteriorate device characteristics or yields. In-wafer distribution of recombination centers can be detected with high sensitivity and visualized with μ-PCD and photoluminescence. The distributions of surface metal concentration measured with TXRF before ion implantation are in good agreement with that of recombination lifetime after ion implantation followed by annealing. In this experiment, the concentration of surface Fe and Ni concentration was varied from 1.0×10^{10} to 1.3×10^{12} atoms/cm^2, and 2×10^{11} atoms/cm^2 in average in the wafers, as shown in Fig. 1.



(a) TXRF mapping of surface metals



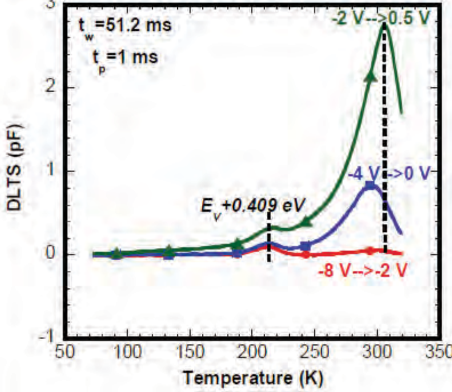
(b) Recombination lifetime

FIGURE 1. Fe and Ni concentration on the surface before arsenic ion implantation and recombination lifetime of silicon with 20 nm SiO_2 after ion implantation followed by annealing.

The recombination lifetime after arsenic ion implantation of the wafers contaminated with Fe varied from 23 µs to 43 µs, as shown Fig. 1 (b). As the amount of Fe contaminated before the implanataion is larger, the resultant recombination lifetime is shorter. The recombination lifetime of the wafers contaminated with even small amount of Fe as much as 1.0×10^{10} atoms/cm^2 is significantly short. On the other hand, the recombination lifetime after arsenic ion implantation of the wafers contaminated with Ni is varied from 158 µs to 168 µs and is longer than that of Fe. Ni is more difficult to generate deep levels than Fe because interstitial Ni is not electronic active, but substitutional Ni is active and the amount of the substitutional Ni is extremely small. This is the reason why the recombination lifetime of the wafer contaminated with Ni is longer than that of Fe. Nevertheless, the in-wafer distributions of surface Ni concentration before ion implantation shown in Fig.1 (a) is still in good agreement with that of recombination lifetime after ion implantation followed by annealing, same as Fe. The region of high concentration metals in the wafer before ion implantation yields carriers with a short lifetime after ion implantation even in 20-nm-thick SiO_2 wafers. It should be noted that low level surface Fe and Ni contamination as little as 2×10^{11} atoms/cm^2 can generate carrier traps even when dopants were implanted through SiO_2. As further reduction of the surface contamination will be required, measurement techniques of recombination centers with higher sensitivity will also be required.

METAL-INDUCED DEEP LEVEL IN SILICON

The depth profiles of the metal-induced deep level depend on metal species and annealing temperatures. Deep levels of the transition metals such as Fe, Ni, and Cr are well reported [2]. Since these metals are fast diffusers, it is difficult to obtain the depth profiles of their deep levels. We have demonstrated the deep level, capture cross-section, and the depth profile of thermally-diffused W in silicon [3]. Two peaks are found in the DLT-spectra of the p-type CZ Si wafers contaminated with W and annealed at 950 ^oC for 10 min: one around 215 K with apparent activation energy E_T of 0.409 eV derived from the Arrhenius plot and, secondly, a broad peak around 300 K, with a peak maximum which shifts with the bias pulse, so that it is difficult to derive a unique activation energy. The 215 K peak is dominant at larger depths from the surface, i.e., for a pulse from -8 V to -2 V, while the deeper trap becomes pronounced closer to the surface and behaves more like an extended defect, with a peak position shifting with reverse bias. Note that these hole traps are absent in reference samples, annealed at 950 ^oC for 10 min. The profile corresponding with the E_V+0.409 eV hole trap has been measured in the temperature range between 200 K and 230 K at two temperatures in that range. The maximum depth is determined by the maximum reverse bias used. A rather flat profile corresponding with a concentration of ~5×10^{13} cm^{-3} is found starting from 0.5 µm depth. At lower depths, the concentration of the 0.409 eV level increases towards the surface, which is particularly clear for the 220 K data. The sensitivity of the current deep level measurements is limited by the junction area and insufficient for the deep level measurements of extremely low concentration of metal impurities depositing on and penetrating silicon in wafer processing in production lines. The sensitivity of the deep level measurements should be improved.



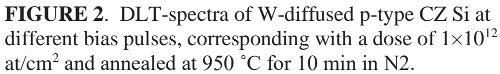


FIGURE 2. DLT-spectra of W-diffused p-type CZ Si at different bias pulses, corresponding with a dose of $1{\times}10^{12}$ at/cm^2 and annealed at 950 ˚C for 10 min in N2.

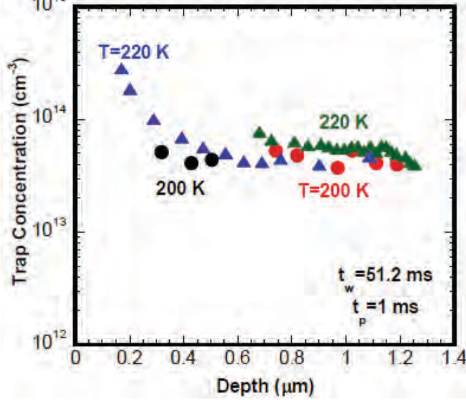
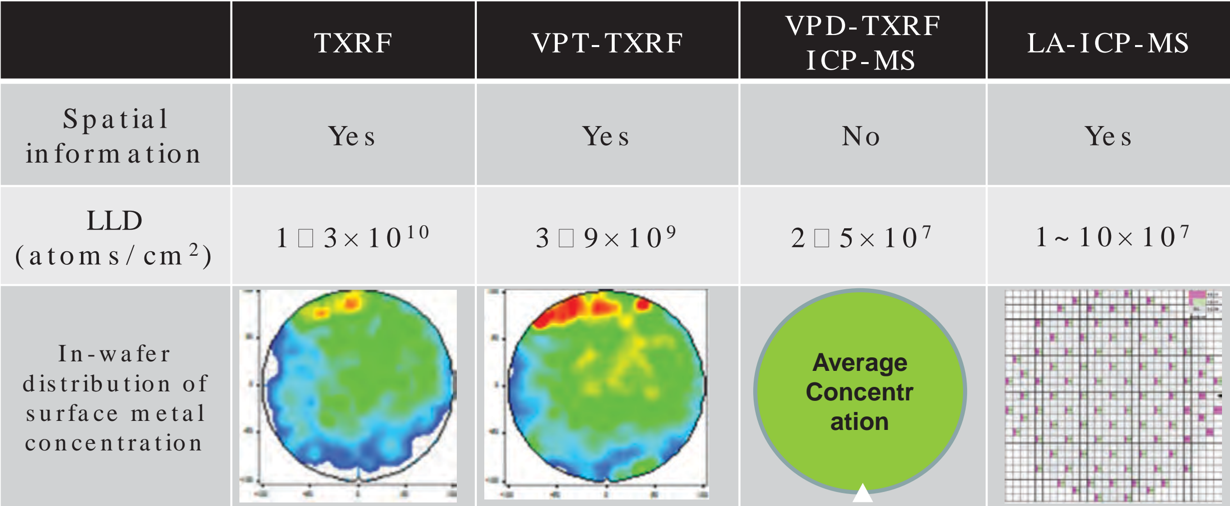


FIGURE 3. Trap concentration profile at 200 K (circles) and 220 K (triangles) for the EV+0.409 eV peak, measured with a saturation bias pulse of 1 ms and a sampling period of 51.2 ms.

DETECTION AND ANALYSIS OF SURFACE METAL CONTAMINATION

Trace metallic contamination on the silicon surfaces can be detected with VPD- or LPD-TXRF, AAS, and ICP-MS and these methods have been widely used. These analyses provide average metal concentration on the whole wafer surface with high detection sensitivity, while they do not give in-wafer distribution of metal concentration. However, metal impurities accidentally deposited in wafer processing are often localized. Direct TXRF provides in-wafer distribution of metal concentration, while its sensitivity is insufficient. Therefore, methods to detect localized metal atoms with high sensitivity are required. TXRF following vapor phase treatment (VPT) has been developed to enhance detection sensitivity without droplet collection [4] and the influence of VPT-induced trace particles on the detection sensitivity has been studied [5]. Recently, the Laser Ablation - Inductively Coupled Plasma Mass Spectrometry (LA-ICP-MS) has been developed by RORZE-IAS [6]. The calculated detection limit of Zn was 2×10^8 atoms/cm^2. Such a metallic contamination detection technique with high detection sensitivity per small spot helps root-cause analysis of metallic contamination sources.



	TXRF	VPT-TXRF	VPD-TXRF ICP-MS	LA-ICP-MS
Spatial information	Yes	Yes	No	Yes
LLD (atoms/cm^2)	1□3×10^{10}	3□9×10^9	2□5×10^7	1~10×10^7
In-wafer distribution of surface metal concentration			Average Concentr ation	

FIGURE 4. Surface metallic contamination measurement techniques.

Summary

We have extensively reviewed metallic contamination control including the analysis, prevention, removal, and gettering in CMOS image sensor processing. Better understanding the behavior of metal impurities diffusing is required for controlling yield of CMOS image sensors. The detection sensitivity of surface metallic contamination analysis and the deep level recombination measurements should be improved.

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KEYWORDS

metallic contamination, analysis, TXRF, ICP-MS, DLTS, μ-PCD

Novel Applications of Nanoscale IR Spectroscopy Coupled with AFM for Semiconductor Metrology

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INTRODUCTION

The ability to detect the chemical origin of materials underneath the sensing probe has been an outstanding challenge for Atomic Force Microscopes since the advent of the technique. Over the last 20 years several measurement methodologies have arisen to close this gap including Tip Enhanced Raman Spectroscopy (TERS), Scanning Nearfield Optical Microscopy (SNOM) and Photothermal Atomic Force Microscopy-Infrared Spectroscopy (AFM-IR) [1,2]. Each technology has been developed to close the gap between nanoscale morphological and chemical analysis.

Photothermal AFM-IR works by detecting the photothermal induced expansion of a material in response to interaction with a pulsed IR light source. AFM-IR has strengths as a method which can convert nanoscale IR spectroscopy from an optical excitation to a mechanical detection, relying on the natural sensitivity of AFM to infinitesimal forces. Operating in resonant modalities the Q-factor of the AFM cantilever amplifies signals and allows for the detection of <1 nm thick materials. Historically, Photothermal AFM-IR has been most favored in soft-matter applications. As the signal in AFM-IR is determined through the high speed deflection signal on position-sensitive photodecteror, improvements to system Z noise performance has expanded the capability for monolayer detection beyond metal substrates to dielectric materials and materials with low coefficients of thermal expansion, increasing application space, opening up new application areas in hard-matter, electronic and semiconductor materials [3-5]. This presentation aims to highlight core applications of AFM-IR in the metrology of advanced nanoelectronic materials

ABSTRACT

Nanocontamination, thin films and photoresists make up some of the significant application areas for photothermal AFM-IR in semiconductor metrology. AFM-IR enables high-resolution chemical analysis of surface contamination. Components are located on a sample substrate using reference coordinates, typically a KLARF coordinate-file. Figure 1 shows a typical example of a nanoscale contamination particle, approximately 30 nm across and 2 nm tall. Spectra on the material can be compared against FTIR databases such as Wiley's KnowItAll which identifies the particle as PLA (Polylactic Acid).

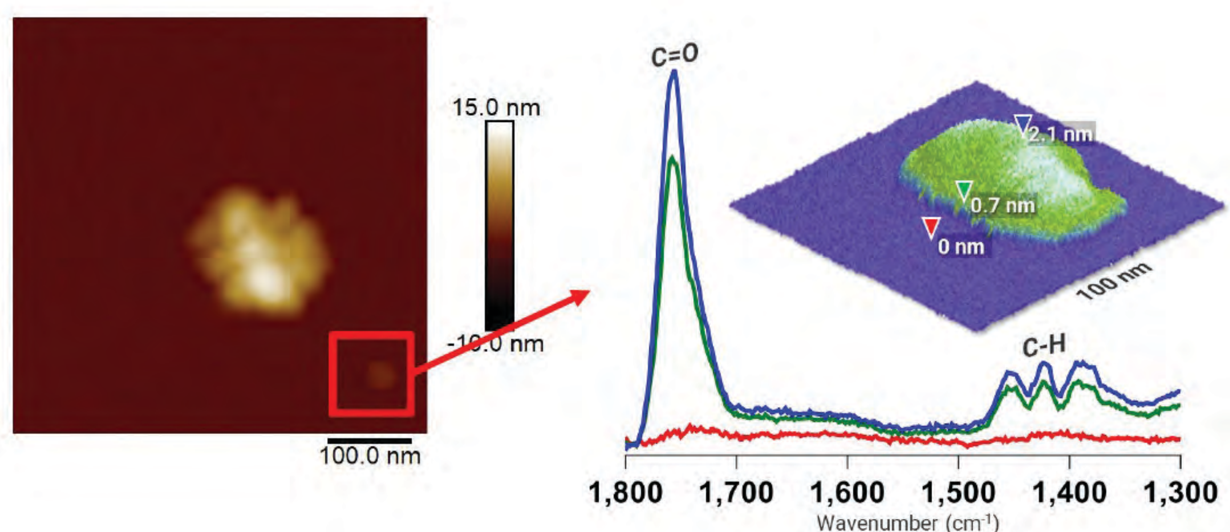

FIGURE 1. Chemical identification of a <3 nm thick particle with Photothermal AFM-IR. (Left) Topography map of survey area with inset red square identifying region of interest. (Right) Chemical map and spectra collected on (blue,green) and off (red) of the polymer nanoparticle. Chemical map at 1760 cm-1 overlaid on the height map with higher IR response in green/white and lower IR response as purple/black.

The high sensitivity of photothermal AFM-IR can also be used to detect materials with low or negative coefficients of thermal expansion. Figure 2 shows an atomically flat four layer graphene sample. By tuning to characteristic wavelengths different layers of material respond in the IR in an otherwise featureless material. Identifying the layer structure can be directly linked with energy transfer in the material, building fundamental understanding on the structure-chemistry-property relationship. Photothermal AFM-IR allows one to get insights into both the surface and subsurface characteristics of 2D materials. Correlative imaging with other AFM modalities including scanning microwave impedance microscopy (sMIM) will be explored, providing complimentary nanoscale data.

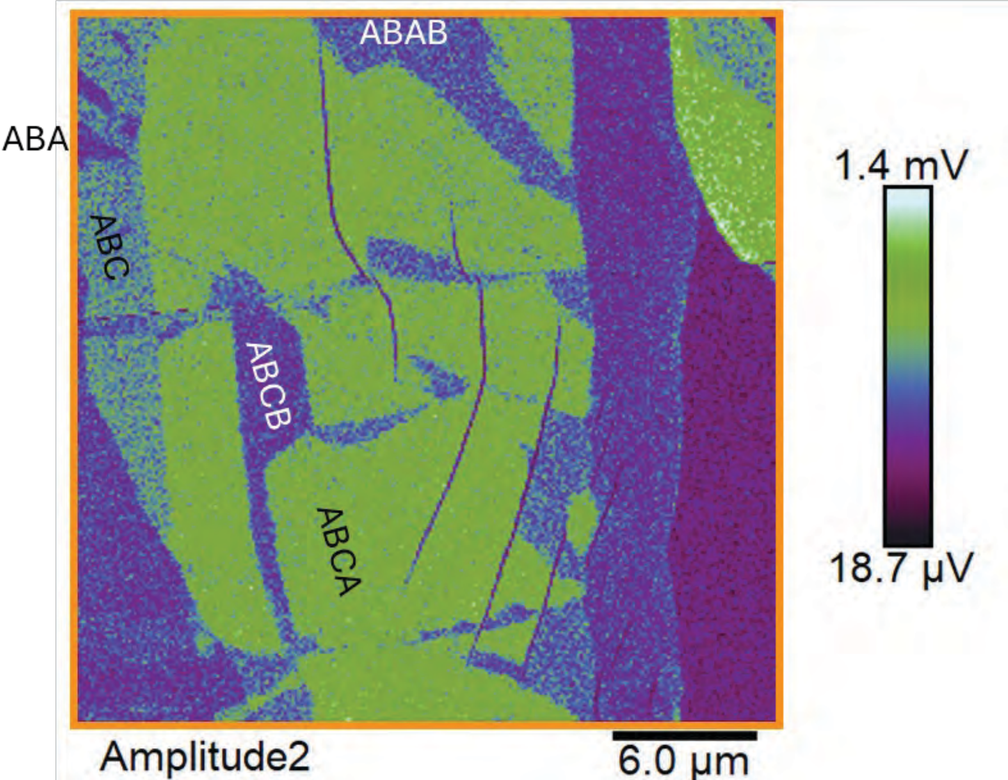

FIGURE 2. Photothermal AFM-IR absorption map of an atomically flat flake of 4 layer graphene acquired at 1576 cm^{-1}.

This presentation aims to introduce the photothermal AFM-IR technology and highlight key applications for the technique for characterization relevant to semiconductor industry and nanoelectronic devices. Applications related to nanocontamination, selective surface deposition, dielectrics, 2D materials, EUV photoresist, and pre-bonding inspection in hybrid bonding processes will be discussed. In the latter, we briefly outline complementary AFM capabilities relevant to critical nanoscale surface morphology analysis, including nanoscale defectivity mapping, copper pad recess metrology, large-area (millimeter-scale) topography mapping and bevel edge profiling.

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KEYWORDS

AFM, nanoIR, Photothermal AFM-IR, nanocontamination, graphene, EUV photoresists

Improving the carbon detection limit with Secondary Ion Mass Spectrometry (SIMS)

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Dynamic SIMS is often used to evaluate the concentration of impurities in solids because of its high sensitivity, depth profiling capabilities, good depth resolution, and high throughput. Continuous ion beam sputtering with a high-density primary beam provides high sensitivity and reduces the background contribution from residual gases within the analytical chamber. Dynamic SIMS experiments performed with several magnetic sector instruments using various sputtering rate conditions demonstrated a slow decrease of the carbon detection limit with the increase of sputtering rate (SR), when it was varied by changing the sputtering beam density. The dependence data, within the scatter limits, can be fit by a power function of SR. The observed detection-limit-dependence curve is common for magnetic sector SIMS instruments, owing to contamination and the design of the analytical chamber. The depth resolution of light-element SIMS analysis (except for oxygen) performed using Cs+ sputtering is limited and cannot be improved by reducing the impact energy of the sputtering beam. A segregation-type depth profile with a long trailing edge was observed in the B, C, and N depth profiles when Cs+ sputtering was employed under ultra-high vacuum conditions. This effect is plausibly associated with preferential sputtering owing to the difference in the surface binding energy, along with the large difference in the mass of the interacting atoms within the collision cascade during sputtering. The depth resolution can be improved with surface oxidation when Cs^+ sputtering was combined with backfilling of the analytical chamber using O_2. The analytical chamber backfilled with oxygen can be sufficiently replaced with a very low-impact energy-focused oxygen beam, enabling simultaneous oxygen and cesium co-sputtering SIMS analysis. More practical approach for the shallow structures would be the surface carbon contamination removal avoiding the segregation type tailing. It can be cleaned by a plasma cleaner used for decontamination of the inner surface of the TEM/SEM chamber or the surface decontamination tool equipped with an oxygen radical's plasma source. Organic contamination reduction can be accomplished using the focused Arx gas cluster ion beam (GCIB) with an energy per atom lower than the sputtering threshold. It was observed that the surface carbon contamination on Si substrates can be completely removed with a gentle O_2^+ ion beam cleaning with energy-per-atom near the sputtering threshold. Exploring possibilities of removing carbon surface contamination on epitaxial grown SiGe layers using oxygen and argon based sputtering beams in magnetic sector and time-of-flight (TOF) SIMS instruments is the focus of this presentation.

Who Needs Electrical Back-Contacts After All?

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Electrical scanning probe microscopy is now a staple of materials characterization with impact on the Electrical scanning probe microscopy is now a staple of materials characterization with impact on the broader community of materials scientists, engineers and nanotechnologists. Starting from the last decade of the twentieth century, the combination of atomic force microscopy (AFM) with electrical secondary imaging modes has begun to offer a wide range of analytical techniques that combine nanoscale-resolved morphology from AFM with various readouts.[1-3] By applying either a static (DC) or alternating (AC) voltage between the tip and the sample, various phenomena such as tunneling current, conductivity, local surface potential, electrochemical reactions, carrier concentration, and piezoelectric response, among others, can be evaluated.[4-6] The list of techniques is long, and multiple publications describe them with great detail.[7-9] Based on the number of publications, some of the most successful techniques are clearly scanning tunneling microscopy (STM), Kelvin probe force microscopy (KPFM), scanning capacitance microscopy (SCM), piezoresponse force microscopy (PFM), conductive atomic force microscopy (C-AFM), and scanning spreading resistance microscopy (SSRM), among others.[10-14] Since their inception, these methods have been critical for addressing complex challenges in material synthesis, characterization, and optimization, spanning from fundamental research to industrial applications such as semiconductor metrology.[15]

While AFM methods for probing surface morphology have been integrated into industrial manufacturing processes, including quality control for automotive, aerospace, and semiconductor manufacturing, electrical AFM modes remain limited to small samples and continue to be measurements that are only partially automated.[16] Sophisticated instruments for AFM morphology, such as those deployed in modern semiconductor cleanrooms, are capable of remarkable scanning stability, large field of view, automation, high-speed data acquisition, and can potentially perform the majority of electrical AFM modes. However, a critical design constraint prevents their adoption in complete in-line wafer and panel metrology: the requirement for an electrical back-contact (BC).[17] Whether for two-probe DC techniques, such as C-AFM and SSRM, or AC-biased modes, like SCM, PFM, and KPFM, a physical electrical connection to the sample is essential to close the circuit or establish a potential difference. This reliance on back-contact constitutes a significant roadblock, preventing the automated deployment of electrical AFM modes in complex manufacturing environments. Using semiconductor metrology as an example, when measuring wafers during chip production, the need for BC forces the manufacturing flow to stop, breaking the entire wafer and obtaining a small coupon, later creating a conductive region by either using ion beam deposition, the application of conductive epoxy glues, or Ag-paste to create a connection between the sample surface and the AFM chuck. Needless to say, none of these steps are compatible with the level of low contamination required to continue the chip manufacturing process; thus, the entire wafer lot is often scrapped due to this step. These steps add prohibitive cost and complexity, which have prevented the adoption of electrical AFM modes for in-line metrology, even forty years after these modes have been introduced.

Furthermore, when targeting ultra-scaled devices, forming an electrical back-contact is complicated by the need to navigate specific electrical signal paths. Great care must be taken to avoid excessive contact resistance or interference with adjacent components. Ultimately, the placement and material selection of the back-contact significantly influence measurement quality; this is particularly critical when characterizing high-resistivity layers or integrated solid-state devices. In these scenarios, high series resistance within the tip-sample electrical loop can severely degrade the signal-to-noise ratio and overall sensitivity. This limitation applies to virtually all two-probe AFM techniques, hindering the full potential of these methods. Consequently, despite their widespread use in offline metrology labs and academic environments, electrical AFM modes have not yet been widely adopted for in-line wafer inspection.

To address the limitations imposed by physical back-contacts, we present a novel solution that replaces the mechanical connection with a low-energy electron beam focused on the sample surface near the AFM probe. We refer to this configuration as electron-beam excited AFM (EB-AFM). This approach yields results comparable to those of conventional techniques while unlocking applications previously inaccessible due to geometric or material constraints. In this work, we first describe the experimental setup and the key parameters that govern e-beam stimulation. We then demonstrate the efficacy of this strategy by performing contact-free electrical characterization on various samples such as 2D materials, metals, and III-V semiconductors, showcasing the competitive defect-mapping capabilities of electron-beam excited conductive AFM (EBC-AFM). Finally, we discuss the potential for extending this e-beam excitation strategy to other modes, specifically scanning spreading resistance microscopy and scanning tunneling microscopy, as well as its applications to fully integrated device structures

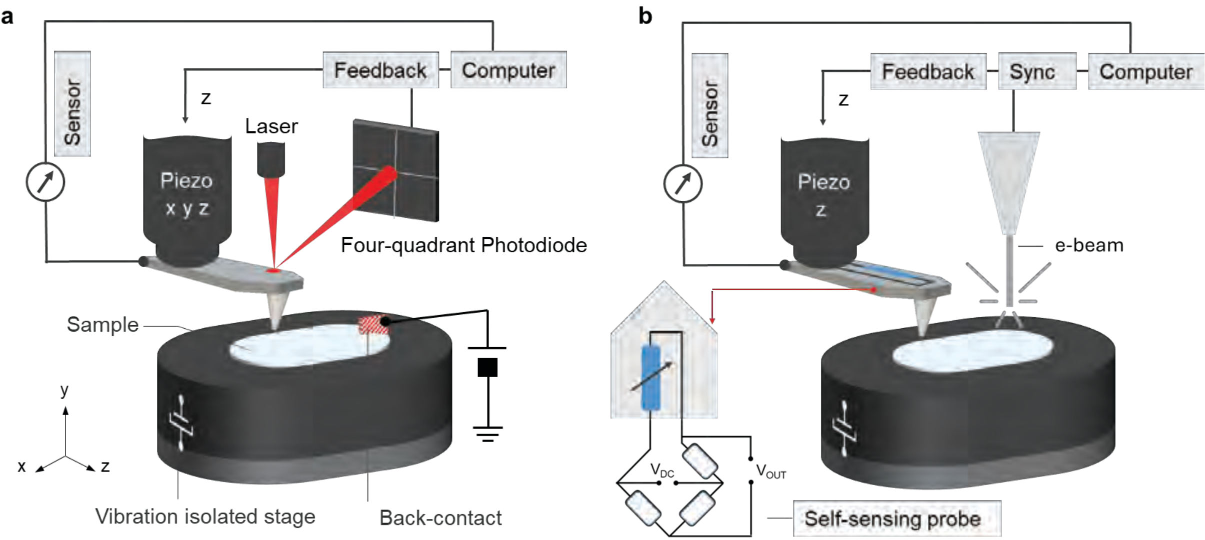

FIGURE 1. a. Basic schematic of the conventional setup of an electrical AFM. It utilizes a laser-photodiode combination system for probing and requires a physical back-contact to apply the tip-sample voltage for injecting charge carriers. **b.** Schematic illustrating the basic setup of EBC-AFM, which utilizes an e-beam to inject charge carriers without requiring back-contact. For probing purposes, a Wheatstone bridge-supported self-sensing mechanism is used (as in the inset).

RESULTS AND DISCUSSION

Figure 2 shows one practical application of e-beam to enhance our ability for site-specific characterization in fully fabricated chips. This is an important area of application for electrical AFM modes with ample use of these techniques for failure analysis (FA), process development, and reliability assessment. Emerging integrated logic devices such as gate-all-around field-effect transistors (GAAFETs) and 3D memory concepts such as current 3D NAND, and future designs for 3D dynamic random-access memory (DRAM), all depend on intricate three-dimensional structures to sustain performance scaling and follow the industry’s ongoing miniaturization goals. While enabling improved performance and reduced power consumption, these integration schemes introduce substantial challenges for conventional characterization techniques, which often lack the spatial resolution or sensitivity required to probe three-dimensional electrical and material properties at the nanoscale. In particular, chiplets and multi-die 3D integration pose a high level of complexity in accessing the area of interest in modern chips. This is generally addressed by a combination of material removal methods, including grinding, polishing, and the use of plasma-

assisted focused ion beam (PFIB), to access the area of interest (Figure 2a). However, access to the area of interest does not imply the ability to perform a localized electrical measurement, i.e., C-AFM or others. As in most cases, the device under test can be further electrically isolated by the presence of a junction, shallow trench isolation, or other electrical obstacles that limit the application of DC and AC signals between the tip and the sample. A simple example is reported in Figure 2b for the case of a modern 3D NAND vertical memory. Here, modern 3D NAND devices can have 200+ worldline layers, which translates into a vertical channel with a length exceeding 10 µm, resulting in substantial insertion of electrical series resistance when measuring conductivity in the channel using an AFM probe. Similarly, a scaled logic device, i.e., a transistor, could be isolated from the substrate because it is built using silicon-on-insulator technology, or because it is placed on a series of doped wells. For all these applications, our results indicate that e-beam excited probing with AFM can offer a potential solution. Figure 2b shows an example of EBC-AFM obtained in a de-processed 3D NAND memory array, after removing the top contacts and exposing the area of the vertical poly-Si channel. The bottom insets in Figure 4b show the region under test, as imaged with scanning electron microscopy (left) and EBC-AFM (right). Here, the contrast in the current map of EBC-AFM is generated without any physical back-contact by leveraging the presence of SEM e-beam, thus obtaining high resolution probing of the conductive poly-Si channel at a fraction of the complexity for the sample preparation. Finally, another potential case study is represented by the analysis of materials that are grown selectively and thus are locally isolated from any electrical grounding. Selective growth methods enable the direct integration of 2D materials onto target substrates or silicon complementary metal-oxide-semiconductor (CMOS) platforms, eliminating the need for a separate, often damaging, transfer process. Figure 2c shows the case of selective area deposition of synthetic MoS_2 grown inside patterned Al_2O_3 trenches. Clearly, the absence of a continuous closed film (SEM image in Figure 2c) would make it impossible to apply classic C-AFM. However, EBC-AFM can be directly applied to the area of interest without the need for any extra steps for the formation of a back-contact, as visible in the bottom inset of Figure 2c showing morphology and current for one of the isolated MoS_2 islands.

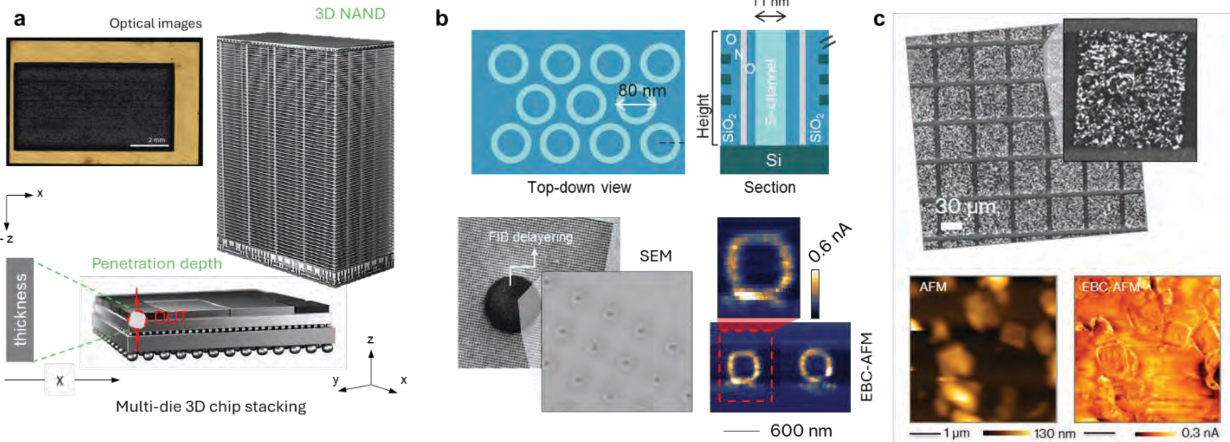

Figure 2. **a**. Schematic of 3D NAND outer look and multi-die chip stack. **b**. Schematic of 3D NAND showing the top view of the poly-Si channel and the corresponding cross-section. At the bottom, SEM and EBC-AFM images of the circular poly-Si channel from the top side. **c**. Top: SEM image. Bottom: AFM morphology and current map of the selective area deposition of MoS_2 grown (CVD) inside patterned Al_2O_3 trenches. Scalebar is 1 µm.

In summary, we have presented a transformative method for performing electrical AFM modes that eliminates the need for physical back-contact. By replacing conventional ohmic connections with a remote, reconfigurable e-beam, we remove the primary obstacle to non-destructive nanoscale characterization. We have demonstrated that this approach is versatile across a wide range of materials and fully fabricated device structures. A key highlight of this work is the application to fully integrated 3D NAND structures, where EB-AFM successfully probed vertical poly-Si channels that were otherwise electrically isolated. This capability reduces sample preparation complexity and enables a "correlative metrology" workflow that combines structural and electrical analysis for multiple types of FA applications. Given the ubiquity of electron-beam systems in semiconductor manufacturing, we believe EB-AFM is a ready-to-deploy solution that can unlock electrical modes on a full-wafer scale, enabling in-line metrology applications without interrupting the chip manufacturing process flow.

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KEYWORDS

Scanning Probe Microscopy; Atomic Force Microscopy, Multi-probes SPM; Tomographic AFM; Reverse Tip Sample Scanning

Advances in 4D-STEM for Applications in Phase Analysis and Strain Engineering

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INTRODUCTION

The demand for faster data processing, faster signal transmission, greater storage capacity, and continuously decreasing power consumption is driving continuous development of new semiconductor devices. Achieving such performance improvements is dependent on increasing the density of the active elements and cutting the signal path in semiconductor devices. Consequently, the importance of scanning transmission electron microscopy (STEM) in the development and failure analysis of semiconductor devices has been growing since the introduction of advanced technology nodes, in which the deposited layers and dimensions of transistors became much smaller and more complex. Besides the morphological and elemental composition, structural and crystallographic properties of the individual device components are key for their function, performance, and energy efficiency. Accurate and repeatable assessment of these key characteristics is essential for the development of new and improved devices, optimization of their preparation process, and ultimately monitoring of the quality of their production. Recent developments of hybrid-pixel direct electron detectors with very fast readout speed and high dynamic range [1] have revived scanning electron diffraction measurements (4D-STEM) using nanobeam illumination as an efficient characterization technique of sample crystallinity and crystallographic properties at the nanometer scale.

ENABLING 4D-STEM FOR USE IN SEMICONDUCTOR INDUSTRY

New techniques and applications of 4D-STEM have been developed and have grown significantly in recent years [2]. The 4D-STEM datasets can be, for example, used for identification of the distribution of different phases in extracted samples and/or for segmentation of individual grains in crystalline phases based on their different orientations [3]. By carefully processing diffraction patterns acquired at the nanoscale, electron diffraction data can also be used to extract information about small variation in the crystal lattice due to strain, or electric and magnetic fields. The quality of acquired diffraction data, and consequently the accuracy and precision of the analytical results, can be substantially improved by beam precession that minimizes the effects of dynamical scattering in the data. However, the experimental setups based on the conventional TEM/STEM microscopes are complex and rather suited to the Academic environment and fundamental research. Throughput of 4D-STEM measurements and the accuracy of obtained results consequently often depend on the skills and experience of individual TEM operators. In contrast, analytical tools in the semiconductor industry depend on and require not only high accuracy, but also reproducibility, accessibility (ease of use), reliability, and fast time to results. The introduction of the new generation of fully integrated and highly automated analytical STEM instruments that are optimized for electron diffraction measurements with beam precession provides a viable analytical tool with high reliability, reproducibility, and accuracy of analytical 4D-STEM results [4]. Precise and fully automated microscope alignments and experimental preset settings assure optimal and reproducible experimental conditions regardless of the operator and maximize the achievable accuracy, precision and spatial resolution of conducted 4D-STEM measurements.

Quantitative Phase Analysis of Polymorphic Thin Films

Polymorphic thin films such as MoS_2, HZO, AZO, are widely used as channel material in ferroelectric thin-film transistors (TFTs) to alter the channel carrier density through the transformation in ferroelectric polarization. In the preparation process, the thin layers are deposited in the monoclinic phase and then transformed into the desirable ferroelectric phase. Beam precession enhanced 4D-STEM measurements enable quantitative phase analysis of these thin layers to assess the fraction of different phases and grain size distribution despite the similarity in the elemental composition and lattice parameters. Using the approach of automated crystallographic orientation mapping [5], acquired diffraction patterns from each pixel in a scanned region of interest are compared with a set of pre-calculated diffraction patterns (templates) of the expected phases in the sample using a template matching function. The best fitting template then determines the phase and orientation at each pixel. Such 4D-STEM analysis of a thin HZO layer is shown in Figure 1. The analysis revealed a sufficient fraction (~50%) of the desirable ferroelectric orthorhombic phase from a sufficiently large area (1200 × 80 nm) to provide statistically significant results [6].

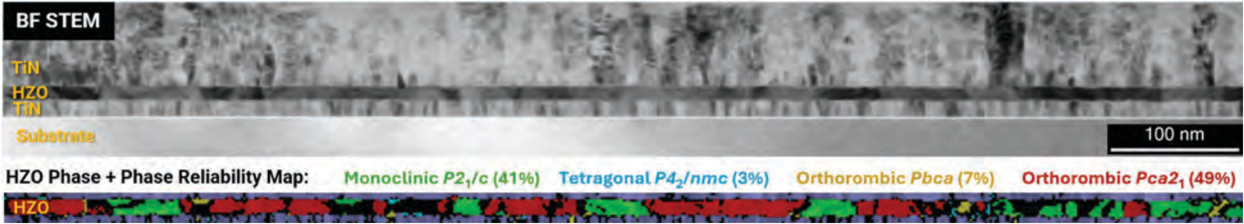

FIGURE 1. Bright field STEM image of a cross-section lamella of ~20-nm thin HZO layer (top) and corresponding phase map of the different HZO phases identified in the layer. The relative fractions of each phase in the layer are indicated in parentheses.

Characterization of Crystallinity in Complex Devices

Fast 4D-STEM measurements can also be used for characterization of complex devices, such as phase change memory modules. Selection of suitable virtual apertures provides deeper insight into the crystallinity of materials in the analyzed device [7], which is only partly visible in the dark field STEM images (Figure 2). The virtual STEM image was reconstructed from an acquired 4D-STEM dataset using a circular virtual aperture (red circumference) that is shown for a representative diffraction pattern from one pixel (inset). Full phase analysis of multiple crystalline and amorphous phases then gave the full picture of the composition and internal structure in the device. Specifically in this example, separation of atomic Germanium from the GST layer was revealed, as well as partial amorphization in some of the connecting vias. Moreover, a defect in one of the PCM segments was uncovered and manifested by increased amorphization around the GST layer at the interface with a heater module. High speed of data acquisition (~5 minutes) and fast data analysis (~15 minutes) make this technique viable for routine usage in physical failure analysis labs.

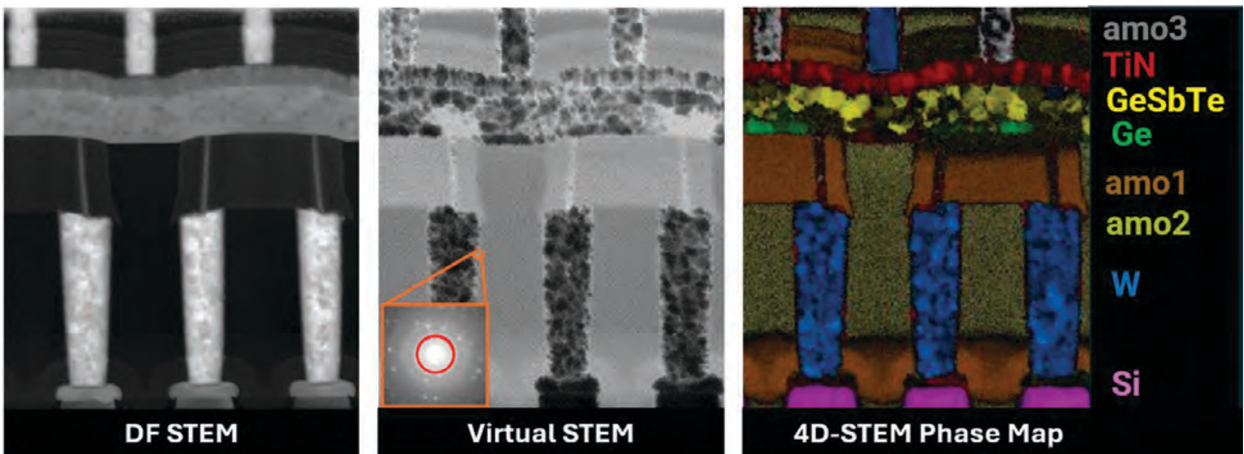

FIGURE 2. Dark field STEM image (left) shows the morphology of the analyzed PCM device. The virtual STEM image (middle) exposes grains of the crystalline phases in the device and highlights the different amorphous regions. The 4D-STEM phase map (right) reveals segments of five crystalline and three different amorphous phases in the device as labeled on the right.

Routine Strain Analysis in Advanced Technology Nodes

Strain engineering is essential for achieving high performance in advanced technology nodes (FinFET) by increasing carrier transport in the silicon channel since their introduction in the 2010s [8]. As the transistor dimensions continue to shrink and their 3D architecture becomes more complex (NS GAA), channel strain engineering becomes increasingly challenging due to the reduced volume of SiGe in the S/D region. Nanoscale strain measurements have therefore become crucial for validating theoretical models in the development of new and improved transistors [9]. Utilization of beam precession is essential for accurate and precise strain measurements in analytical STEM to suppress the deteriorating effects of dynamic scattering. The improved quality of diffraction patterns then allows for accurate determination of both tensile strain in GeSi stressors and induced compressive strain in gate channels despite interfering signals from other crystalline metals in the gates (Figure 3). Additionally, we examined effects of beam precession alignments as well as scan speed and specimen drift on the accuracy and spatial resolution of 2D strain maps and profiles obtained by precession-assisted 4D-STEM to evaluate suitability of this approach for strain analysis in future advanced technology nodes.

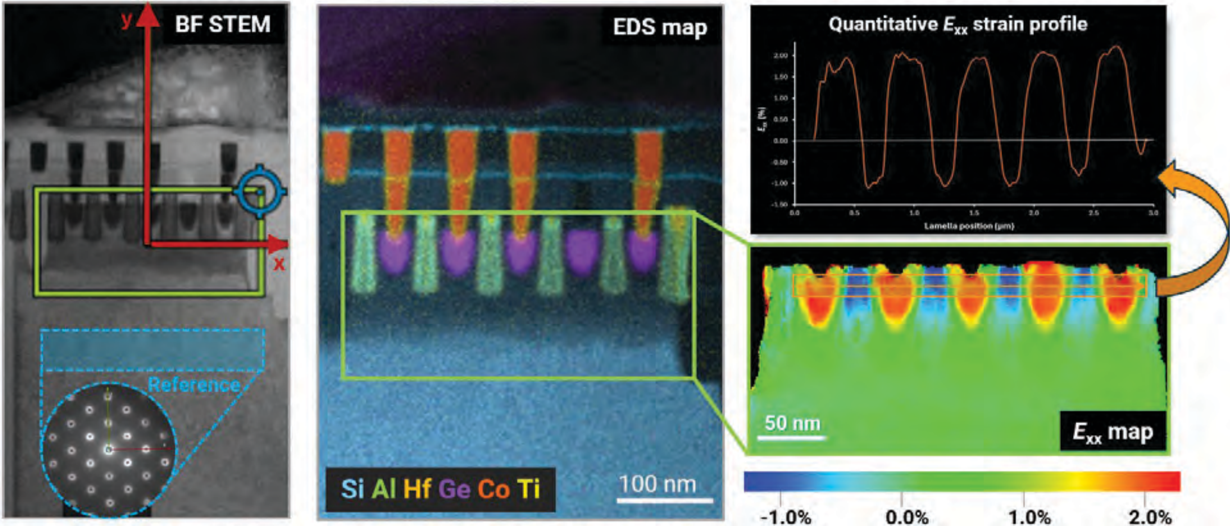

FIGURE 3. Bright field STEM image (left) and EDX elemental map (middle) of a 5-nm FinFET circuit cross-section showing multiple gate channels, SiGe stressors, and connecting vias. A broad region of silicon in the substrate (blue rectangle) was used for obtaining a reference diffraction pattern (blue inset) for the calculation of 2D strain map in the region of interest (right).

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KEYWORDS

Electron microscopy, 4D-STEM, beam precession, crystallinity, phase-orientation mapping, strain analysis

Harnessing the extreme ultraviolet for critical dimension metrology

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INTRODUCTION

The semiconductor industry has long adopted visible and ultraviolet wavelengths for optical critical dimension (OCD) measurements. Decreasing feature sizes, increasing architecture complexity, and troublesome parametric correlations all motivate approaches leveraging shorter wavelengths into the vacuum- and extreme-ultraviolet (VUV, EUV) spectral regions. Straightforward extendibility of established OCD techniques from the visible range into these vacuum wavelengths is greatly hampered by absorption. We review the initial and developing efforts to utilize these vacuum wavelengths for model-based measurements of CD, often labeled "EUV scatterometry" in the literature. The predominant mode for EUV-based CD metrology is diffraction, while our group at the National Institute of Standards and Technology (NIST) is pursuing both EUV diffractometry and spectroscopic ellipsometry at VUV and EUV wavelengths. Current progress will be presented in the context of a gaps analysis of EUV scatterometry for near-line and in-line process control.

OPTICAL SCATTEROMETRY AND EUV SCATTEROMETRY

The terms "scatterometry" and "OCD" (for optical critical dimension metrology) are now practically interchangeable. Nigel Smith defined these at FCMN 2024 as the "non-destructive optical measurement of many dimensional parameters of interest for semiconductor process control…based on either single-wavelength or spectral ellipsometers with a very narrow range of incident angles."[1] This consensus definition of scatterometry has evolved with its underlying technologies. At one time, an "optical scatterometer" was a reflectometer outfitted with an array of detectors to capture diffused light [2]; experts in that methodology recognized that one could capture diffraction patterns off periodic patterned gratings. Later, industrial measurements could be optimized by positioning photodiodes to the angular positions of diffraction orders [3], then further improved using the spectroscopic 0th order reflection with analysis of changes in polarization state, *i.e.*, ellipsometry [4]. As metrology challenges increased with decreasing feature size, industrial applications of full Mueller matrix spectroscopic ellipsometry (MMSE) also emerged [5] which also exploits depolarization. Improvements in the application of optical techniques led to the optical scatterometry employed today by this industry as the workhorse of nondestructive metrology.

When considering the extendibility of optical techniques to shorter wavelengths, two key questions emerge. First, what is "EUV scatterometry?" The initial report in the literature of EUV scatterometry came from synchrotron-based experiments of EUV masks, a work that defined scatterometry as "the analysis of light diffracted from a periodic structure".[6] Laboratory experiments utilizing high-harmonic generation (HHG) for producing EUV wavelengths followed, with some research groups measuring masks [7] and others measuring gratings.[8] These types of experiments have been repeated as lithographic technology has improved. A notable recent effort [9,10] seeks to commercialize diffraction in the 10 nm to 20 nm range, which overlaps the soft-x-ray (SXR) region and is thus termed

"SXR Scatterometry". Our team at the National Institute of Standards and Technology (NIST) has recently reported our collaborative diffraction experiments with the University of Colorado-Boulder [11] in 2025; we will defer from repeating the results here.

A second question is whether it is possible to perform industrial scatterometry (spectroscopic ellipsometry, or SE) at EUV wavelengths. Our NIST project team is also leveraging NIST's Synchrotron Ultraviolet Radiation Facility (SURF-III) to test a new NIST-patented [12] concept for performing Mueller matrix spectroscopic ellipsometry (MMSE) at these shorter wavelengths. Our two-pronged approach (diffractometry, SE) allows NIST to develop world-class laboratory diffraction methods for semiconductor metrology while also extending SE capabilities down to 10x shorter wavelengths.

EXTENDING SPECTROSCOPIC ELLIPSOMETRY TOWARDS THE EUV

At time of abstract submission, we are preparing for our initial demonstration of an ultrahigh-vacuum-compatible spectroscopic ellipsometer using SURF-III. Thus far, we have fabricated its optical and sample manipulation instrumentation as shown in Fig. 1(a). The polarization stage generator (PSG) and polarization state analyzer (PSA) are four-bounce chevrons, with piezoelectric motors rotating the PSG and PSA at proportional speeds. The PSG and PSA each contain four Si blanks, which should yield both sufficiently broadband reflections and modifications of the incident linear polarization state in the 50 nm to 150 nm wavelength range.

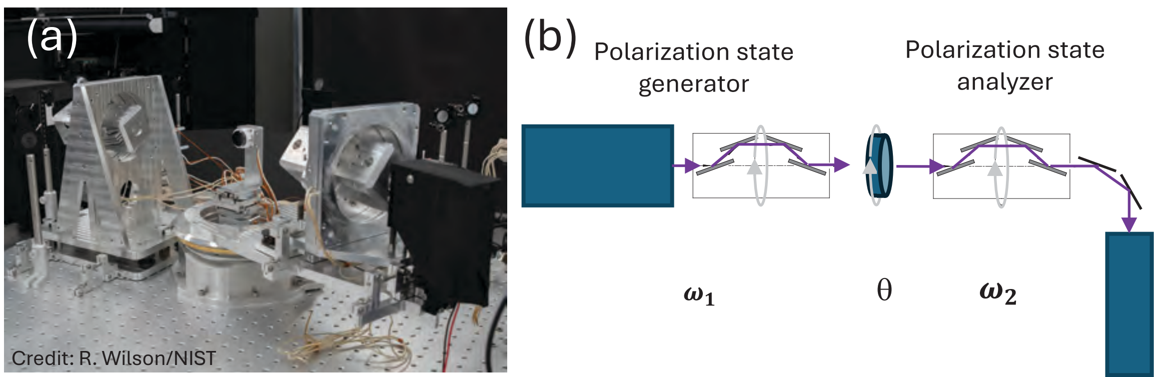

FIGURE 1. (a) Newly constructed UHV fully reflective spectroscopic ellipsometer (SE) tested on an optical bench prior to synchrotron experiments. (b) Schematic of initial experiment with a quarter-wave plate (QWP).

Our confidence in this equipment prior to these synchrotron experiments is based upon tabletop testing using a 266 nm wavelength laser. Figure 2(a) shows the ellipsometry signal for a quarter-wave plate (QWP) at four different QWP rotation angles (θ) and a straight-through measurement. Figure 2(b) shows the ellipsometric quantities (N,C,S) identified correctly for a QWP.

Known challenges for the SURF-III experiments we will address include beam size control, normalization of synchrotron output, and filtering of 2nd order light from the monochromator. We will discuss upcoming steps to demonstrate the technology on an EUV high-harmonic generation source (HHG) using more industrially relevant targets. We will compare the extensibility of EUV diffractometry and EUV spectroscopic ellipsometry for higher throughput as needed by the industry.

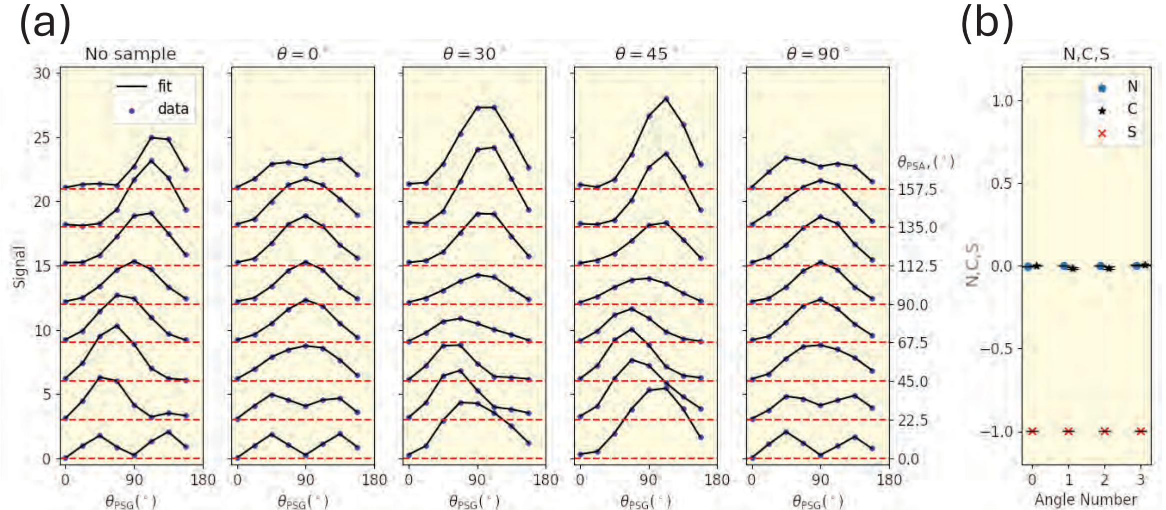

FIGURE 2. (a) Measurement signal with fitting for the QWP experiment at 266 nm wavelength, varying the QWP rotation. Data at varying values of θ_{PSA} are offset for clarity. (b) Fully reflective SE qualitatively identifies the ellipsometric quantities (N,C,S) correctly. Systematic errors were treated nonparametrically as in Ref. [13], with care to avoid parameter confounding.

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KEYWORDS

Extreme ultraviolet, scatterometry, diffractometry, spectroscopic ellipsometry, vacuum ultraviolet

Hybrid Metrology for Hot Spot Prediction in Post-Etch Patterning

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ABSTRACT

Extreme ultraviolet lithography has enabled the semiconductor industry to continue on the long-term path of patterning shrink. Impressively, the industry is now approaching the atomic scale, where the quantized nature of light and materials is becoming a very significant limiter to the ultimate performance of the patterning process. While stochastics on the photoresist side has justifiably attracted much attention over the past few years, stochastic processes also have important implications on EUV mask characteristics which in turn ripple down to observed patterning stochastics including effects such as line-width roughness and contact hole critical dimension uniformity problems. It will be shown that, fundamentally, these problems arise from phase stochastics on the mask and that only actinic metrology is directly sensitive to these effects. In the second half of the presentation, focus will be turned to applying these same actinic scattering metrologies to the characterization of indented EUV phase shift structures instead of the undesired stochastic phase noise discussed above. In this section, the sensitivity of the EUV phase shift mask to various critical parameters such as wavelength, illumination angle, and pitch is explored. These effects are used to highlight some of the challenges and constraints in the application of phase shift masks in the EUV regime.

Advancing Metrology for High Aspect Ratio Structures: Lam Research's Journey with CDSAXS

Jin Zhang

Lam Research

TBD

Impact Assessment of In-line SIMS Utilization on Logic Device Performance

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INTRODUCTION

The high-resolution compositional depth profiles generated by In-line secondary ion mass spectrometry (In-line SIMS) in Logic device manufacturing provide invaluable process insights inaccessible through other techniques available in a fab environment [1]. The technology brings additional benefits to the table such as fast turnaround time, reduced scrap, and increased yield. However, concerns have been raised regarding the potential impact on product wafers due to sputtering.

To address these concerns, an in-depth analysis was conducted to thoroughly understand and evaluate the potential contamination and performance-impacting defects arising from ion sputtering on product wafers for Advanced Logic.

The analysis included assessments such as post-SIMS particle inspection, crater fill, and planarization prior to lithography, in-line electrical tests to evaluate transistor performance, and surface roughness characterization as a function of sputter direction.

In this presentation, we will share detailed results and observations from our analysis. We will demonstrate how in-line SIMS analysis on product wafers does not impact device reliability or performance and hence is suitable as an in-fab metrology technique.

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KEYWORDS

SIMS, contamination, in-fab metrology, in-line, product wafer

High Speed AFM as an Enabling Technology for Next Generation Semiconductor Devices

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The in-line metrology requirements for advanced semiconductor manufacturing become ever more rigorous with each generation of devices. To meet these requirements, the 'ideal' metrology tool would have lateral and vertical resolution of well below 0.1 nm, large area scanning capability and a throughput (pixel rate) sufficiently high to offer a cost – effective in – line solution.

Optical, Electron Beam and X-Ray based metrology methodologies offer good solutions for various applications but generally lack the highly desirable capability of simultaneous high vertical and lateral resolution. AFM has emerged as a solution for some applications and has begun to be used for in – line metrology in HVM, with tens of systems installed worldwide. Early manifestations of AFM, however, were limited to relatively small area scanning at low speed, limiting the application space, and lacked automation features required in manufacturing.

This paper will describe an automated AFM system that combines a large imaging area with an extremely high pixel rate, high spatial resolution and a very low noise floor. Automation features such as large area mapping and long-range linear profiling will be described. Data will be shown from the use of such a system for critical metrology challenges including Copper Hybrid Bonding for Advanced Packaging and Cell Stacking, CMP pre – litho evaluation, After Develop EUV measurement, After Etch measurement and others. Lastly, future developments will be discussed.

Multibeam inspection tool development for detecting below 10 nm physical defects

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INTRODUCTION

With High-NA-EUV lithography expected to be introduced in mass production in the coming years, and the evolution of 3D structures in logic and memory devices, the defect size that must be inspected in process control for high-volume manufacturing (HVM) of semiconductor devices is becoming increasingly smaller. The number of complex defects, such as embedded defects, is expected to increase, and the requirements for defect inspection processes are becoming more stringent year by year.

For defect inspection of critical defects below 10 nm, conventional optical defect inspection tools (Bright field), which have been utilized over years by adding advanced algorithms, are reaching their limits. As a result, there is growing demand for the development of high-speed electron beam inspection tools [1]. Under such circumstances, multibeam inspection tools are being developed. However, due to their complex optical systems, it's hard to achieve the same resolution and sensitivity as single-beam systems. Therefore, instead of utilizing its high resolution for inspection, the initial validation focuses on applying these tools to voltage contrast (VC) inspection with a relatively large pixel size, which is expected to achieve higher throughput [2].

Hitachi High-Tech (HHT) has developed a multibeam inspection tool using a column developed by Carl Zeiss MultiSEM GmbH [3]. Leveraging its high-resolution capability, achieving up to 3.5 nm resolution, physical defect inspection (PDI) targeting 6 nm programmed defects (HHT standard wafer) was conducted. In this study, the inspection results from several types of inspection algorithm such as die-to-die (D2D) of those smaller defects, the correlation between defect detection rate and inspection parameters such as pixel size, and the advantages in throughput will be introduced.

METHODOLOGY

For the basic study of physical defect inspection by the multibeam tool, a HHT standard wafer was fabricated using a mask that contains protrusion patterns at the line edges of a line and space pattern. There are edge-extension -types of programmed defects with size distribution depending on the protrusion pattern size. The CD-SEM measurement results of the edge-extension-type of programmed defect sizes for the pattern in Group 1 to 3 are summarized in Table 1. In a measurement of the defect size, a total of 16 chips were measured for each group, and

TABLE 1. CD-SEM measurement results of the edge extension type of programmed defect size formed in Group 1 to 3.

	Group 1	Group 2	Group 3
Average defect size	6.24 nm	9.02 nm	11.8 nm
Min. defect size	2.28 nm	4.68 nm	7.23 nm
Max. defect size	12.1 nm	17.0 nm	19.8 nm
STD deviation	1.38 nm	1.54 nm	1.58 nm

the size of 4,000 defects was measured on average. These results indicate that sub-10 nm defects were successfully formed as planned, and a sufficient number of defects were fabricated to statistically evaluate defect inspection performance of the multibeam tool.

Basically, multibeam tools are expected to realize high-speed inspection of smaller defects below 10 nm that are hard to detect using conventional optical inspection tools. In this study, SEM images were acquired with different optical conditions such as pixel sizes and scan frequencies. Table 2 shows representative test conditions selected from those tested in this study, along with a description of detection difficulty and throughput, which are related to optical conditions. SEM images captured under each optical condition are included in this table. These are raw images as captured, with no image processing applied. To evaluate the performance of the multibeam tool, it is necessary to set a large pixel size in order to achieve high throughput. However, there is a concern that with a large pixel size, it may be difficult to detect smaller defects. Nevertheless, even when the pixel size is in the same order as the defect size, it is theoretically possible to detect defects if there is a contrast difference across several pixels in the horizontal and vertical directions.

TABLE 2. Representative test conditions conducted in this test, along with a description of detection difficulty/ throughput and acquired SEM images.

Pixel size(nm)	2		5		10	
Image resolution	6000 x 5200		2400 x 2080		1200 x 1040	
Scan frequency (MHz)	10	80	10	80	10	80
Images captured by multi-beam SEM						
Detection difficulty	Easy					Difficult
Throughput	Slow					Fast

In this study, defect inspections using several algorithms such as Die-to-Die(D2D), Trainable Die-to-Die(T-D2D) and Cell-to-Cell(C2C) were conducted. In the D2D algorithm, the same location on adjacent dies is used as the reference. The C2C algorithm is applied to the inspection of devices with periodic patterns, such as memory, where adjacent periodic patterns are used as reference images. By using these algorithms, the defect inspection is executed by comparing the pixel-by-pixel gray level differences between the reference image and the actual inspection image. When capturing images with a large field of view (FOV), as in the case of a multibeam tool compared to a single-beam tool, there is a possibility that factors such as distortion, which degrade image uniformity, may reduce the robustness of inspection results. To reduce such negative factors, inspections using the T-D2D method was conducted in parallel. By applying machine learning to multiple acquired SEM images, a reference image that minimizes image non-uniformity caused by distortion as much as possible was generated. The inspection is then performed by comparing the gray levels between this predicted reference image and the actual inspection image. C2C performs inspections by using identical patterns within the same field of view (FOV) as reference images. However, if there is image non-uniformity within the FOV as mentioned earlier, it may lead to issues in the inspection results.

RESULTS AND FUTURE WORKS

In this study, we performed SEM imaging under different optical conditions with the HHT standard wafer containing programmed defects of sufficiently small size. Inspections were then carried out using several algorithms. Specifically, for the pattern Group 2 containing 9 nm defect on average, we conducted a D2D inspection on images captured at 2 nm/pixel and a scan frequency of 10 MHz, achieving a sufficiently good recall rate of 97.7%. However, under these imaging conditions, the throughput is limited to less than 50 mm^2/h. Therefore, comparisons of inspection results under higher throughput conditions and with other algorithms will be presented at the conference.

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KEYWORDS

Multi-beam, Physical defect inspection, Die-to-die inspection

Workflow Automation For High Volume TEM Data Production

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INTRODUCTION

Modern semiconductor process development and production are driving the demand for atomic-scale transmission electron microscopy (TEM) data to new heights. Critical features on the latest generation memory and logic devices have shrunk below the ability of SEM-driven conventional metrology techniques, requiring significantly more resolution to provide process feedback.[1] Addressing the challenge of rapidly scaling TEM laboratory operations while maintaining high efficiency and productivity is crucial. The Thermo Scientific Vulcan Automated Lab (VAL) offers a comprehensive, scalable solution for addressing the challenges of modern TEM data production, ushering in a new era of atomic-scale data acquisition. The Vulcan Automated Lab features a seamlessly connected, AI-powered TEM metrology workflow, bridging the gap between the lab and the fab. This innovative system enhances productivity by delivering high-volume data of exceptional quality while reducing operator burden through advanced on-tool automation, materials handling automation, and continuous data connectivity.

WORKFLOW SOLUTION

The Vulcan Automated Lab builds upon Thermo Fisher's existing portfolio of semiconductor sample preparation and imaging instruments to enable automated material handling and logistics for wafers, individual sample die, and TEM samples. Vulcan Automated Lab integrates a SEMI E177 complaint TEM grid (Lamella Carrier) EFEM to enable automated handling of TEM samples for preparation and imaging instruments. The integrated EFEM allows for full traceability of samples throughout the prep and imaging workflow. Traditional TEM data production relies on significant manual intervention in both operation of the instruments set as well as moving samples between tools to produce the final dataset. Automation of data and material handling enables sampling of nanoscale structures in the S/TEM without the requirement of operator presence, at statistically significant volumes required for modern devices.[2]

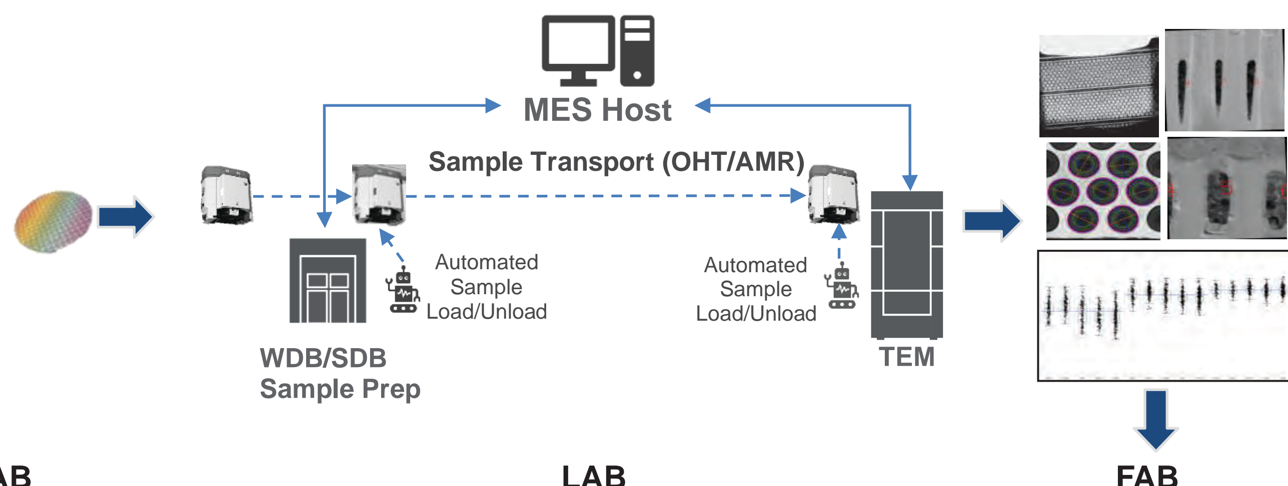

FIGURE 1. Workflow elements in the Vulcan Automated Lab.

When selecting/preparing a region for cross-sectional imaging in the S/TEM two figures of merit are used to describe the physical characteristics of the sample production process: Lamella Centering Accuracy (LCA) describing the measurement of the target feature relative to the center of the produced lamella, and Lamella Thickness Accuracy (LTA) relating the overall lamella thickness variation in the region of interest.

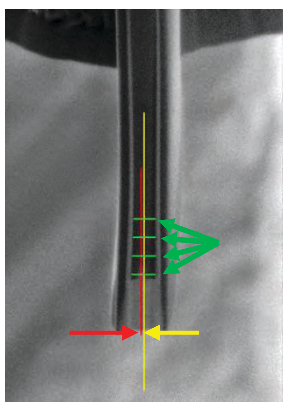

FIGURE 2. Cross-section image of a TEM lamella showing LTA (green) and LCA (yellow-red) measurements

Historical approaches to cut placement relied on passive control of the cut face, where the milling system is aligned, a cut is called for, and the resultant cut face incorporates both placement error and any subsequent drift that occurs during the mill. The combination of cut face inaccuracy on both sides of the lamella contribute to both LCA and LTA error. These placement and thickness errors in turn have implications for the maximum allowable thickness to ensure the full removal of any neighboring obscuring material.[3] Vulcan Automated Lab introduces active cut face control during sample preparation steps to reduce LCA and LTA figures, allowing better control of sampling volume needed for smaller process geometries. Active, AI-guided endpointing has demonstrated significant improvement in cut placement control and associated LCA/LTA figures compared to historical capabilities.

TABLE 1. Typical Cut Placement Capabilities for TEM sample preparation

Preparation Method/System	Typical LCA	Typical LTA
Manual Sample Preparation on Helios EXL	6nm, high operator dependance	6nm, high operator dependance
ExSolve G2 Automated TEM Sample Preparation	<4.4nm	<3.6nm
Vulcan Active Endpointing	<2nm	<2nm

Fully automated, AI-driven sample preparation has been demonstrated down to <18nm final thicknesses with automated endpointing at lowkV FIB polishing steps on both memory[4] and logic devices. In addition to overall process performance, high levels of process automation improve data reliability and mitigation of human errors. [5]

CONCLUSION

The Thermo Scientific Vulcan Automated Lab represents a significant advancement in the field of atomic-scale transmission electron microscopy (TEM) data acquisition. By integrating AI-driven automation and advanced materials handling, Vulcan Automated Laboratory addresses the critical challenges of scaling laboratory operations while maintaining high efficiency and productivity. The seamless integration of automated sample preparation,

imaging, and data traceability enhances lab productivity and enables scalable data production for modern semiconductor manufacturers.

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KEYWORDS

Automated, Workflow, Sample Preparation, TEM, process control, TEM metrology, Machine learning, Material Handling

Combined Acoustic and X-Ray Microscopy for Advanced Packaging Metrology and Defect Inspection

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INTRODUCTION

The rapid evolution of advanced packaging technologies, including hybrid bonding, poses significant challenges for metrology, defect inspection, and physical failure analysis. These challenges stem from increasing complexity, shrinking feature sizes, the heterogeneous integration of ICs, and chiplet architectures, which together demand high-resolution, high-throughput, and preferably nondestructive analytical techniques. To meet these requirements, innovation in microscopy techniques and associated workflows is essential, particularly when balancing data and image acquisition speed with achievable spatial resolution [1].

Developing next-generation analytical tools that address vertically stacked dies, dense interconnect structures, and novel materials is a key task for engineers at universities, RTOs, and equipment manufacturers. In this context, nondestructive imaging workflows that combine complementary techniques - delivering both high throughput and high resolution - are particularly attractive to the semiconductor industry. Such workflows must rapidly identify critical defects at the wafer- or package-level and then characterize them in 3D with high resolution.

SCANNING ACOUSTIC MICROSCOPY AND X-RAY MICROSCOPY

Scanning acoustic microscopy (SAM) remains the tool of choice for assessing interfacial integrity, including delamination, and for detecting defects such as voids and cracks in bonded wafers [2]. The method provides information on subsurface discontinuities in materials and systems, and its scan speed is significantly higher than that of high-resolution X-ray computed tomography (XCT), making SAM particularly suitable for initial screening and high-throughput inspection. However, conventional SAM faces fundamental limitations when applied to 3D-stacked dies and chiplets with high-density submicron interconnects. One limitation is the trade-off between penetration depth and lateral resolution: highly penetrating low-frequency acoustic waves cannot achieve the spatial resolution required for advanced packaging technologies, where resolutions of 500 nm or below are needed for fault isolation and defect inspection in high-density sub-micrometer interconnects. In addition, signal convolution from various die interfaces along the acoustic path complicates selecting the correct signal from the interface of interest, making it difficult to render an accurate image of specific buried interfaces. These challenges have motivated several beyond-state-of-the-art approaches in acoustic microscopy. We will demonstrate the detection of voids in through-silicon vias (TSVs) using a new GHz-SAM technology [3]. In this approach, SAM interferometry is used, in which a defocused sound field induces surface acoustic waves that, in turn, generate unique interference patterns associated with the quality and integrity of each TSV. These interference patterns can be analyzed to distinguish between good and defective TSVs. Furthermore, a fully automated, highly efficient end-to-end convolutional neural network (CNN) model is used to classify thousands of TSVs and to provide statistical information about defect distributions and process stability. This combination of advanced SAM concepts and AI-based data analysis significantly increases throughput and reliability in defect classification [4].

X-ray microscopy and high-resolution XCT are well-established failure analysis (FA) techniques for visualizing defects in metal interconnects and package structures, such as TSVs, copper pillars, and solder microbumps [5,6]. Nevertheless, their application is constrained by trade-offs between image quality and scan throughput, owing to limitations in source brilliance, optics efficiency, detector performance, and data-processing speed. In addition, state-of-the-art laboratory nano-XCT requires destructive sample preparation, such as thinning the silicon to approximately

50 µm, to achieve the desired spatial resolution and contrast. High-resolution imaging of voids in Cu-TSVs and AgSn microbumps, obtained with conventional nano-XCT after such thinning, will be shown. To extend nondestructive 3D imaging to sub-500 nm and even sub-100 nm defect sizes in advanced packages, further development of micro-XCT and nano-XCT techniques is needed. A key requirement is to significantly reduce image acquisition time without sacrificing spatial resolution or contrast, which necessitates high-brilliance laboratory X-ray sources and advanced detector systems. In parallel, AI algorithms for image reconstruction and denoising, as well as for automated defect detection and classification, are indispensable for imaging large-form-factor objects (dies and wafers) and for high-speed data processing. We will demonstrate for solid–liquid interdiffusion (SLID)-bonded $Cu/Cu_6Sn_5/Cu$ interconnects that destructive sample preparation steps for nano-XCT are not needed in the hard X-ray regime - i.e., at photon energies greater than 10 keV [7]. This enables truly nondestructive 3D imaging of interconnect structures and defects in 3D-stacked dies.

NONDESTRUCTIVE WORKLOW FOR DEFECT INSPECTION AND ANALYSIS

A major development goal is to establish new nondestructive workflows compatible with semiconductor manufacturing requirements. Such workflows should combine a high-throughput technique that identifies regions of interest (ROIs) - for example, scanning acoustic microscopy (SAM) or quantum diamond microscopy (QDM) - with a high-resolution 3D imaging technique such as nano-XCT. In this way, the strengths of each method can be exploited: rapid defect detection and localization on the one hand, and defect analysis or detailed structural analysis on the other.

We will present a concept for a seamless workflow for advanced package FA and defect inspection that combines acoustic and X-ray techniques to detect and classify defects automatically, thereby improving both throughput and defect detectability [8]. One potential example, illustrated in Fig. 1, is a seamless, nondestructive workflow for defect inspection in hybrid bonding. In this workflow, SAM is used first to scan the entire wafer or package and identify ROIs that may contain buried defects, such as delamination, voids, or microcracks at bonding interfaces. Owing to its high scan speed, SAM provides an efficient pre-screening step that narrows the areas requiring more detailed investigation. Within the selected ROIs, nano-XCT is then applied to visualize defects with high spatial resolution.

SAM can be integrated into a nondestructive workflow for wafer-level inspection, followed by local, high-resolution 3D imaging. As discussed above, conventional SAM techniques are limited by trade-offs between penetration depth and resolution, and by signal convolution from multiple interfaces, which restrict their applicability to 3D-stacked chiplets with high-density sub-micrometer interconnects. Beyond-state-of-the-art approaches, particularly GHz-SAM, address these challenges by providing enhanced resolution and improved depth discrimination. The use of SAM interferometry and AI-based classification of TSVs demonstrates how acoustic methods can be extended to meet the demands of advanced packaging technologies.

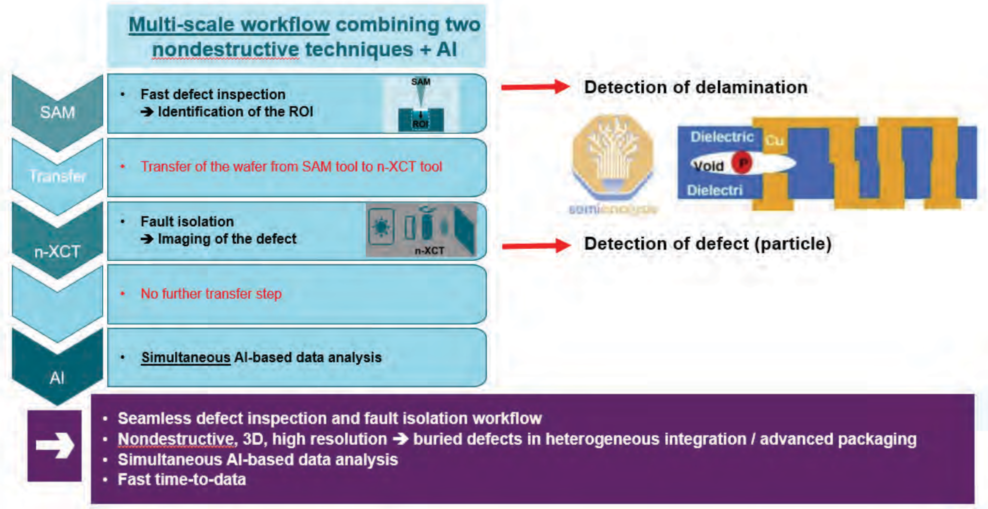

FIGURE 1. Nondestructive workflow for buried defect detection, combining SAM and nano-XCT, for hybrid bonding technology [8].

For the X-ray imaging in the workflow, it is essential to perform nano-XCT in the hard X-ray regime at photon energies above 10 keV to avoid destructive sample-preparation steps while still achieving high contrast and resolution in buried structures. This capability is particularly important for imaging defects in dies or packaged systems, where cross-sectioning or thinning would be unacceptable in an industrial environment. The combination of SAM and nano-XCT in a unified workflow enables automated defect detection and classification, as well as quantitative analysis of defect types, sizes, and spatial distributions.

In this paper, complementing several existing reviews that focus on micro- and nano-XCT and extending them to quantifying reconstruction quality, the typical industrial applications of high-resolution XCT are analyzed, structured, and classified into three main categories: (1) structure analysis, (2) flaw detection, and (3) reliability engineering [8]. These application categories have different requirements for the accuracy of the 3D reconstruction and for the time-to-data. Limitations in available time or computing resources may require algorithm optimization and parameter tuning, which can affect accuracy and, therefore, make accuracy assessment a key task.

CONCLUSION

New developments and innovations in metrology and inspection will enable the semiconductor industry to control critical process steps and identify defects faster and with higher accuracy than before—an urgent requirement for chiplet architectures with high-density sub-micrometer 3D interconnects. New metrology solutions will support the development and ramp-up of advanced packaging technologies, characterized by further feature shrinking and the integration of novel materials, and will contribute to continuous yield improvement. The EDFAS roadmap addresses the need to improve the resolution of 2D and 3D X-ray imaging to the sub-micrometer level to reliably detect and classify defects in interconnects and at hybrid bonding interfaces [1].

Significant efforts remain before X-ray techniques can be fully integrated into production lines and before inspection of high volumes of heterogeneously integrated chiplets becomes routine. One important aspect is the integration of AI and machine learning (ML) algorithms into metrology and inspection tools, which enables dynamic adjustment of measurement protocols (e.g., by monitored tomographic reconstruction [9]), reduces data acquisition time, and supports corrective actions in the manufacturing process before yield is affected. This new approach will have important implications for risk mitigation strategies in the semiconductor industry.

Advanced workflows for process monitoring and accurate, efficient defect detection and classification in the semiconductor industry will integrate multiple analytical techniques with varying spatial resolutions and throughput, complemented by advanced data analysis using AI and ML. For advanced packaging, and particularly for hybrid bonding technology, a seamless workflow for defect inspection that combines acoustic and X-ray techniques to detect and classify defects automatically - thereby improving throughput and defect detectability - is proposed.

The accuracy of 3D information obtained from nano-XCT of opaque objects depends on acquisition parameters - such as the number of projections and the data acquisition time per projection - as well as on data analysis methods, including the use of deep convolutional neural networks for denoising and artifact mitigation. Continuous improvements in these areas are crucial to meet the stringent requirements of semiconductor manufacturing and advanced packaging. The adoption of high-resolution X-ray imaging techniques in the semiconductor industry is driven by the need to detect flaws in advanced micro- and nano-structured materials and in high-tech products manufactured using nanotechnologies.

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KEYWORDS

Scanning acoustic microscopy, X-ray tomography, X-ray microscopy, advanced packaging,

Wednesday, March 18

Spectrum-to-structure Hybrid Metrology: SEM Referenced Model Guided M/L of 3D Profiling from SE and Xray Signals

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TBD

Hybrid Metrology Assisted by Machine Learning at Nanometer Scale

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INTRODUCTION

The device miniaturization challenge in microelectronics leads to critical dimensions and three-dimensional profiles reaching nanometer and sub-nanometer scales. At these dimensions, measurement accuracy is increasingly affected by instrumental artifacts, probe–sample interactions, and model assumptions. Reliable estimation of critical dimension (CD), pattern height, and sidewall angle (SWA) is therefore a major challenge for process monitoring and control. Conventional metrology techniques such as AFM, CD-SEM, scatterometry, and CD-SAXS provide complementary information on structures but suffer from intrinsic limitations when used independently [1-3]. To overcome these limitations, hybrid metrology has emerged as an approach that combines multiple techniques within a coherent framework [1]. More recently, machine learning methods have been introduced to enable efficient fusion of heterogeneous metrology data [6]. However, their deployment is limited by the scarcity of experimental, traceable datasets, which motivates the use of simulated data for training purposes.

STATE OF THE ART AND POSITIONING

CD-SEM is one of the most widely used techniques of inline process control due to its high throughput and repeatability. However, it is difficult to reach a sensitive information on height and SWA parameters [3]. AFM provides accurate three-dimensional measurements and serves as a reference technique for calibration and validation, but it suffers of a limited throughput. Indirect techniques such as scatterometry offer fast, non-destructive measurements but rely on inverse modeling that may suffer from ambiguities and parameter correlations [2]. CD-SAXS has emerged as a powerful indirect technique, offering enhanced sensitivity to three-dimensional profiles and buried interfaces while remaining non-destructive and insensitive to charging effects [4,5]. However, like scatterometry, it relies on complex inverse problems and cannot be efficiently deployed alone in high-volume manufacturing. Hybrid metrology addresses these limitations by combining complementary techniques to improve accuracy and robustness [1]. Recent advances increasingly rely on machine learning to handle the growing complexity of multi-technique datasets [6]. In this context, physically based simulated datasets have become essential for supervised learning, particularly for scatterometry and CD-SAXS applications [5,8]. This evolution aligns with the IRDS 2024 recommendation [7], which highlights hybrid metrology as unavoidable for sub-10 nm dimensional control as schematized in Figure 1, and emphasizes its potential for uncertainty reduction and cost optimization

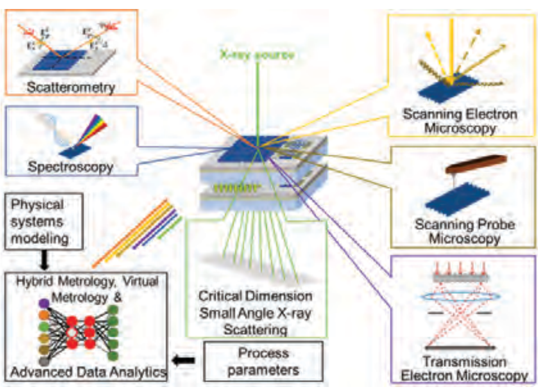

FIGURE 1. Hybrid metrology approach illustration (taken from 2024 IRDS Metrology)

NEURAL NETWORK ARCHITECTURE AND GEOMETRIC MODEL

The hybrid metrology framework is based on a parametric geometric model of a one-dimensional periodic line, defined by three key parameters: CD, height (H), and sidewall angle (SWA). These parameters provide a physically meaningful and sufficiently expressive description of the structures measured by the different techniques.

A multi-branch neural network architecture is employed as visible in Figure 2. The input data are the line shape parameters obtained from each technique, and the output data are the line shape parameters after hybridization. Each branch estimates separately the (CD, H, SWA) parameters, accounting for different sensitivities, uncertainties and other geometric parameters.

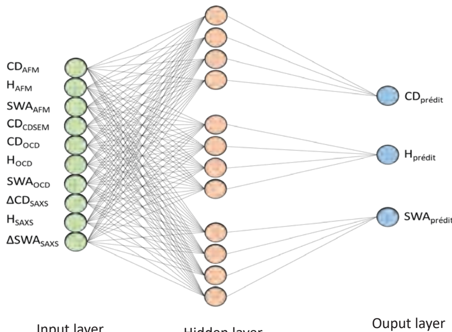

FIGURE 2. Multi-branch network architecture for hybrid metrology

The network architecture is selected using purely artificial datasets, enabling architecture optimization independently of experimental noise and instrumental variability. This design ensures physical interpretability and compatibility with metrological validation requirements.

PHYSICALLY REPRESENTATIVE SIMULATED DATA GENERATION

Simulated datasets are generated using physically based models to compensate for the limited availability of experimental training data. All simulations rely on the common geometric model defined by (CD, H, SWA). These datasets are built regarding some experimental samples of lines gratings with a range of parameter values : 30 nm $\leq$ CD $\leq$ 65 nm ; 20 nm $\leq$ H $\leq$ 100 nm ; 80 ° $\leq$ SWA $\leq$ 90 °. CD-SEM data are simulated using the Nebula software, which accounts for electron–matter interactions, secondary electron generation, and imaging conditions. AFM, scatterometry, and CD-SAXS simulations are performed using in-house tools which accounts model probe convolution effects, optical diffraction, and X-ray scattering physics, respectively. To further constrain the geometric model, transmission electron microscopy (TEM) measurements are used to obtain a high-resolution reference profile of the line structure. While not suitable for routine metrology, TEM provides essential information to validate the parametric model and ensure physical realism of the simulated model. The Figure 3.A shows the top and bottom corner rounding in the line shape. This is considered in the modeled profile as shown in the Figure 3.B.

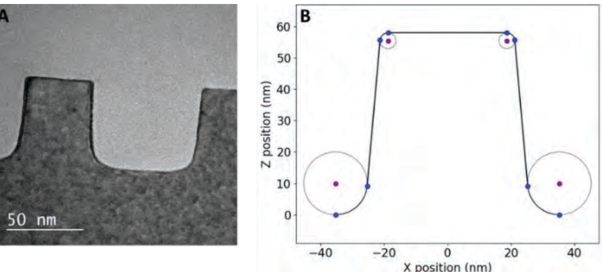

FIGURE 3. A: Line profile measurement with TEM and B: corresponding modeling profile

AFM measurements observation on experimental samples show dimensional variations between lines within the same grating. This variability is one of the sources of uncertainty in dimensional parameter measurements. It is therefore important to quantify these variations in order to model them. Based on these observations, we considered a modeling approach known as “multi-line.” This method allows the observed variations to be implemented directly into the geometric models, thereby impacting the raw data obtained after simulation.

UNCERTAINTY REDUCTION THROUGH HYBRID METROLOGY

Each metrology technique exhibits intrinsic limitations and parameter correlations when used independently. The proposed hybrid approach exploits complementary sensitivities and the correlations as an advantage to reduce the uncertainty. The multi-branch neural network acts as a data-driven regularization operator, learning the physical correlations between geometric parameters and measurement responses across techniques. Training on simulated datasets allows controlled exploration of the (CD, H, SWA) parameter space and implicit weighting of each technique according to its metrological relevance. As an example, for each technique a large number of simulated data are generated, allowing an uncertainty determination for these isolated techniques. These data are also used to train and validate the Neural Network. The obtained results exhibit reduced uncertainties compared to single-technique measurements as visible in Table 1.

Measurement uncertainties		CD	H	SWA
AFM	σ (std dev)	0,65nm	0,68nm	1,29°
CDSEM	σ (std dev)	0,91nm		
Scatterometry	σ (std dev)	2,05nm	0,92nm	3,49°
CD-SAXS	σ (std dev)	0,54nm	0,26nm	0,67°
NN prediction	σ (std dev)	0,35nm	0,47nm	0,43°

TABLE 1. Comparison of standard deviations for different techniques and the neural network performing hybridization

CONCLUSION AND PERSPECTIVES

This work demonstrates that machine-learning-assisted hybrid metrology enables robust and physically consistent estimation of nanometric geometric parameters. By combining complementary techniques and training neural networks on physically representative simulated data, significant uncertainty reduction is achieved compared to conventional approaches. Future work will focus on extending this framework toward direct integration of raw measurement data—such as images and diffraction spectra—into neural networks. This evolution is expected to further enhance information extraction while maintaining metrological traceability, supporting next-generation dimensional control in advanced microelectronics manufacturing.

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KEYWORDS

Hybrid Metrology, Machine Learning, Nanometer-scale dimensional measurement, Data fusion, Measurement uncertainty reduction

A Compact X-ray Light Source for Characterization and Metrology

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INTRODUCTION

The continuous progress towards smaller and faster semiconductor devices demands innovations in prototyping and characterization tools, and there is urgent need to develop small-scale metrology platforms can be installed directly at the fab-scale production facilities for in-line diagnostics. We will discuss a Compact X-ray Light Source (CXLS) that we have recently commissioned at Arizona State University (ASU) CXFEL facility. This source is based on inverse Compton scattering and offers tunability and high flux which can open new approaches to x-ray characterization.

X-RAY SOURCE IMPLEMENTATION

We have developed a compact high-brilliance x-ray source optimized for small-angle scattering instrument intended to provide performance levels near those of CD-SAXS instruments at major synchrotron facilities but having a very modest cost and footprint. As the CXLS flux is 100x higher than a conventional x-ray lab source, it hopefully solves the key throughput limitation of CD-SAXS and enables compact in-line fab tools for non-destructive wafer probing, revealing key shape parameters at typical FinFET or GAA feature sizes.

Technical Approach and Footprint

The CXLS source is based on inverse Compton scattering (ICS), where photons from a high-power laser backscatter from a high brightness electron beam. The CXLS source is a product of several years of intensive research and development at ASU. The operational instrument in its current form as shown in the Figure 1 is installed in a vault of approximately 10m length, with parallel enclosures for the RF amplifiers and laser. The commercial version of such source can be made more compact than this prototype.

CXLS consist of an electron accelerator, high power ICS laser, and x-ray optics. The electron accelerator components consist of an RF gun to produce electrons, a short 1 m long standing wave linac, and magnets for beam transport. The gun and linac are innovative high-efficiency 9.3 GHz x-band devices that have been designed locally. The gun and linac are powered by a commercial 6 MW RF transmitter operating at up to 1 kHz. Electrons are produced at the flat copper cathode and accelerate to 3 MeV in the 3.5 cell RF gun. A solenoid focuses the electron beam into the linac which has an adjustable final energy depending on the desired x-ray energy. The x-ray energy scales rapidly as the square of the electron beam energy so that a wide range of tunability of x-ray energies is possible. Quadrupole magnets focus the electron beam to a approximately 3-micron spot at the interaction point where it collides with the ICS laser, after which it goes into the beam dump that is easily shielded for radiation protection.

The ICS laser is based on a commercial thin-disk Yb:YAG amplifier. The 200 mJ IR output pulse from the laser amplifier is transported to the interaction chamber where is collides with the electron beam at a small angle to

allow both the electron and x-ray beams to avoid the laser optics. The same laser oscillator that drives the ICS laser also seeds a separate laser amplifier for the UV photocathode drive laser to produce electron bunches.

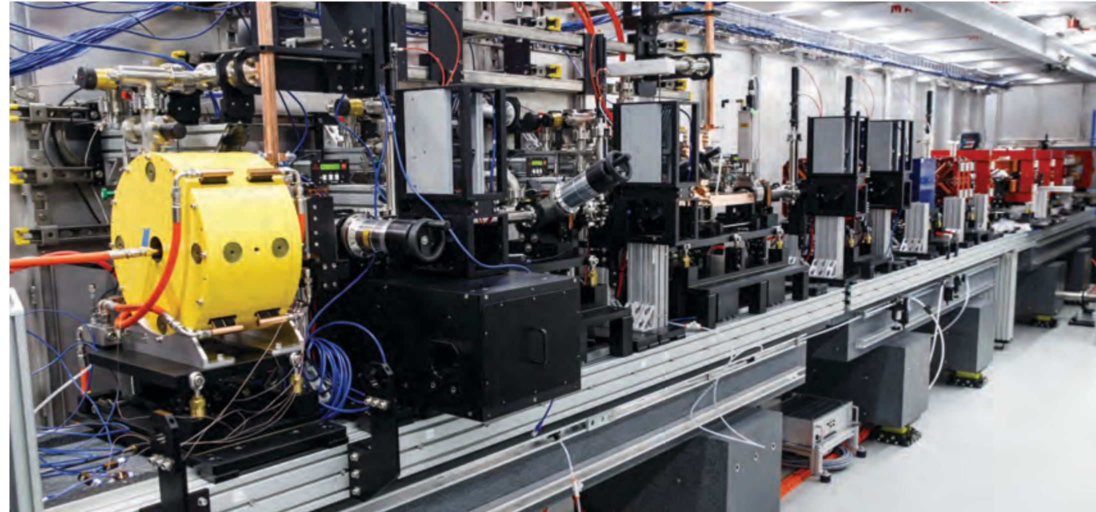

FIGURE 1. The image ASU CXLS device which is less than 10 meter in length. Compact linear accelerator (1.5m length) and electron transport are on the left. High power RF amplifiers and industrial quality Yb laser located behind the shield wall. The laser beam is transported through tubes to the interaction chamber on the right where it collides with electron bunch to produces x-rays. The x-ray optics are located inside the interaction chamber. CD-SAXS and other characterization methods can be implemented in the hutch past the right wall.

It is important to note that the central wavelength of this x-ray source is rapidly tunable between 6-20 keV by varying the electron energy. In the optimal configuration, the RMS source size is 2.5 microns with RMS divergence angle of 3 mrad. The average flux (before optics) is 3 X 10^{11} photons/sec at 17 keV in a 5% bandwidth. The optics can collect 80% of flux, and the surface reflectivity is 0.7, resulting in 40% throughput, or ~1 X 10^{11} photons/sec in a <100 µm diameter spot on the sample.

With some modification of the interaction geometry, the source can be operated in the soft-x-ray regime (0.3-2.5 keV). The upgrade of the accelerator can lead to harder x-rays >20 keV. The performance at 20-25 keV would have the same flux within a slightly smaller divergence angle due to the higher electron beam energy. We envision that this source opens new possibilities in transmission and reflection mode SAXS, as well as in fluorescence measurements and soft-x-ray resonant scattering. By virtue of its modest cost and footprint, along with its new technical capabilities, the CXLS source holds a lot of promise for in-line characterization.

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KEYWORDS

Compact x-ray source, Inverse Compton Scattering, CD-SAXS, metrology, characterization

Hybrid Metrology for Hot Spot Prediction in Post-Etch Patterning

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ABSTRACT

In semiconductor patterning processes, minimizing hot spots is essential, yet they are frequently undetected until pattern transfer or electrical characterization. In this work, we demonstrate how a low-cost hybrid metrology approach, in the form of an AI-augmented physics-informed etch model, can be trained with minimal metrology data to accurately predict etch performance and identify potential etch-induced hot spots across the wafer. The model is calibrated using tri-layer mask etch data from simple line/space structures. Once calibrated, the model simulates and predicts 3D post-etch profiles on a wide range of pattern layouts and geometries, highlighting areas that are susceptible to hot spot formation, such as tip-to-tip and tip-to-line patterns. Model predictions are experimentally validated against pre- and post-etch results on various pattern types. Overall, this hybrid metrology approach enables the early detection of problematic lithographic areas prior to wafer processing and could be used to establish patterning design rules that minimize etch-induced hot spots.

INTRODUCTION

Lithographic hot spots are regions in a chip layout that are prone to processing defects. These hot spots may occur due to factors such as stochastic lithographic variations or geometric effects in the feature layout[1]. A subset of these hot spots, such as pattern bridging or incomplete etch, arise during the pattern transfer process[1]. These etch-induced hot spots may occur for various reasons including random variations in feature spacing or pattern density effects that lead to microloading. The presence of hot spots ultimately leads to device failure and reduced yield, so early detection and correction is critical. Previously, we presented a synthetic demonstration of a low-cost hybrid metrology approach that predicts etch-induced hot spot formation prior to wafer processing[2]. We applied the calibrated hybrid metrology model to a complex tip-to-line pattern and simulated a dramatic drop in the tri-layer mask's etch rate when the post-lithographic spacing between the tip and the line falls below 18 nm, as shown in Figure 1. This abrupt reduction in the etched depth, characteristic of critical mask spacing/gap width, significantly increases the probability of incomplete etch hot spots during pattern transfer. The objective of this study is to experimentally validate the hybrid metrology model's post-etch hot spot predictions.

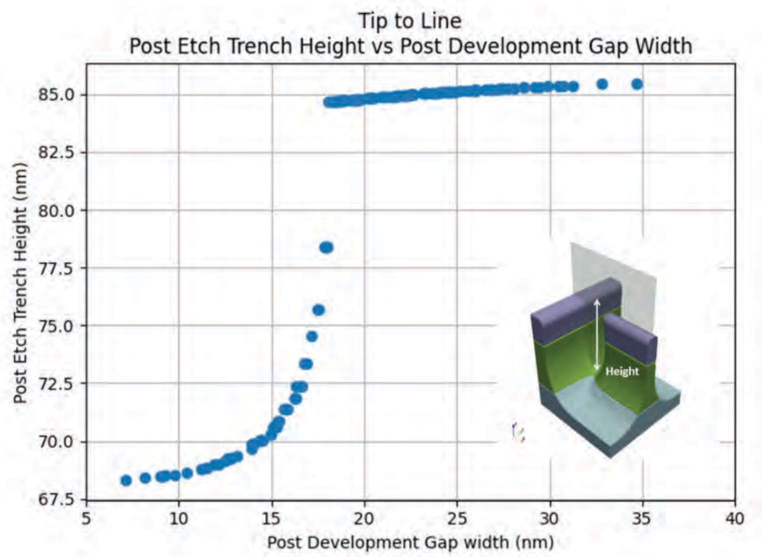

FIGURE 1. Trench height after amorphous carbon layer etch vs initial ADI gap width.

METHODOLOGY

To experimentally validate our hybrid metrology approach to predict and detect etch induced hot spots, 300 mm wafers were prepared with a tri-layer stack consisting of metal-oxide resist (22 nm)/spin on glass (10 nm)/amorphous carbon (35 nm). The mask layers were deposited on an oxide film (15 nm) that was deposited on a TiN film. The wafers underwent lithographic exposure, development, and plasma etching. CD-SEM images were taken on multiple pattern types after each fabrication step, specifically after development of the metal oxide resist and after etch of each individual layer through the oxide film. Additionally, cross-sectional SEM images were taken only on line/space patterns after each fabrication step. The SEM images of the line/space patterns were used to calibrate a physics-based etch model. Afterwards, the calibrated model predicted etch performance on more complex pattern layouts.

RESULTS AND CONCLUSIONS

Model simulations of etch-induced hot spots were validated against corresponding CD-SEM images. The hybrid metrology model simulates etch rate shifts and hence increased probability for etch-induced hot spots, in tip-to-tip and tip-to-line patterns. Experimentally, these defects were observed in those specific layouts. These results highlight the benefits of using an AI augmented, physics-enhanced hybrid metrology approach, including its non-destructive nature, speed, high resolution, and insight into the full 3D pattern geometry. Furthermore, there is potential for massive sampling and predicting defect behavior prior to wafer processing, saving valuable time and resources. Lastly, the calibrated hybrid metrology model can inform patterning design rules that minimize the formation of etch-induced hot spots, leading to less failures and higher yields.

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KEYWORDS

Hybrid Metrology, EUV, Lithography, hot spots, defectivity

Frontiers in Semiconductor Devices with 3D Integrations Opportunities for process and metrology

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INTRODUCTION

The semiconductor industry is on track to reach 1 trillion US dollars market size by 2030, to support the growing demands in artificial intelligence, mobile, personal computing, automotives, industrial, internet of things and robotics. This expansion is driven not only by capacity, but also by technology inflections into faster, denser and more efficient logic, DRAM and NAND devices, and new methodologies to package them together. Threedimensional (3D) inflection is one common theme across all device segments. NAND has already migrated to 3D NAND. FinFET logic transistors are migrating to gate-all-around (GAA). Very active development is in progress for 3D-DRAM. Such 3D migrations create unprecedented complexity for both process and metrology to deliver performance enhancements and yield improvements.

This talk will discuss existing and future challenges associated with semiconductor devices with 3D integrations, and the corresponding solutions required for both process and metrology. Notably, the challenges and needs are significantly different between the R&D phase and high-volume manufacturing phase, in terms of precision, throughput, in-situ versus exsitu, and to the broader scope of Equipment Intelligence® fusing on-tool and off-tool metrology data for productivity and yield enhancement. There are abundant opportunities for process and metrology engineering to collaborate and accelerate the 3D inflections needed for the semiconductor industry.

Addressing Metrology Challenges in Hybrid Bonding: An Overview of Tokyo Electron's X-ray Imaging Program Focused on Overlay and Defects

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INTRODUCTION

The hybrid bonding equipment market has been rapidly growing, driven by advancements in AI and the resulting demand for higher interconnect density. This increasing pressure on advanced packaging is accelerating the growth of 3D integrated packaging. According to a Yole Group research report, the global hybrid bonding equipment market is expected to expand from $152 million in 2025 to $397 million by 2030, at a compound annual growth rate (CAGR) of 21.1%, fueled by adoption in AI, chiplets, and high bandwidth memory (HBM) stacks [1]. The rapid evolution of semiconductor technology toward 3D integration—such as die-to-wafer (D2W) hybrid bonding and multi-die stacking in HBM—has introduced unprecedented metrology challenges.

An ideal overlay metrology strategy for 3D integration hybrid bonding would satisfy several critical criteria: (1) non-destructive measurements at both intermediate and full 16-die (and later 20-die) stacking levels; (2) elimination of the need for a metal-free zone; (3) fiducial dimensions no larger than 50×50 µm², eventually progressing to no fiducials required; (4) accuracy within ±50 nm; and (5) high throughput. Current infrared-based metrology tools and fiducials struggle to meet these requirements due to limited penetration depth and field of view, resulting in indirect, offset measurements with cumulative stack-up errors. These limitations hinder accurate alignment detection beneath dense metal interconnects and complex multilayer stacks.

Beyond overlay alignment, defect detection—particularly void characterization at bonding interfaces—constitutes a critical bottleneck for yield and reliability. Voids as small as 1 µm can degrade electrical continuity and mechanical robustness. However, traditional absorption-based X-ray inspection and other modalities lack sufficient sensitivity and resolution in metal- or dielectric-rich environments. Research has shown that the phase shift cross section per atom is more than three orders of magnitude higher than absorption for dielectric materials [2].

Addressing the challenges of non-destructive metrology through dense materials requires innovative approaches that combine high-resolution imaging with industrial throughput and no radiation damage to devices. In this paper, we discuss the key metrology challenges and the necessity for a deeply penetrating imaging system. We present our novel multi-modal X-ray imaging system coupled with a Moiré fiducial design. The multi-modal X-ray approach aims to reduce radiation-induced damage to devices, while the Moiré fiducials enhance overlay measurement sensitivity, enabling more precise and reliable inspections.

METHODOLOGY

Our approach innovatively combines multi-modal X-ray imaging based on Talbot-Lau grating interferometry principles with advanced Moiré fringe-based fiducials designed for 3D integration stacks [3, 4].

Multi-Modal X-ray Imaging

The Talbot-Lau system employs three precision gratings—source modulation, beam splitter, and analyzer—to simultaneously capture transmission (absorption), phase contrast (refraction), and dark-field full-field small-angle scatter (FI-SAXS) imaging modalities. Leveraging phase and scatter signals minimizes energy deposition in devices, significantly reducing the risk of radiation damage. As published earlier in [3], the X-ray source energy is optimized to minimize absorption while maximizing the sensitivity of other modalities.

Advanced Moiré Fiducials

Moiré-based fiducials amplify misalignments by a magnification factor of up to 100×, enabling detection of overlay errors well below ±50 nm despite the system's spatial resolution being on the micron scale. The dual-row differential pair configuration detects opposing fringe shifts, providing high sensitivity and linear measurement response. A proprietary library of fiducials, optimized in spatial and frequency domains, maximizes the signal-to-noise ratio (SNR), even when fiducials are buried beneath multiple Cu and dielectric layers, without requiring clear-out zones—a common design constraint in optical systems.

RESULTS AND DISCUSSIONS

Figure 1 provides an overview of the X-ray imaging metrology system designed for hybrid bonding inspection. Figure 1(a) shows the full system setup capable of non-destructive inspection through bonded interfaces, demonstrating the superior penetration capabilities of X-rays compared to other optical methods. Figure 1(b) presents a simplified schematic highlighting critical components such as the integrated EFEM with wafer and film frame loading ports, a high-power X-ray source, a sample stage with normal and oblique incidence, and a large field-of-view detector. The combined multi-modal images in Figure 1(c) illustrate how these imaging modes complement each other to enhance contrast and reveal detailed structural features beneath metal and dielectric layers that are challenging to detect with conventional methods. Experimental modulation transfer function (MTF) analyses show a spatial resolution of 2 μm with a field of view exceeding 1.7 mm².

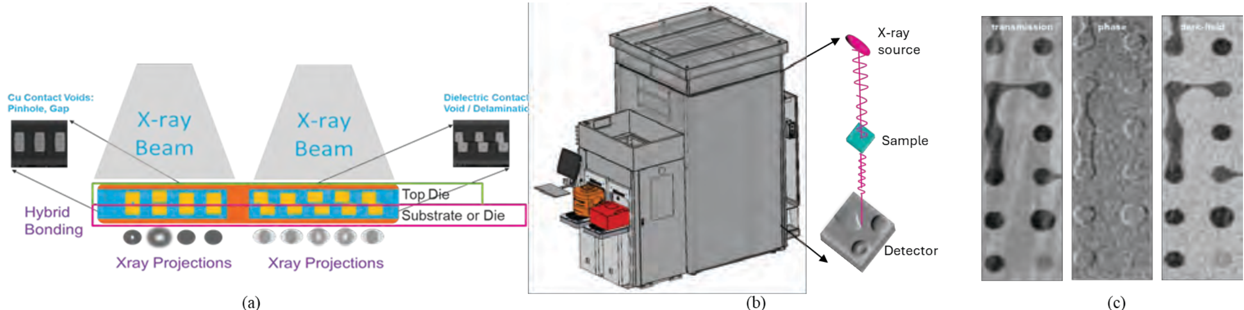

FIGURE 1. (a) X-ray imaging-based metrology system for hybrid bonding inspection. (b) Simplified schematic highlighting critical components of the X-ray imaging system. (c) Multi-modal images acquired by the system.

Figure 2 focuses on the Moiré fiducials integrated into the hybrid bonding layers for overlay metrology. Figure 2(a) shows the Moiré fiducials located on the same hybrid bonding layer, positioned on the left side of the bonding pads for illustration purposes. Figure 2(b) presents actual images of the Moiré fiducials, confirming their high contrast and visibility. Figure 2(c) presents measurement data demonstrating improved sensitivity and linearity, with overlay misalignments amplified by up to 20×.

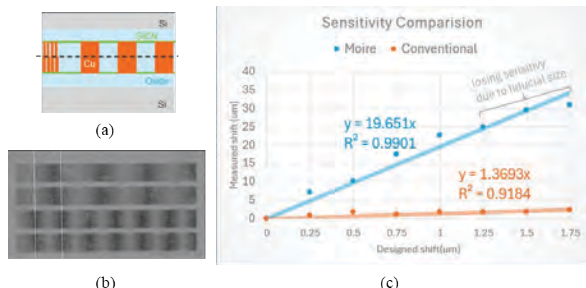

FIGURE 2. (a) Illustration of Moiré grating fiducials positioned on the hybrid bonding layer. (b) Actual images of Moiré fiducials demonstrating high contrast and visibility. (c) Measurement results showing improved sensitivity of Moiré fiducials.

These results confirm that combining multi-modal X-ray imaging with advanced Moiré fiducials is a promising approach to deliver accurate, high-throughput metrology for overlay and defect detection in challenging 3D hybrid bonding structures—addressing key needs in next-generation semiconductor packaging.

CONCLUSIONS

Advanced multi-modal X-ray imaging, combined with innovative Moiré fiducial designs, provides a transformative solution to the dual metrology challenges of alignment accuracy and defect detection in 3D hybrid bonding. This technique overcomes the penetration and field-of-view limitations of optical systems, enabling direct and non-destructive metrology with demonstrated improvements in overlay sensitivity and void inspection resolution. The low-dose phase-contrast approach ensures no X-ray induced device damage, which is critical for sensitive memory and logic devices, while projected throughput targets align with industrial requirements for high-volume manufacturing. Continued development and integration efforts promise practical deployment supporting next-generation heterogeneous integration technologies such as HBM stacking, CoWoS, and SoIC. This capability addresses the aggressive demands of leading semiconductor manufacturers striving to extend Moore's law via advanced packaging, positioning Tokyo Electron's X-ray imaging technology as a key enabler for future 3D integration fabrication and quality control.

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KEYWORDS

Hybrid bonding, X-ray imaging, metrology, overlay, defect, void, die-to-wafer, wafer-to-wafer

From Wafer to Package: High Performance X-Ray Sources Driving Semiconductor Progress

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INTRODUCTION

The continuous drive for higher performance, lower power consumption, smaller form factors, and reduced cost per function is accelerating the transition from traditional 2D scaling to advanced 3D integration across the semiconductor value chain. Consequently, system complexity increases, and early defect detection and yield management become increasingly critical. Simultaneously, the introduction of novel material systems further amplifies the challenges in metrology and inspection.

To address these challenges, a wide range of X-ray based methods, including analytical techniques such as spectroscopy, diffraction, and scattering, as well as 2D and 3D X-ray imaging, are being employed. However, as the requirements for throughput, resolution, and detection limits continue to intensify, there is a growing demand for improved X-ray tools suitable for off-line laboratory as well as at-line and in-line inspection environments.

One of the major bottlenecks in advancing X-ray based methods lies in the X-ray source itself. Achieving sufficiently small X-ray spots and beam sizes, high brightness and flux as well as optimized spectra for specific applications remains a key challenge in this field.

In this work, we discuss the fundamentals of X-ray generation and present recent advances in both solid- and liquid-target X-ray technologies. The benefits of these developments are illustrated through application examples, particularly in the field of advanced semiconductor packaging.

ADVANCING X-RAY SOURCE PERFORMANCE

Any X-ray application ultimately depends on the performance of its source, and because X-ray generation is an inherently inefficient process, the source typically represents the main limiting factor in the overall system performance. Most X-ray sources rely on electron-impact generation, where an accelerated electron beam strikes a solid target to produce X-rays. The achievable brightness is fundamentally limited by the power density that the target material can withstand before melting.

Excillum addresses this limitation through two innovative X-ray source technologies, as illustrated in Figure 1. First, the liquid MetalJet source technology replaces the traditional solid target with a continuously flowing liquid metal, eliminating the thermal limit associated with melting and thereby enabling significantly higher power densities and brightness. First introduced in 2009 and now in its third generation, the MetalJet technology offers unprecedented speed and performance in many different types of applications especially when combined with optics.

Second, Excillum's diamond transmission solid-target technology utilizes a thin target layer bonded to a diamond substrate. The exceptional thermal conductivity of diamond allows for efficient heat dissipation, enabling higher electron-beam power loading. Combined with a finely and precisely focused electron beam, this design produces an extremely small and bright X-ray spot, which is ideal for high-resolution imaging suitable for advanced metrology and inspection applications.

FIGURE 1. Illustration of MetalJet (left) and NanoTube (right) X-ray source technology.

X-RAY METROLOGY AND INSPECTION FROM LAB TO FAB

The higher complexity and greater need for inspection is true from off-site laboratory analysis such as failure analysis to at-line and in-line inspection in the fab environment. Traditional laboratory methods typically offer the highest levels of resolution and accuracy, as these techniques often allow for lower throughput and may tolerate some sample preparation. In contrast, metrology and inspection in a manufacturing setting must balance measurement precision with higher throughput requirements while maintaining non-destructive operation. Here, we illustrate the current state of the art with two advanced packaging examples. Details on the X-ray setups used can be found in [1] and [2].

Example 1: Nano-CT of Hybrid Bonding

Hybrid bonding is a technique for interconnecting vias without solder, in which small copper pillars are used to directly connect silicon dies. This approach is highly attractive from a cost perspective because it can reduce the number of processing steps. More importantly, it enables significantly higher via densities, making it a key technology for next-generation 3D integration. Although hybrid bonding has been commercially deployed, several challenges remain. Hence, there is a strong need for effective tools for failure analysis and process control to support the continued development and scaling of this technology.

As hybrid bonds and connected TSVs are typically very small, this poses a significant challenge for 3D X-ray measurements. Here, we performed a high-quality scan of an AMD Ryzen 7 5800X3D processor at a voxel size of 100 nm, as illustrated in Figure 2. The hybrid bonds imaged here have a diameter of 1.5 µm, are 15 µm long (including Cu pillars), and are arranged with a pitch of 9 µm.

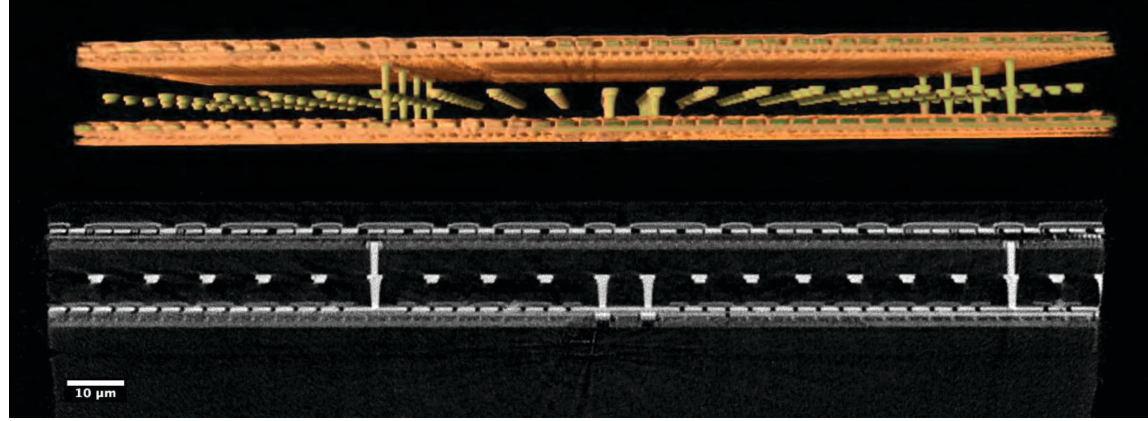

FIGURE 2. 3D render and virtual slice through hybrid bonds. (N.b. No AI/ML was used to obtain these images.)

Example 2: Non-destructive laminography of HBM microbumps

In this study, we measured a GPU sample containing a stack of eight HBM DRAM modules. These are interconnected using 5 µm TSVs and 20 µm microbumps. A 3D render is shown in Figure 3, which provides an overview of the inspected structures. In addition, virtual slices extracted from the reconstructed volume are illustrated in both the horizontal and vertical directions.

The horizontal slice, benefiting from a higher in-plane resolution, clearly revealed voids and other defects within the microbumps. The vertical slice, although affected by reconstruction artifacts associated with the missing cone of the laminography geometry, still provides valuable information on the TSV alignment and small defects in the microbumps.

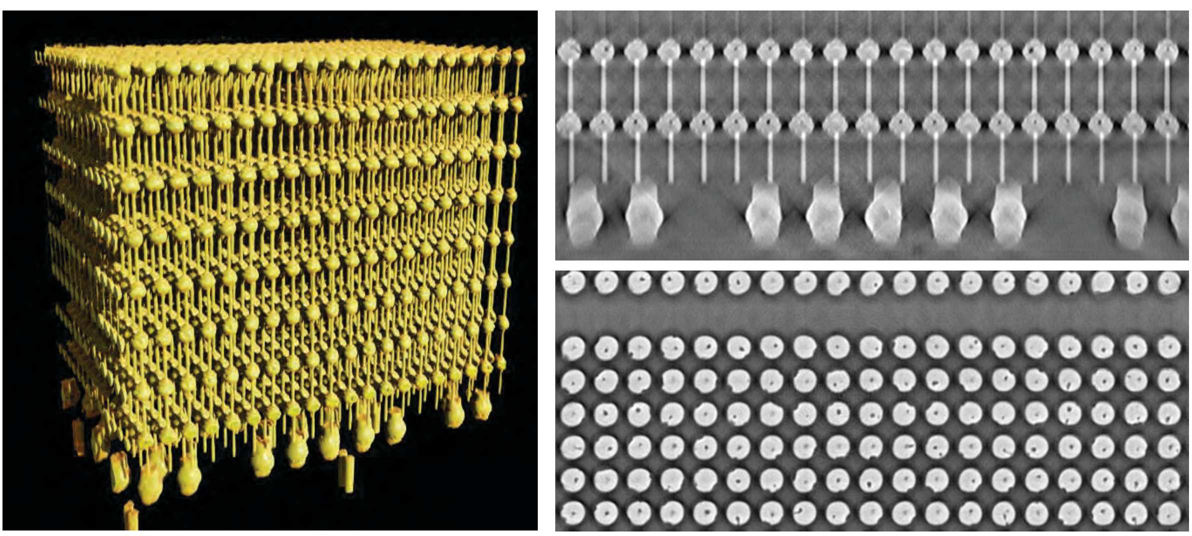

FIGURE 3. 3D render, vertical and horizontal virtual slices of the HBM stack illustrating TSVs and 20 µm microbumps. (N.b. No AI/ML was used to obtain these images.)

BEYOND GEOMETRIC MAGNIFICATION

The above examples illustrate how the resolution of features down to a few hundred nanometers is possible. However, breaking the 100 nm resolution limit is not easy using geometric magnification. Here, methods utilizing a bright and powerful source like a Gallium and Indium MetalJet coupled with optics (e.g., poly-capillary optics and Laue or zone plate lenses) is needed as described in [3-4]. In such setups resolutions down to sub 50 nm have been demonstrated for semiconductor samples [4].

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ACKNOWLEDGEMENTS

The author would like to thank Till Dreier and Daniel Nilsson for providing experimental data and invaluable support.

KEYWORDS

X-ray source, MetalJet, Inspection, Metrology, Nano CT, Laminography, Advanced packaging

TBD

Aviram Tam

Applied Materials

Metrology for EUV Lithography at NewSUBARU Synchrotron Light Facility

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EUV lithography was started to use in the high-volume manufacturing from the 7 nm+ logic node since 2019. However, three main technical issues are still remained. The first priority of the technical issue is to realize resists which can satisfy the specification of resolution < 10 nm, line width roughness < CD of 10%, sensitivity < 30 mJ/cm^2, and low defectivity. And the second priority is to realize the EUV mask to satisfy the low defect density, defect inspection through the pellicle, and handling without defect. The third priority is to realize the EUV light source which has light power > 1 kW with long lifetime and stability. Especially to solve the technical issues on resist and mask, the metrology technics are very significant to use synchrotron radiation. From this viewpoint we will introduce the metrology using synchrotron radiation for EUV lithography at NewSUBARU synchrotron radiation facility. Figure 1 shows the NewSUBARU synchrotron light facility. Since 2021 NewSUBARU has been operated using new linear accelerator as an injector of NewSUBARU. which is based on the c-band technology supported by the accelerator group of the SPring-8 RIKEN. NewSUBARU is operated at the electron beam current of 350 mA in Top-up mode (continuous injection mode to keep the beam current with high stability). Now we have four beam lines for the research of EUV lithography.

Fig. 1 Photograph of NewSUBARU synchrotron light facility.

The metrology for EUV lithography is very significant for the research of EUV resist and mask. In this presentation, the usage metrology methods of synchrotron are introduced. The main phenomena of photon interactions between materials are reflection including scattering, transmission and absorption, and diffraction. Using those phenomena, various kinds on metrology methods can be constructed. As the metal pitch is coming smaller and smaller to control in the size order of picometer, the metrology in the dimension size of picometer is required necessariliy. Thus, the light wavelength should be shortening to the soft x-ray region is required for the light source of the metrology for EUV lithography. The instruments for the EUV lithography which are listed below are the instrumentations of the NewSUBARU beamline. As shown in Table 1, there are six type instruments for the resist

research and seven type instruments of the research of mask, pellicles, and optics, mainly. In the presentation the key points of the metrology will be discussed.

Table 1. The list of the instruments for EUV lithography at constructed at the EUVL NewSUBARU beamlines.

Resist	➢ Sensitivity and outgassing[1)] measurement ➢ Total Electron Yield (TEY) [2)] for the chemical reaction analysis for EUV and BEUV resists ➢ Transmission[3)] and absorption measurement of various materials for the lithography ➢ Patterning by the interference lithography[4)] ➢ Chemical homogeneity evaluation[5)] by RSoXS, and PEEM ➢ 2ndry electron (Photoelectron energy) distribution analysis and low 2ndry electron chemical behavior analysis[6)]
Mask, pellicle, and Optics	➢ Measurement of reflectance[7),] transmission, scattering, and optical index measurement ➢ Reflectance of large optics (< ϕ800 mm) for the collector mirror of EUV LPP light source[8)] ➢ Mask defect inspection by EUV microscope[9)] ➢ Coherent scattrometry microscope (EUV-CSM) for the mask defect inspection in 3D[10)] ➢ High harmonic gas laser adapted on EUV CSM[11)] ➢ Out-of-band (OoB reflectometer)[12)] ➢ EUV durability in H_2 / H_2O[13)]

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KEYWORDS

EUV Lithography, short wavelength, soft X-ray, synchrotron radiation, metrology, EUV resist, EUV mask, EUV pellicle

Metrology Requirements for Nanoimprint Lithography

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INTRODUCTION

Imprint lithography is an effective and well-known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of advanced semiconductor device levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

To establish a new lithographic production solution requires the support of an ecosystem in order to enable seamless insertion of the technology. Examples include the fabrication and qualification of a 1x imprint mask. In this paper, we review the advanced semiconductor device metrology requirements for the supporting infrastructure, the NIL process itself simulation and touch on metrology needs for other applications suitable for NIL.

NIL Infrastructure and Mask Metrology

The NIL infrastructure[1], as shown below in Figure 1 starts with the design and fabrication of an imprint mask.

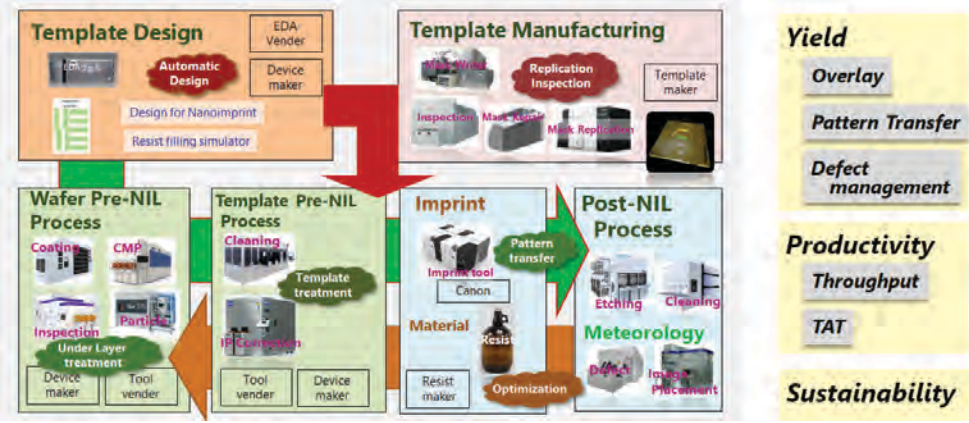


FIGURE 1. Schematic illustration of the NIL ecosystem

As opposed to optical lithography, where mask features are written four times larger than what is printed on a wafer, the NIL mask patterns must be the same size as what is printed on the wafer. This creates challenges for the writing, inspection and repair of the mask. The most advanced mask writers can resolve 14nm lines, but future device nodes will require resolution better than 10nm. Optical inspection methods can "see" breaks in 14nm lines, but the requirements are more aligned with sub-5nm resolution. Repair techniques are largely untested at dimensions below 14nm.

Similar challenges exist for the placement of features on the mask. A good starting point is 1nm, 3σ. Mask image placement (IP) is critical for NIL, since any errors become part of the NIL overlay error budget. DNP has written different mask types using IMS Nanofabrication multibeam mask writers. The result for both critical dimension uniformity (CDU) and IP are shown below in Figure 2. For the pillar type mask, image placement was ~1nm.

2x nm line/space

		Master
Defects	pcs/cm^2	-
CDU (3σ)	nm	0.44
IP (3σ)	nm	1.52/0.91

2x nm pillar

		Master
Defects	pcs/cm^2	-
CDU (3σ)	nm	0.65
IP (3σ)	nm	0.97/1.02

FIGURE 2. Critical dimension uniformity (CDU) and image placement (IP) for two mask types.

NIL Metrology

Advanced device fabrication requires layer to layer overlay of better than 2nm in many cases. The NIL approach for overlay is quite different that optical lithography which manipulates both the lens and stage during the exposure process. A different approach is required for nanoimprint. High Order Distortion Correction (HODC) for NIL can be enabled by combining two techniques.

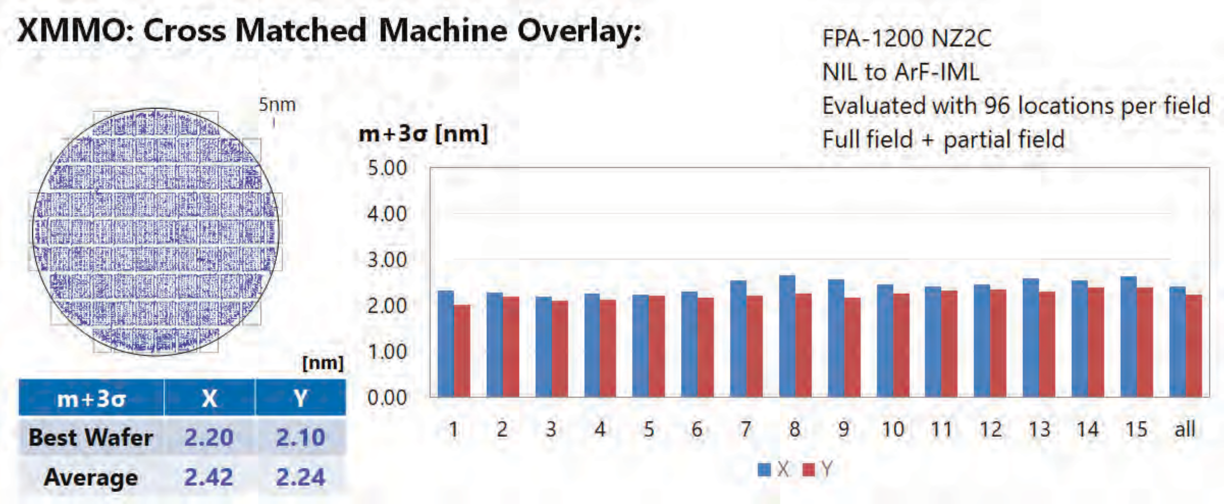
- One is using Magnification actuators, which apply force using an array of piezo actuators.
- And second is Heat input, which is supplied by a DMD to correct distortion on a field-by-field basis.

The HODC method has been presented in the past, and recently additional corrections methods have been applied in order to drive cross matched machine overlay (XMMO) to an ArF immersion scanner down to 2nm. Additional terms include:

- drop pattern compensation
- imprint force
- imprint tip/tilt control
- pattern placement
- compensated masks
- and wafer zone chuck pneumatics.

Details on these correction methods can be found in references 2-3.

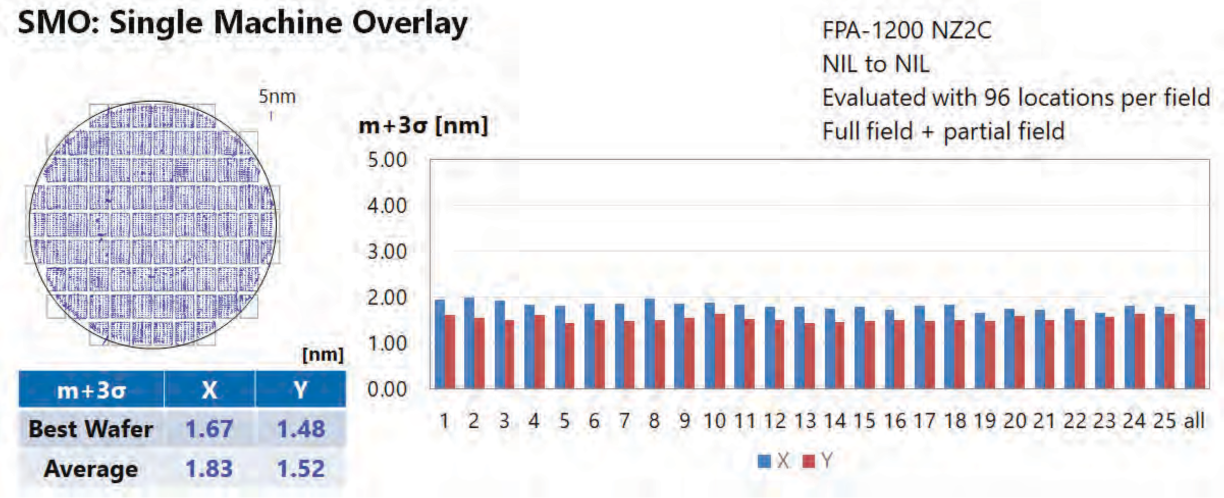
In Figure 2, we present the most recent cross matched machine overlay (XMMO) results from 2022. For this work, NIL was matched to an ArF immersion scanner, and the reported results show the measurements for all fields, 96 locations per field. Full field XMMO was on the order of the 2nm mean plus three sigma. Full field and partial fields results were slightly higher. Overall, the average mean plus 3 sigma variations was 2.4nm and 2.2nm in x and y, respectively. Best results were on the order of 2.2nm and 2.1nm.



m+3σ	X	Y
Best Wafer	2.20	2.10
Average	2.42	2.24

FIGURE 2. NIL to ArF immersion cross matched machine overlay.

In Figure 4, we present the most recent single machine overlay (SMO) results. The NIL NZ2C tool was matched to itself, and the reported results show the measurements for all fields, 96 locations per field. The best results achieved were on the order of 1.6nm, mean plus 3 sigma. On average across a full lot of twenty-five wafers, the SMO was 1.83nm and 1.52nm in x and y, respectively.



m+3σ	X	Y
Best Wafer	1.67	1.48
Average	1.83	1.52

Figure 4. Full field and partial field single machine overlay on an NZ2C imprint platform.

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KEYWORDS

Nanoimprint lithography, NIL, overlay, image placement, inspection, repair

Cross-Validated Anisotropic Thermal Conductivity Metrology of AlN Films

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INTRODUCTION

Backside power delivery networks (BSPD) and heterogeneous integration are shifting both electrical and thermal paths in advanced logic. High thermal conductivity dielectric and passivation films, including aluminum nitride (AlN), are being evaluated to reduce local temperature rise while maintaining electrical isolation. For BSPD process development and production control, thermal conductivity must be quantified in both the cross-plane ($k_\perp$) and in-plane ($k_\parallel$) directions at film thicknesses relevant to integration, and with sufficient throughput to support wafer-scale decision making.

MEASUREMENT CHALLENGES AND STACK DESIGNS FOR HIGH-K FILMS

Thermoreflectance techniques provide non-contact access to thermal transport in thin films, but high thermal conductivity films can be difficult to measure because the extracted conductivity can be coupled to interface resistances, metal transducer properties, and the thermal length scales set by spot size and modulation frequency. Here we use stack design as a metrology variable. A high-k film on silicon primarily drives heat into the substrate, increasing sensitivity to $k_\perp$, while inserting a low thermal conductivity oxide underlayer (SiO_2/Si) promotes lateral spreading within the film, increasing sensitivity to $k_\parallel$ (Figure 1).

Cross-Validation Across SSTR, TDTR, and FDTR

We present a comparative study of AlN films using three thermoreflectance modalities (steady-state, time-domain, and frequency-domain). Across the three measurements, we quantify $k_\perp$ and $k_\parallel$, evaluate parameter sensitivities, and consolidate best practices for high thermal conductivity films intended for BSPD modules. The workflow emphasizes (i) selecting a stack that maximizes sensitivity to the targeted conductivity component, (ii) separating film conductivity from boundary resistances, and (iii) reporting uncertainty based on sensitivity-informed error propagation rather than fit residuals alone.

Case for In-Line and 300 mm Thermal Metrology

To translate these best practices into manufacturing-relevant metrology, the same measurement physics can be deployed in an automated, fiber-based platform with recipe-driven operation and statistically grounded sampling plans across wafers. In-line or near-line deployment on 300 mm enables rapid screening of BSPD dielectric stacks, monitoring wafer-to-wafer drift in $k_\perp$ and $k_\parallel$, and faster down-selection of deposition conditions that preserve high thermal conductivity under thermal budget constraints.

For high thermal conductivity films, wafer-scale implementation is especially impactful because spatial non-uniformity in thermal conductivity often correlates with microstructure and defect density, which also influence electrical leakage and reliability. By measuring thermal properties at multiple sites per wafer, the metrology can serve as an early indicator of process excursions before electrical test structures are fully available.

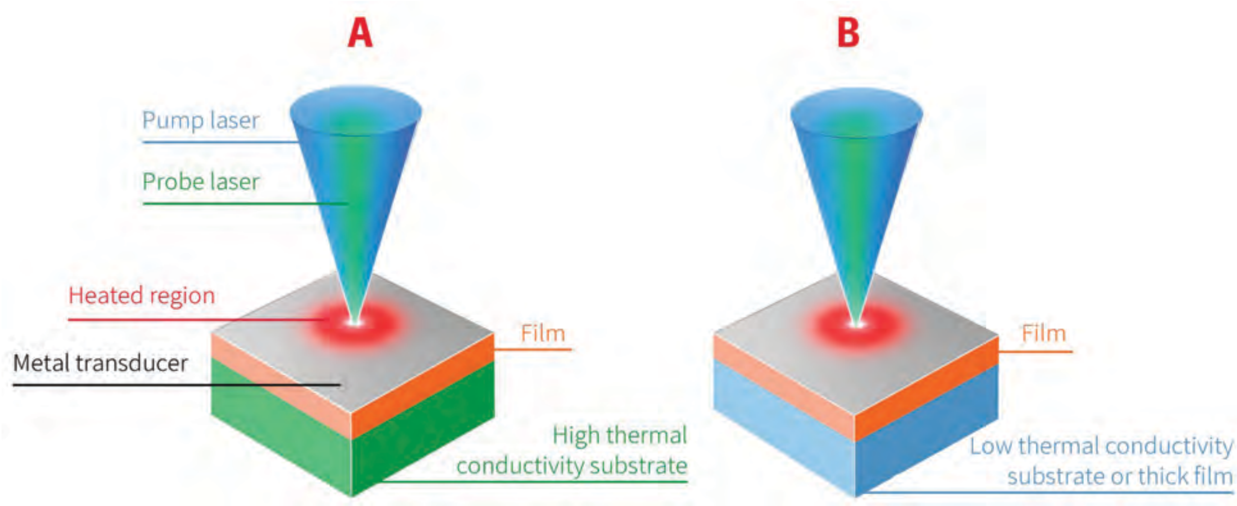

Figure 1. Stack-engineered sensitivity for high thermal conductivity films. (a) High-k film on Si increases sensitivity to cross-plane conductivity (k⊥). (b) High-k film on SiO_2/Si increases sensitivity to in-plane conductivity (k∥) through enhanced lateral heat spreading.

RESULTS AND DISCUSSION

Thermal conductivity measurements under two generic process conditions show that the high temperature condition yields higher thermal conductivities than the low temperature condition in both the cross-plane and in-plane directions. Rather than emphasizing specific numeric values in this extended abstract, we summarize the complementary roles of the three thermoreflectance modalities used for cross-validation and best-practice development (Table 1).

Sensitivity analysis across the three thermoreflectance modalities shows that the substrate stack strongly determines the identifiability of k⊥ versus k∥. For AlN on Si, the measurement response is dominated by through-thickness heat flow, enabling robust extraction of k⊥ with reduced correlation to k∥. For AlN on SiO_2/Si, the added thermal resistance beneath the film promotes lateral gradients, improving k∥ sensitivity and enabling anisotropy validation within a single material system. We discuss practical best practices for high thermal conductivity films, including selecting transducer thickness and modulation conditions to avoid over-weighting interface resistance and to maintain high signal-to-noise across wafers.

Table 1. Relative strengths and weaknesses of the thermoreflectance modalities used for cross-validation and best-practice development.

Method	Relative strengths	Relative weaknesses
SSTR	Direct access to total thermal resistance; useful constraint when interfaces dominate; pairs well with other methods; sample geometry can be used to extract multiple parameters	Lower leverage for separating multiple unknowns without complementary data; steady-state time constants can limit throughput depending on implementation
FDTR	Frequency sweep separates sensitivities across length scales; strong for multi-parameter fitting when	Requires good priors (thickness, substrate, transducer); multiple solutions can exist for ultra-

	regimes provide distinct leverage; automation-friendly	high-k, ultra-low-TBR stacks
TDTR	Mature, high-SNR transient response; strong for cross-plane extraction with appropriate thermal penetration depth; flexible spot size and delay-time shaping	Thin, high-k films can be underconstrained; interface resistances can mask film k without careful experiment design

CONCLUSIONS AND OUTLOOK

Cross-validated thermoreflectance metrology on stack-engineered test structures provides a practical path to confident k⊥ and k∥ values for AlN films intended for BSPD integration. Extending these workflows to automated 300 mm sampling unlocks process monitoring and statistical process control for thermal performance of backside dielectric stacks, accelerating material insertion while reducing risk to yield and reliability.

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KEYWORDS

backside power delivery, anisotropic thermal conductivity, thermoreflectance, in-line metrology, thermal boundary resistance, advanced packaging

Failure Analysis in the AI Era: Ensuring Reliability at Scale

Dr. James Chambers

Vice President of Silicon Engineering and Sourcing, NVIDIA

The semiconductor industry has entered a new era, driven by generative AI and large language models. AI models have scaled from millions to trillions of parameters, with datacenters hosting hundreds of thousands of GPUs and quadrillions of transistors. This complexity demands unprecedented silicon quality, reliability, and advanced failure analysis (FA). Modern AI factories are massive GPU networks that require near-zero latent

defects across silicon and system components. Compute-intensive workloads push the limits of process technology, integration, and packaging, exposing the subtlest of defects. Recent innovations such as 2.5D/3D integration, backside power delivery, and co-packaged optics introduce new defect mechanisms requiring even more advanced fault isolation and root cause determination methodologies. This talk explores how Failure Analysis (FA) is evolving to meet these challenges. We will discuss advanced probing, non-destructive techniques, and AI/ML-driven

automation to accelerate defect detection and diagnosis. Success depends on deep collaboration across fabs, design, product, and system teams to achieve stringent reliability targets. Finally, we will examine how accelerated computing and semiconductor innovation create a powerful feedback loop driving industry progress.

Nano-Optical Imaging And Spectroscopy Of Semicon Materials – An S-SNOM And AFM-IR Overview

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INTRODUCTION

nano-IR is a set of scanning probe techniques based on atomic force microscopy (AFM) in combination with a focused infrared (IR) laser beam. nano-IR enables IR imaging & spectroscopy with ca. 10 nm spatial resolution determined by the AFM tip radius. Here, we first differentiate and classify the existing nano-IR techniques (particularly the variants of AFM-IR and nano-FTIR / s-SNOM). Secondly, we recap the near-field probing mechanism and how this provides access to molecular absorption, crystal lattice vibrations and optical conductivity in a non-destructive, contact-free and nanoscale-resolved way for almost any AFM-scannable material [1]. Lastly, we will look at quantitative examples of nano-IR applied to semiconductor materials such as chemical identification of nanoscale contaminants, latent imaging of photoresists, and profiling of dopant density and charge carrier mobility as illustrated in Fig. 1.

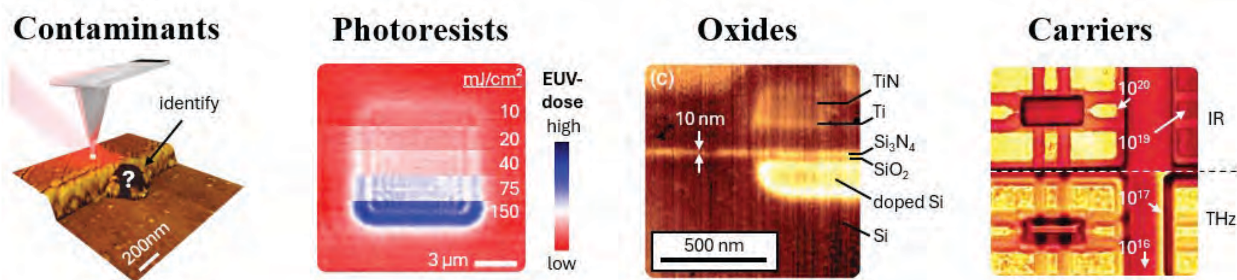

FIGURE 1. Semicon applications using nano-IR. (a) Chemical identification of a nanoscale contaminant, here PDMS [2]. (b) Chemical mapping of EUV-exposed but not-developed photoresist (latent image) [3]. (c) Analysis of oxide and nitride thin films in a cross-sectioned transistor device. [4] (d) Optical conductivity mapping of SRAM sample in the IR & THz spectral range [5]. Further use-cases not illustrated: III-V semiconductors, nanowires, topological insulators, metamaterials, 2D materials & more.

Molecular Absorption - Latent Infrared Nano-Imaging Of Photoresists

In nano-IR, the sample's local IR response is detected either via photothermal expansion forces (AFM-IR) or light scattering (nano-FTIR / s-SNOM), depending on the measurement goals. Notably, the nano-FTIR phase and AFM-IR amplitude both closely resemble IR spectra known from FTIR absorption spectroscopy – greatly simplifying the data interpretation. A conceptually simple use-case is the chemical identification of nanoscale contaminants, where obtaining the material type (e.g. via comparison with FTIR libraries) is sufficient – as demonstrated already in the earliest nano-FTIR publications [2]. Going further, Kim et al. used nano-IR to visualize latent patterns in photoresists, by essentially mapping the cross-linking density (red areas in Fig. 2a correspond to un-exposed "cage-like" resist). Interestingly, the nano-IR absorption signal scales linearly with the EUV dose,

enabling the quantification of exposure dose before any chemical development [3]. In a follow-up work, the authors provide visual evidence that chemical noise (inter-mixing of different molecular chains) in a PS-PMMA copolymer is effectively reduced via additional thermal treatment of the photoresist (Fig. 2b) [6].

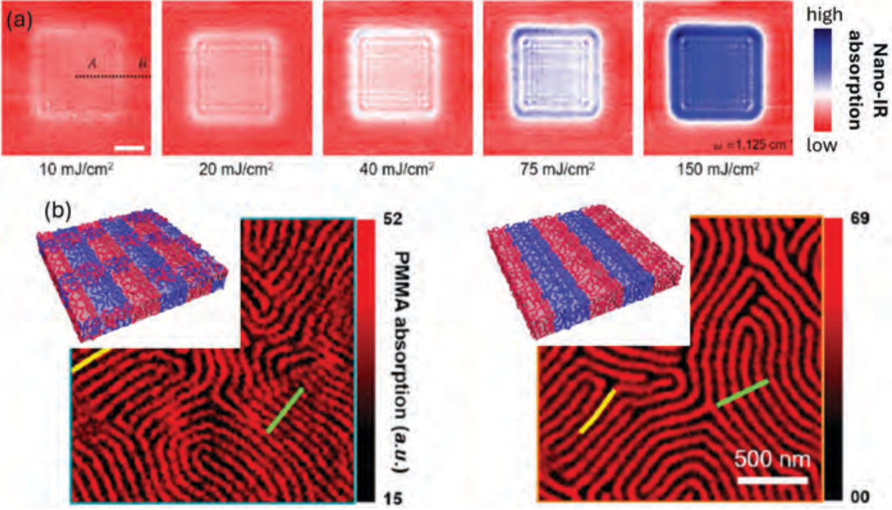

FIGURE 2. Nano-IR mapping of molecular vibrations in photoresists. (a) Chemical maps as a function of EUV-exposure dose, taken before chemical development of the resist. (b) Chemical noise in a PS-PMMA copolymer (left) is reduced via thermal annealing (right). [3, 6]

Crystal Lattice Vibrations - Mapping Of Strain And Stoichiometry

Crystal lattice vibrations (phonons) provide insights into defects, ion implant damage, crystal polytypes, lattice strain, and more. This class of materials was frequently studied in the early nano-FTIR years (due to signal levels being resonantly enhanced when sample permittivity $\varepsilon \approx -1$, as is often the case for lattice vibrations), and is slowly gaining interest also among AFM-IR users (despite the typically low thermal expansion coefficients of these materials). The recent introduction of widely tuneable OPO laser sources (570-7100 cm^{-1}) enables access to phonons of more materials such as SiC (~785 cm^{-1}), GaN (~725 cm^{-1}) and AlN (~610 cm^{-1}) that have not been accessible by QCL-based systems (800-1800 cm^{-1}). Overall, there is much untapped potential in using nano-IR for studying phonons. Fig. 3a illustrates strain-mapping which is enabled by probing small shifts of the phonon frequency [7]. Nano-IR probing of phonon vibrations may also provide a non-destructive way of quantifying the stoichiometry as shown in Fig. 3b at the example of $Ga_{1-x}Al_xN$ samples of varying material composition.

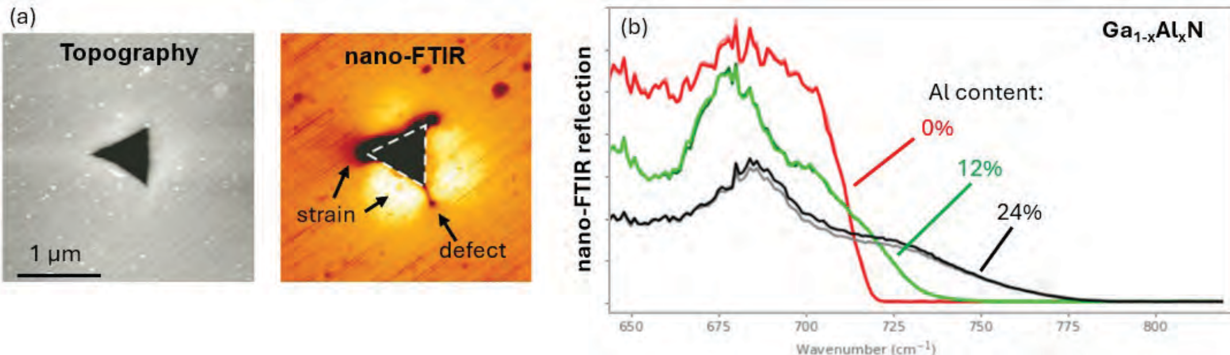

FIGURE 3. nano-IR probing of crystal lattice vibrations. (a) nano-IR map revealing strain and defects in SiC [7]. (b) nano-IR spectra of $Ga_{1-x}Al_xN$ samples with varying Al content.

Charge Carriers and Mobility – Non-destructive and contact-free quantification

Free charge carriers give rise to a plasma frequency, below which the reflectivity quickly increases (Fig. 4a) – this is called the plasma edge, from which the carrier concentration, carrier mobility and conductivity can be obtained. Nano-FTIR provides reflection and absorption in the IR and THz spectral range, which can be used to quantify both charge carrier concentration and mobility. Potential advantages of nano-FTIR over other techniques such as SSRM are that nano-FTIR needs no electrical contacts, is non-destructive, is not limited to Silicon-based materials, works on isolated nanoscale objects (such as single nanowires [8] or individual flakes of 2D materials [9]), and can provide subsurface information. To access a large range of doping concentrations (Fig. 4b), a large spectral coverage of light source must be employed, such as high-power THz-TDS emitters (0.1-5 THz), widely tunable OPO laser (625-7100 cm^{-1}), or synchrotron radiation using broadband nano-FTIR.

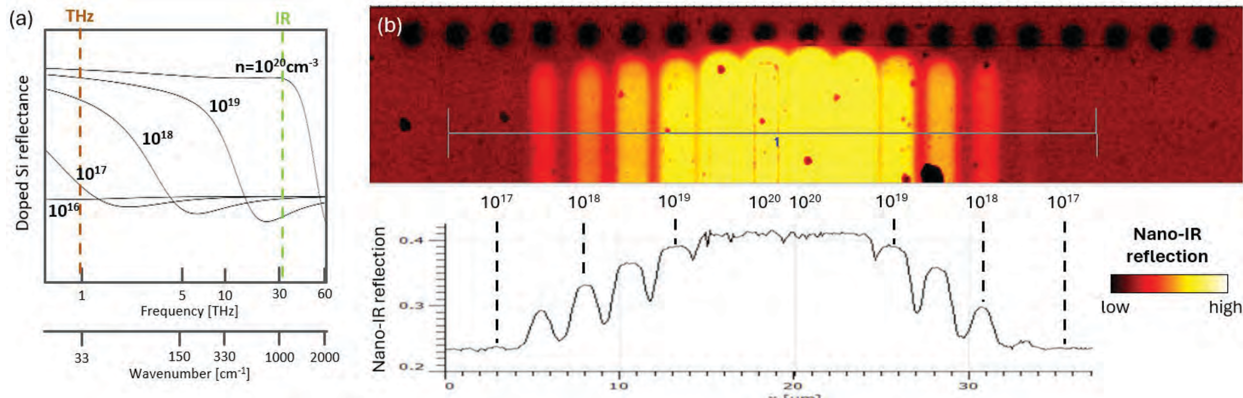

FIGURE 4. nano-IR for quantification of carrier concentration and mobility. (a) Calculated reflection of doped silicon. (b) nanoTHz-TDS reflection map and line profile of the IMEC doping calibration sample.

In this presentation we provide an overview of the possibilities and underlying probing mechanism in nano-IR. Please don't hesitate to contact the author for a more detailed discussion on specific applications.

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KEYWORDS

Nano-IR, Contamination, Defects, Photoresist, Lattice vibrations, Doping concentration and mobility

NANOSCALE QUANTUM SENSING FOR SPINTRONICS AND ELECTRONICS

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INTRODUCTION

Scanning NV Microscopy (SNVM) uses the highly sensitive properties of a single atomic defect in diamond to detect very weak electromagnetic signals and image magnetic materials and electronics with nanoscale precision. Over the past years, SNVM was successfully used to surface new data across various domains such as materials science, semiconductors, battery research and biology [1]. In this presentation we review the latest advances in SNVM applied to spintronics and electronics, including the testing of magnetic random access memory [2], the study of antiferromagnetic bits [3], probabilistic bits and piezo-electric domain walls [4].

SCANNING NV MICROSCOPY

Scanning NV (nitrogen-vacancy) Microscopy is a high-resolution quantum sensing technique that combines Atomic Force Microscopy with the magnetic sensitivity of a single point defect in diamond. A diamond probe containing a single NV center —an "artificial atom" composed of a nitrogen atom and a nearby vacancy—is scanned just nanometers above a sample surface. The process works through a method called Optically Detected Magnetic Resonance (ODMR). A green laser initializes the NV center's spin and triggers red fluorescence. By applying microwave radiation and monitoring changes in the fluorescence brightness, the system precisely measures the magnetic field. As the probe scans the sample, it simultaneously captures the sample's topography and a quantitative, nanoscale map of its magnetic stray fields, all while operating under ambient conditions.

MAGNETIC TESTING OF SPINTRONIC DEVICES

We first present results obtained on STT-MRAM. We show that SNVM can be used to map the magnetic textures of individual STT-MRAM bits (Figure 1). We analyze bit-to-bit variation and switching distributions over two different samples and compare our data with electrical measurements. Our results demonstrate the capability of SNVM to measure key parameters of MRAM devices early in the manufacturing process, positioning the technique as an interesting metrology solution for rapid testing of new processes and memory architecture. We further introduce results obtained on granular 100-nm-thick magneto-electric Cr_2O_3 films patterned in circular bits with diameters ranging from 500 down to 100 nm and ultra-scaled nanowires. We discuss what makes SNVM approach unique for surfacing such data, including in particular a reproducible spatial resolution in the 10nm range and magnetic fields sensitivities in the uT/sqrtHz range.

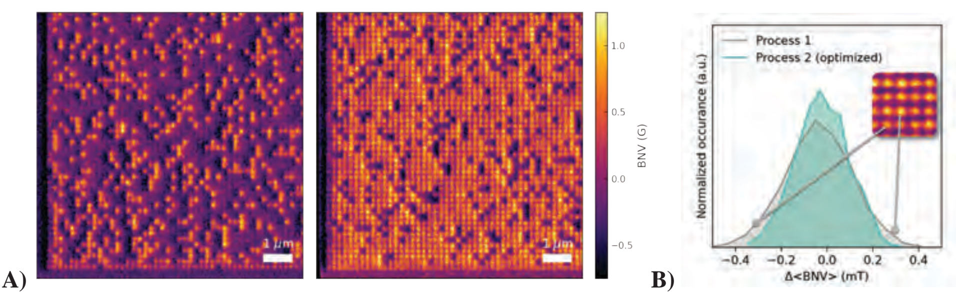

FIGURE 1. A) Magnetic bits in an MRAM array B) Magnetic Roughness and bit distribution

CURRENT IMAGING IN FERROELECTRIC MEMRISTORS

Domain walls in piezo-electric materials are used to build memristive devices, which can store and process information by switching and maintaining resistance states. Such devices are key candidates for future neuromorphic computing and low-power memory applications. SNVM is used to directly image the distribution of current flow by measuring the nanoscale magnetic fields generated by electrical currents in the device. The results reveal that, contrary to common assumptions, only a limited number of domain walls actually carry significant current. The current pathways are sparse and spatially localized, leading to a major reassessment of charge carrier density estimates in these systems—by as much as two orders of magnitude in some cases. We show how the combination of SNVM with other standard AFM techniques allowed to gain new insights into these materials.

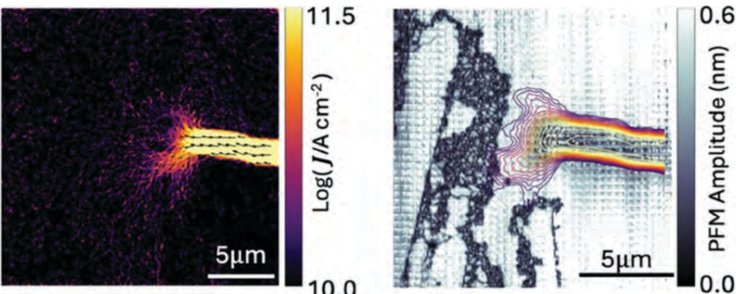

FIGURE 2. A) Current density map at the around the internconnect B) overlay of the local ferroelectric domain structure (PFM amplitude) with the current density contour map.

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KEYWORDS

NV Center, Quantum Sensing, MRAM, Magnetic Sensors, Spintronics, Nanoscale Electronics, Piezo-electric materials

TBD

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PTB

Moore's Law is dead. Long live Moore's Law

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ABSTRACT

Moore's Law is about far more than simple scaling. Gordon saw it as future driver using the law of supply and demand, where lower prices would create new demand. Moore's Law is dead because the areal cost of a wafer is now rising faster than the rate of density increase from scaling due to increasing process complexity. Essentially, the part of Moore's Law that's dead is using scaling to drive cost down.

Long live Moore's Law… There is always a prince in waiting to take the place of the dead king. The new Moore's Law is about using scaling and material systems engineering to drive up value in terms of computational power. This paper examines the factors driving up cost, looks at what has happened to other industries when costs stopped falling and started rising, and examines how organizations are adapting to the shift.

Metrology and Inspection for Advanced DRAM Production Using Second-Harmonic Generation

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[1]*CTO, Femtometrix. and* [2]*Team Lead, DRAM Metrology, SK Hynix*

INTRODUCTION

The field of optical metrology has mined the electromagnetic spectrum from mid-IR to x-rays looking for better ways to measure semiconductor parameters during the manufacturing process. In this paper, we present a new direction for metrology using non-linear optics. Second-harmonic generation (SHG), a non-linear optical effect, can be used to directly measure internal electrical properties of semiconductor devices during wafer processing. In this presentation, we provide the first results of SHG being used to monitor semiconductor electrical properties in high-volume production of advanced DRAM devices.

HOW SHG WORKS

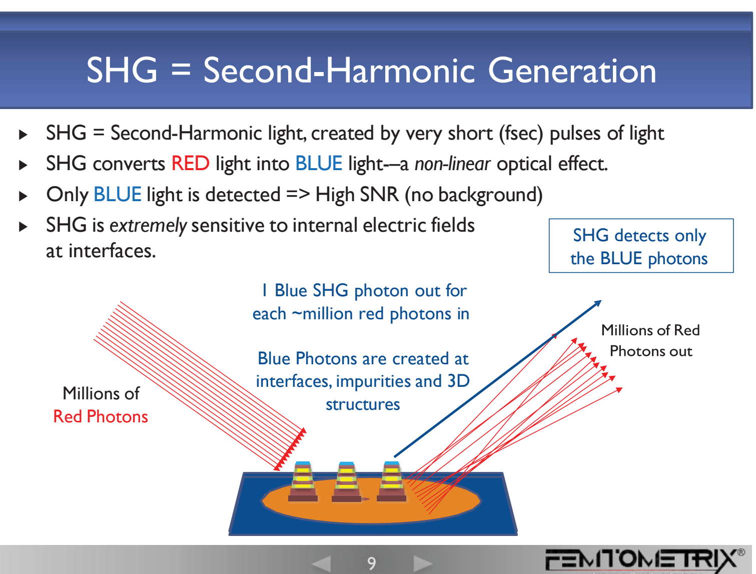

FIGURE 1. A Second-Harmonic Generation signal (SHG) is created by directing a femtosecond red (800nm) pulsed laser at the device under test. Blue light (400 nm) is generated inside the device at the material interfaces, which is detected after filtering out the red light.

Second harmonic light is generated by the sample when femtosecond pulses of red light (800 nm) are directed at a semiconductor wafer. The wafer can be patterned or non-patterned. Inside the wafer, the light excites electrons with strong electric fields. In specific locations, two red photons will combine to produce one blue photon at twice the frequency and half the wavelength (400 nm) of the incident light. It takes between 1 to 100 million red photons to

produce one blue photon. Moreover, the blue photons are generated only at surfaces, interfaces, small 3D features, as well as, in other places where the bulk symmetry of the crystal is broken.

SHG MEASURES INTERNAL ELECTRIC FIELDS

A strong internal electric field in the material increases the emission of SHG light. This effect, called Electric Field-Induced SHG, or EFISHG, can be used as a sensitive and precise method to measure internal electric fields in semiconductors. It may be used on planar wafers or patterned wafers. Because it is non-contact, non-destructive and fast—12 wafers per hour or more—it can be used to measure and monitor these internal fields.

The sensitivity of SHG light to internal fields is given by the second- and third-order permittivities of a material under with an internal electric field:

$$I^{2w} = (\chi^{(2)} + \chi^{(3)} * \mathbf{E}si)^2 * I^2 \text{, where:}$$

I^{2w} = second harmonic intensity; I = fundamental laser intensity
$\chi^{(2)}$ = second-order permittivity; $\chi^{(3)}$ = third-order permittivity
$\mathbf{E}si$ = internal electric field

Changes to the internal fields will therefore change the SHG signal. These changes can come from doping, strain, contamination, trapped charge or point defects in the device—anything that changes the internal local electric fields can change the SHG signal. For example, a change in threshold voltage, Vt, due to a shift in the fermi level in the semiconductor changes the electric field at the surface of the silicon. (Fig. 2) The change in electric field produces a change in the SHG signal, which is easily detected.

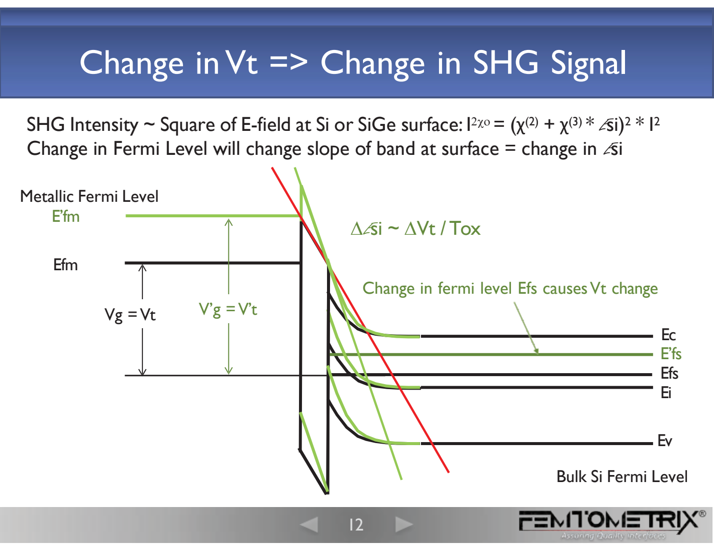

FIGURE 2. A change to the threshold voltage, Vt, arises from a shift of the Fermi level, Efs. This shift changes the electric field at the silicon-metal interface, aka band bending. This change in field in turn changes the second harmonic generated light coming from the silicon at the interface, $I^{2\mu}$. In this way, the change in SHG light may be used to measure changes to the threshold voltage of the device.

USE CASE: ADVANCED DRAM PRODUCTION

As a practical example, we compare SHG measurements versus spectral reflectometry after ion implantation. In an advanced DRAM FAB, Semiconductor wafers were implanted sequentially with five different ion species designed to modify the band structure at the Si/SiGe interface. Implant depths ranged from 10 nm to 600 nm. The

samples were measured after each implantation step. Sequential ion implantations modified the band structure, producing a corresponding change in SHG signal. The measurements over time on subsequently processed wafers is shown in fig. 3. The SHG signals show distinct changes due to each ion implantation, and these results are consistent over time. The changes represent changes to the band structure due to the doping. By comparison, spectral reflectometry results show considerably larger variations wafer-to-wafer, and are not well-separated. The SHG results may further be translated into dopant depth and concentration, and the defect density and dopant activation may be estimated both before and after annealing. The SHG results are from the Femtometrix G780, deployed at SK Hynix DRAM production facilities.

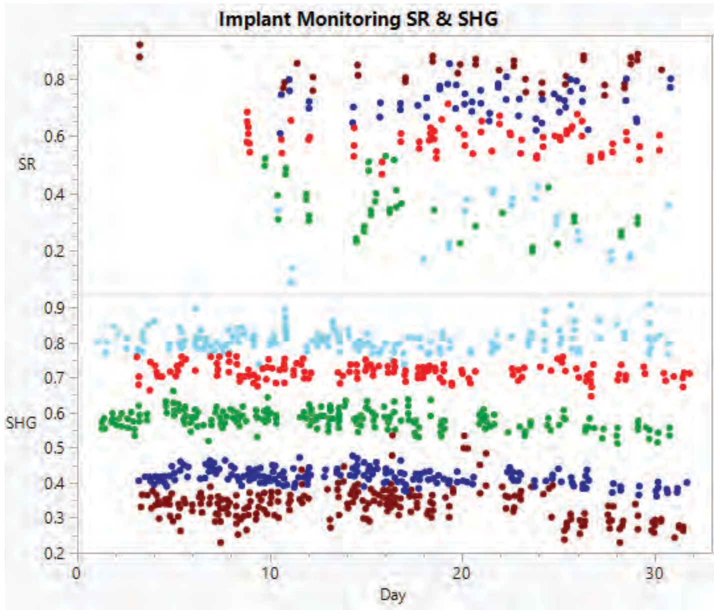

Fig. 3 Spectroscopic Reflectometry (SR) measurements (top) and SHG measurements (bottom) for ion-implanted wafers. Each color represents a different implantation process step. Implant depth range from 10 nm to over 500 nm.

In addition to monitoring ion implantation, SHG may be used to look for electrical changes due to: strain, diffusion, contamination, oxygen vacancies, under/over etch, and point defects. In order to differentiate between these effects, extensive non-linear modeling capabilities have been developed. Using these models, a model-based metrology method may be used to extract device parameters, including threshold voltage, implant depth and concentration, and critical dimensions.

KEYWORDS

Semiconductor Metrology, inspection, Second Harmonic Generation, SHG, interface engineering

Exploring Integrated Differential Phase Contrast for Enhanced 3D Imaging of Semiconductor Devices

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INTRODUCTION

In this work, we test a new method for determining the 3D structure of semiconductor devices, allowing us to visualize sub-volumes even when they're hidden beneath other materials—for example, the channel enclosed in the gate of CFET devices.

ABSTRACT

As the semiconductor industry transitions toward increasingly 3D device architectures to improve yield and performance, the need for accurate 3D metrology and fault analysis has become critical. This is especially true for foundries moving beyond the 3 nm node, where yield improvements depend on addressing challenges in Gate-All-Around (GAA), Forksheet, and Complementary Field Effect Transistor (CFET) technologies. Key process steps that often limit yield include channel SiGe recess, source/drain epitaxial growth, channel SiGe release, and replacement gate removal.

While tomography is a well-established technique capable of providing 3D structural and chemical information (including EDS tomography) with nanometer-scale resolution, it has important drawbacks. Volume reconstruction requires specialized expertise, stage or sample drift can distort the data, and acquisition times typically exceed an hour—delivering an electron dose that's often too high for advanced devices. Our goal in this study is to explore a simpler, faster, and lower-dose method that still achieves high-precision 3D metrology.

Building on recent advances in depth sectioning[1], we evaluate the potential of through-focus Integrated Differential Phase Contrast STEM[a] (iDPC-STEM) as a new approach for visualizing the 3D structure of semiconductor devices. Our focus is on CFET devices after gate deposition, where obtaining a full 3D view of the gate volume (~55–60 nm) is essential to assess structural integrity.

We compare the structural information obtained from iDPC-STEM with that from conventional microscopy methods such as S//TEM[a] imaging and EDS[b] mapping). Our results show that iDPC-STEM reveals significantly more detail because it allows imaging of buried sub-volumes without interference from the surrounding materials. We demonstrate that 3D imaging of $80 \times 80 \times 4$ nm sub-volumes can be routinely achieved at 200 kV, and that full $80 \times 80 \times 55$ nm volumes can be recorded and processed in about 10 minutes.

Finally, we present the underlying principles of depth information recovery, discuss the parameters that determine depth resolution, describe our data processing workflow for 3D visualization, and outline the current limitations of the method.

[a] STEM: Scanning Transmission Electron Microscopy; TEM: Transmission Electron Microscopy
[b] EDS: Energy Dispersive Spectroscopy

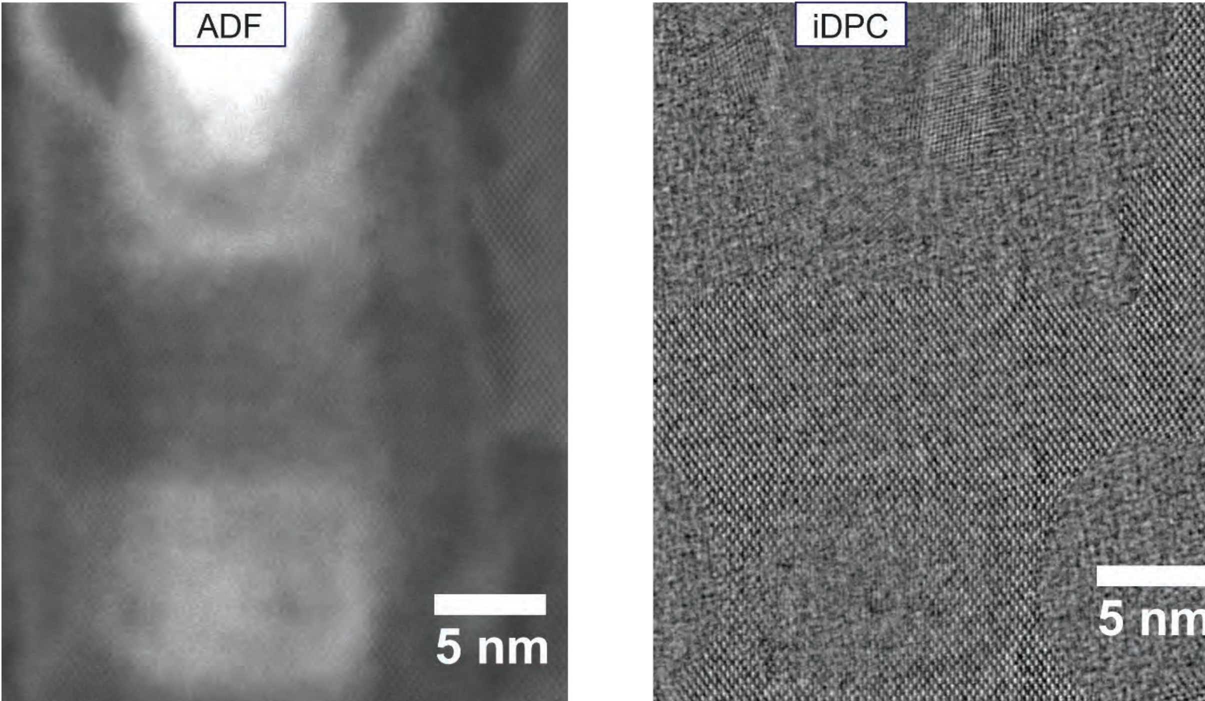

FIGURE 1. Comparison of simultaneously acquired traditional dark-field STEM and iDPC images. The iDPC image clearly reveals the channel structure, even though it is enclosed within the gate metal. In contrast, the dark-field STEM image primarily highlights the positions of the gate metal and channel with limited structural detail. Together, these images provide a complete view of the device architecture

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KEYWORDS

3D imaging, Transmission Electron Microscopy, 3D metrology, 3D visualization

StrataPHI for Thin Film Surface & Interface Engineering: Depth-Resolved, Non-Destructive Analysis of Layered Materials

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INTRODUCTION

Next generation engineered materials increasingly demand new approaches, as insights into ultra-thin films, surfaces, and interfaces are often obscured by the limitations of even traditional surface analysis techniques. As material systems become more complex, the need for precise, depth-resolved characterization of layered structures is critical for understanding performance, reliability, and process control. Strata*PHI* introduces a next-generation characterization platform designed for non-destructive analysis of multi-layer films composed of ultra-thin layers.

By leveraging X-ray photoelectron spectroscopy (XPS) and hard X-ray photoelectron spectroscopy (HAXPES), StrataPHI extracts key processing-dependent material parameters such as thickness and composition across stacks extending up to 30 nm beneath the surface. Figure 1 demonstrates that Strata**PHI** model of HAXPES data can accurately determine the thickness of Al_2O_3 gate oxides in GaN/AlGaN HEMT devices, even for relatively thick layers (up to 30 nm).

Al_2O_3 Thickness, nm

nominal	*HAXPES*
5 nm	4.5
10 nm	8.2
20 nm	18.9
30 nm	27.8

Structure of 20 nm Al_2O_3 film modeled using *StrataPHI*

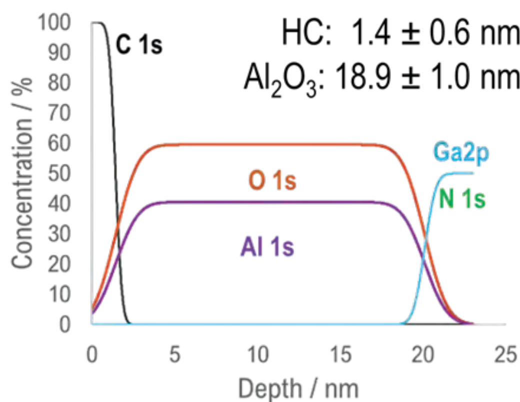

FIGURE 1. The table and graph show that measured thicknesses by HAXPES closely match nominal values.

Fractional coverage analysis in Strata*PHI* also enables detection of partial film formation and interface quality such as incomplete Al_2O_3 growth, which is essential for optimizing atomic layer deposition (ALD) and other advanced coating processes. Figure 2 shows the thickness and coverage of ALD layers calculated from ADXPS data using Starat*PHI*. There are several advantages of using this approach in comparison to standard ISS or LEIS methodologies. The Strata*PHI* analysis is non-destructive, allowing the sample to be easily analyzed afterward by additional techniques. ISS is extremely sensitive to surface contaminations, requiring heating/thermal oxygen

bombardment to remove adsorbed hydrocarbons. Starat*PHI* can calculate coverage without requiring a blank substrate, which simplifies the process and reduces preparation time. It can calculate coverage from variable areas as defined by the X-ray probe size, while ISS data are limited to one size defined by ion beam probe used. StrataPHI can be applied to a large range of layer thicknesses, while ISS is limited to coverage from a monolayer thick film. Strata*PHI* provides simultaneous individual layer thickness and fractional coverage analysis, offering comprehensive insights in a single test.

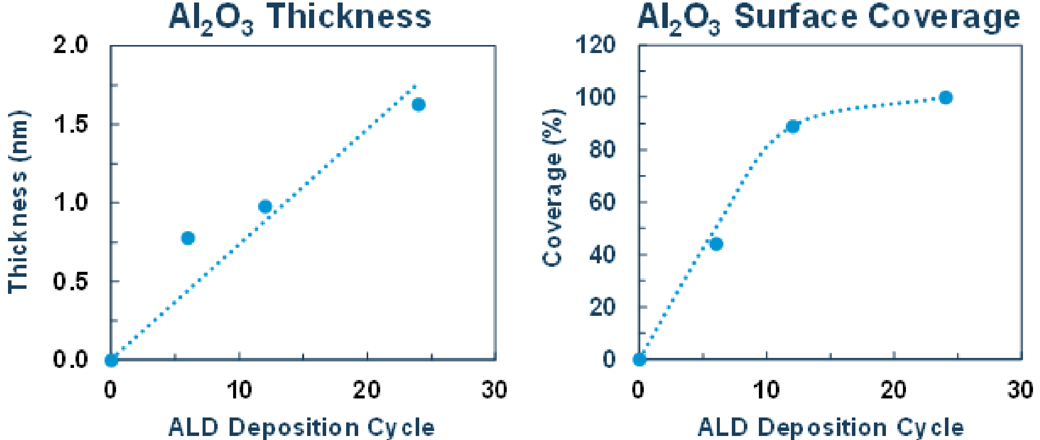

FIGURE 2. Al_2O_3 thickness and coverage calculated by StrataPHI as a function of deposition cycle.

The newest StrataPHI platform introduces an integrated analyzer acceptance angle mode that builds on the traditional model of a single photoelectron escape angle from the surface by including all escape angles as detected by the analyzer. This enables Strata*PH*I's application in engineered materials, delivering reliable thickness measurement of individual layers in a multi-layer thin film, equivalent to thicknesses traditionally obtained via angle-resolved XPS. The latest version of StrataPHI also enhances automated, real-time batch processing and full traceability of the relationship between material and processing parameters.

This presentation will demonstrate how StrataPHI enables researchers and engineers to model complex ultra-thin film stacks and extract insights into process-induced variations using its real-time batch processing capability, providing a comprehensive materials characterization suite for a deep understanding of ultra-thin films as well as their surfaces and interfaces.

KEYWORDS

XPS, HAXPES, thin films, thickness, coverage

Posters

Enhancement of Passive Voltage Contrast Using a Newly Designed Electron Energy Filter in a Scanning Electron Microscope

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INTRODUCTION

Passive voltage contrast (PVC) is typically observed using scanning electron microscopy (SEM) and is widely employed for semiconductor failure analysis [1,2]. In PVC, the connection status of metal plugs and the regions of PN junctions can be evaluated by detecting secondary electrons (SEs) generated under an accelerating voltage of approximately 1 kV during SEM observation. However, optimizing the conditions for PVC is challenging because they depend on both the surface condition of the sample and the energy distribution of the SEs used for imaging.

In our previous study [3], we investigated the fundamental properties of PVC and found that SEs with energies in the range of 4–12 eV, emitted from W plugs surrounded by insulating films, exhibited distinct contrast. Typically, an immersion-type objective lens is used in SEM to efficiently collect SEs via a magnetic field.

In the present study, we conducted imaging using an SEM equipped with this electron energy filter, a high-efficiency detector, and a semi-in-lens objective lens to effectively capture the targeted electrons. This configuration significantly improved the visualization of electrically isolated regions and subtle defects in semiconductor devices, thereby enhancing the effectiveness of failure analysis.

METHOD

The samples were prepared using Ar ion beam milling (JEOL IB-19530CP) equipped with a rotation holder. PVC observations were performed at an ion acceleration voltage of 8 kV with an irradiation angle of 3°–4° for approximately 20–35 minutes, depending on the layer thickness. This process produced a flat surface with a diameter exceeding 200 μm, suitable for PVC imaging.

In this study, a semi-in-lens scanning electron microscope (JEOL JSM-IT810<SIL>) was used. This microscope is equipped with an advanced detection system capable of collecting both secondary electrons (SEs) and backscattered electrons (BSEs). Figure 1 shows the PVC information acquired by the detectors. Notably, the Upper In-lens Detector (UID) is particularly effective for detecting low-energy SEs in the range of 0–8 eV because it utilizes the magnetic field in the semi-in-lens system. To obtain clear PVC images, we employed the UID in this study.

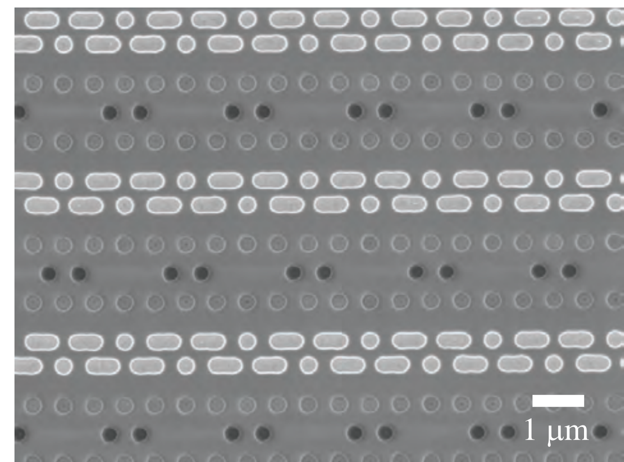

Figure 1. Typical PVC image was taken at 0.8 kV.

An electron energy filter optimized for PVC observation was developed based on our previous findings [1] and integrated into the SEM objective lens. By applying a potential to the electrodes installed within the objective lens to suppress low-energy SEs, an effect equivalent to applying a bias voltage to the sample surface can be reproduced. This approach enables clearer PVC observation. A schematic diagram is shown in Figure 2. By establishing a negative electrostatic field on the filter electrode, low-energy SEs can be effectively removed. Furthermore, the voltage can be finely adjusted in 0.1 V increments, allowing the optimal imaging conditions to be precisely tuned for each sample.

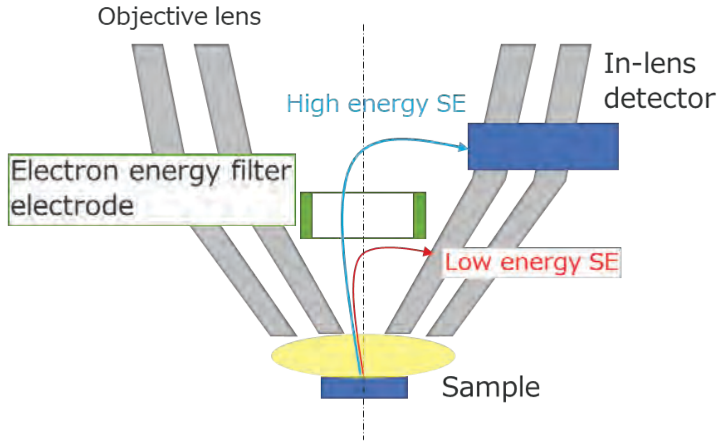

Figure 2. Schematic diagram of PVC filter.

RESULT AND DISCUSSION

1. Sample preparation

We observed surface contamination on two samples that were prepared using chemical mechanical polishing (CMP) and Ar ion milling, respectively.

Figure 3 shows the PVC images of these samples. First, the sample surfaces were observed at higher magnification using SEM, followed by observations at lower magnification. The PVC images revealed that the contamination on the sample prepared by Ar ion milling was significantly lower than that on the sample prepared by CMP. This difference in contamination level was clearly reflected in the brightness and uniformity of the PVC contrast.

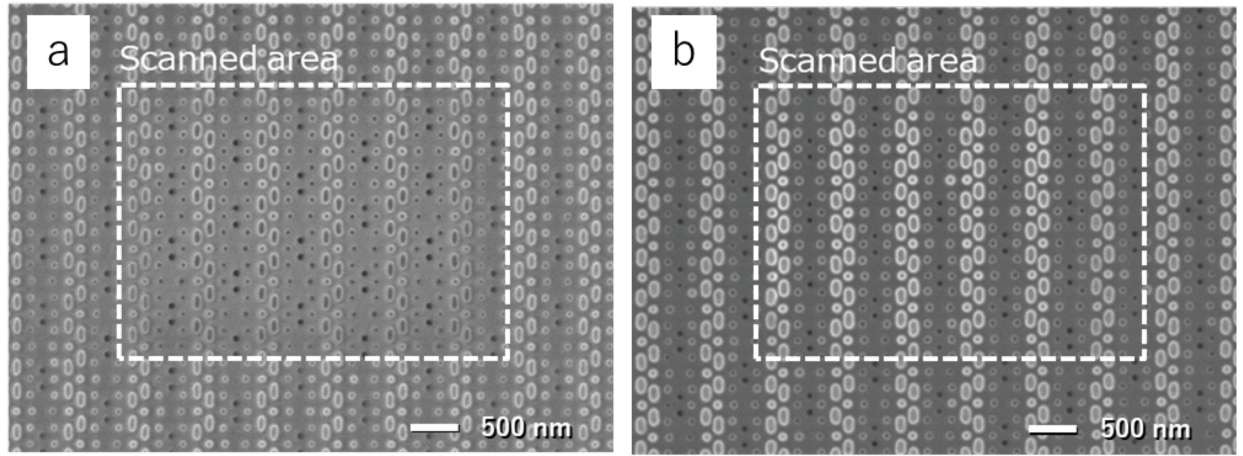

Figure 3. Comparison of PVC images obtained from samples prepared by (a) chemical mechanical polishing (CMP) and (b) Ar ion milling.

2. Electron energy filter

We observed a sample prepared by delayering and polishing using Ar ion milling. The observation was performed at an accelerating voltage of 0.8 kV, a beam current of 100 pA, and a working distance (WD) of 8 mm, as shown in Figure 4.

Although PVC could already be observed under standard conditions, the newly developed electron energy filter significantly reduced charging effects when a filter bias of –1.0 V was applied (Figure 4). Furthermore, the reduced contrast at the edges of the tungsten plugs enabled clearer identification of the PVC. Figures 4(a) and 4(b) show

magnified areas with corresponding line profiles. In contrast, in Figure 4(b), the higher intensity at the plug edges results in lower contrast between the plugs and the substrate.

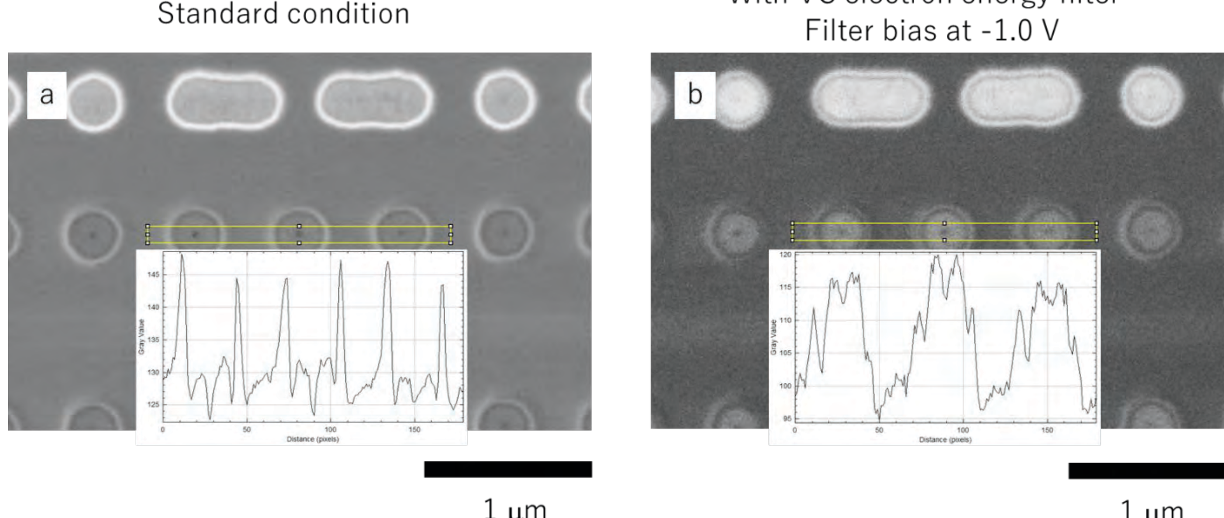

Figure 4. Effect of the Electron Energy Filter on PVC Observation.

In this study, we used an electron energy filter mounted on a SEM for observing PVC in a semiconductor chip. In addition, we determined the optimal preparation and conditions for PVC imaging using a semi-in-lens scanning electron microscope. To this end, we applied a negative bias in electron energy filter, which enabled enhanced PVC. Moreover, surface contamination of the sample was reduced by adopting the Ar ion milling method. We believe that the method proposed in this work will be applicable for observing PVC in next-generation semiconductor chips as well.

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KEYWORDS

Scanning electron microscope (SEM), Passive voltage contrast (PVC), Electron energy filter, Auger electron spectrometer (AES)

Denoising of multispectral images by PCA-assisted self-supervised deep learning

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INTRODUCTION

Among multispectral imaging techniques, Secondary Ion Mass Spectrometry (SIMS) is a potent method for investigating the spatial distribution of elements and molecules within a sample. Modern SIMS instruments can achieve sub-100 nm lateral resolution, with some capable of resolving features below 20 nm[1]. Time-of-Flight SIMS (TOF-SIMS) generates multispectral datasets, typically comprising either three dimensions (two spatial and one spectral) or four dimensions when depth profiling through sputtering or analyzing serial sections. Unlike electron or optical microscopy, TOF-SIMS images often exhibit a low signal-to-noise ratio (SNR), which can hinder image interpretation. Consequently, substantial efforts have been directed towards developing instruments with enhanced lateral resolution and sensitivity[2]. However, obtaining high lateral resolution and high chemical sensitivity simultaneously is physically constrained. As lateral resolution increases, the sampled volume decreases, reducing the number of analytes per pixel. This results in shot noise or Poisson noise, ultimately compromising sensitivity.

Various methods have been proposed to denoise SIMS data, including binning and wavelet-based techniques. These methods, while efficient and high-fidelity, often reduce lateral resolution. Mass spectrometry images are multispectral, sharing spatial patterns that enable clustering and classification. Dimensionality reduction methods like Principal Component Analysis (PCA) and Non-negative Matrix Factorization (NMF), along with clustering techniques such as k-means and t-SNE, are commonly used. These methods can be combined and are increasingly used with neural networks and deep learning.

Other imaging fields, such as astronomy and biological imaging, also face high noise issues. In 3D fluorescence live-cell imaging, quick acquisition and low beam intensity result in low-count, Poisson-noise-corrupted images. Deep learning methods, particularly Noise2Void (N2V), have shown significant success in denoising these images without requiring ground truth data. N2V masks pixels and learns to distinguish noise from signal using neighboring pixels.

However, the performance of N2V and similar methods decreases with poorer input quality. MSI images have high spatial correlation, which can be leveraged for more efficient denoising. Building on these advances, a new method called Principal Component Assisted Noise2Void denoising (PCA-n2v) combines PCA with self-supervised deep learning[3]. This approach aims to enhance the denoising of TOF-SIMS images, aiding in data interpretation.

Implementation of Principal component assisted Noise2Void denoising

To evaluate PCA-n2v, it was benchmarked against common denoising methods such as down-binning, Gaussian filtering, and Block-Matching and 3D Filtering (BM3D) on a ground truth dataset created from noise-free synthetic images. Down-binning and Gaussian filtering, while faithful to original data, degrade lateral resolution. PCA-n2v

was found to significantly improve the signal-to-noise ratio (SNR) and image quality, surpassing the Peak Signal-to-Noise Ratio (PSNR) of 4x4 data binning but without losing original lateral resolution. PCA-n2v outperformed other methods, providing smoother and more resolved images. It enabled the identification of small image features. This improvement pushes the lateral resolution and sensitivity of TOF-SIMS, or allows for shorter acquisition times and thus higher throughput experiments.

While PCA-n2v improved image quality, it sometimes introduced artifacts due to the linear combination of original images in the PCA decomposition. These artifacts can mislead image reconstruction, inducing biases. Applying Noise2Void directly to single 2D images provided an intermediate solution, avoiding bleedthrough artifacts but with lower resolution improvement and some morphological artifacts. The PSNR metric was not indicative of artifact presence. Given the challenges of denoising very noisy data, it is crucial to critically evaluate PCA-n2v results. Visual comparison with binned data is recommended to validate the outcomes. Users should be cautious and perform thorough checks, especially when dealing with highly noisy datasets.

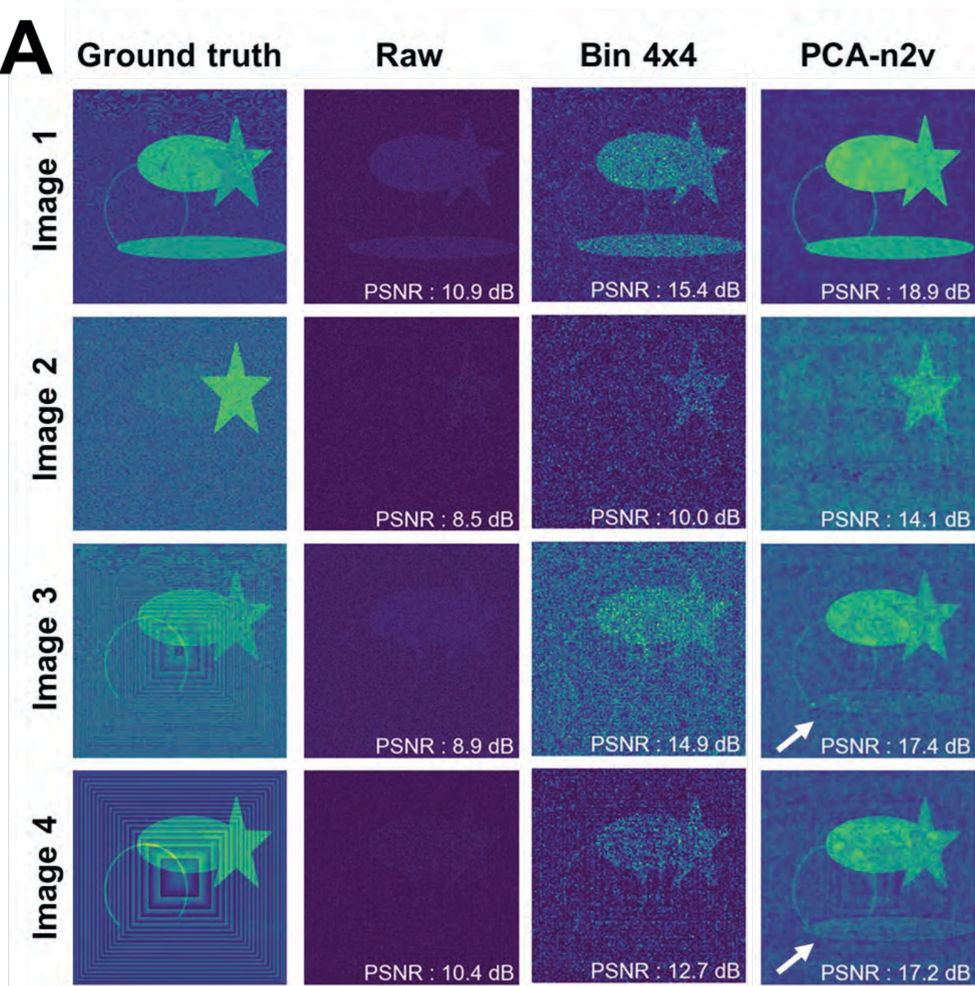

FIGURE 1. PCA-n2v compared to the synthetic ground truth image, raw image and 4 x4 binned image for four different slices in the multispectral data cube. White arrows indicate bleed through artefacts from other slices.

This paper introduces PCA-n2v, a method combining Principal Component Analysis (PCA) and Noise2Void denoising tailored for the multispectral nature of SIMS imaging to improve image quality. The method's limitations were tested using a synthetic dataset, highlighting the need for careful application. PCA-n2v enhances lateral resolution in MSI without requiring additional instrumental developments, enabling high-resolution and faster

imaging. This improvement facilitates subsequent processing steps like clustering and segmentation. The method shows promise for denoising images from other spectral imaging techniques, such as electron microscopy and X-ray photoemission spectroscopy, although further investigation is needed for each application. The approach offers a powerful tool for advancing MSI and related imaging fields, but users should be mindful of its limitations.

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KEYWORDS

Denoising, Secondary Ion Mass Spectrometry, self-supervised deep learning, multispectral imaging

Workflow Automation For High Volume TEM Data Production

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INTRODUCTION

Modern semiconductor process development and production are driving the demand for atomic-scale transmission electron microscopy (TEM) data to new heights. Critical features on the latest generation memory and logic devices have shrunk below the ability of SEM-driven conventional metrology techniques, requiring significantly more resolution to provide process feedback.[1] Addressing the challenge of rapidly scaling TEM laboratory operations while maintaining high efficiency and productivity is crucial. The Thermo Scientific Vulcan Automated Lab (VAL) offers a comprehensive, scalable solution for addressing the challenges of modern TEM data production, ushering in a new era of atomic-scale data acquisition. The Vulcan Automated Lab features a seamlessly connected, AI-powered TEM metrology workflow, bridging the gap between the lab and the fab. This innovative system enhances productivity by delivering high-volume data of exceptional quality while reducing operator burden through advanced on-tool automation, materials handling automation, and continuous data connectivity.

WORKFLOW SOLUTION

The Vulcan Automated Lab builds upon Thermo Fisher's existing portfolio of semiconductor sample preparation and imaging instruments to enable automated material handling and logistics for wafers, individual sample die, and TEM samples. Vulcan Automated Lab integrates a SEMI E177 complaint TEM grid (Lamella Carrier) EFEM to enable automated handling of TEM samples for preparation and imaging instruments. The integrated EFEM allows for full traceability of samples throughout the prep and imaging workflow. Traditional TEM data production relies on significant manual intervention in both operation of the instruments set as well as moving samples between tools to produce the final dataset. Automation of data and material handling enables sampling of nanoscale structures in the S/TEM without the requirement of operator presence, at statistically significant volumes required for modern devices.[2]

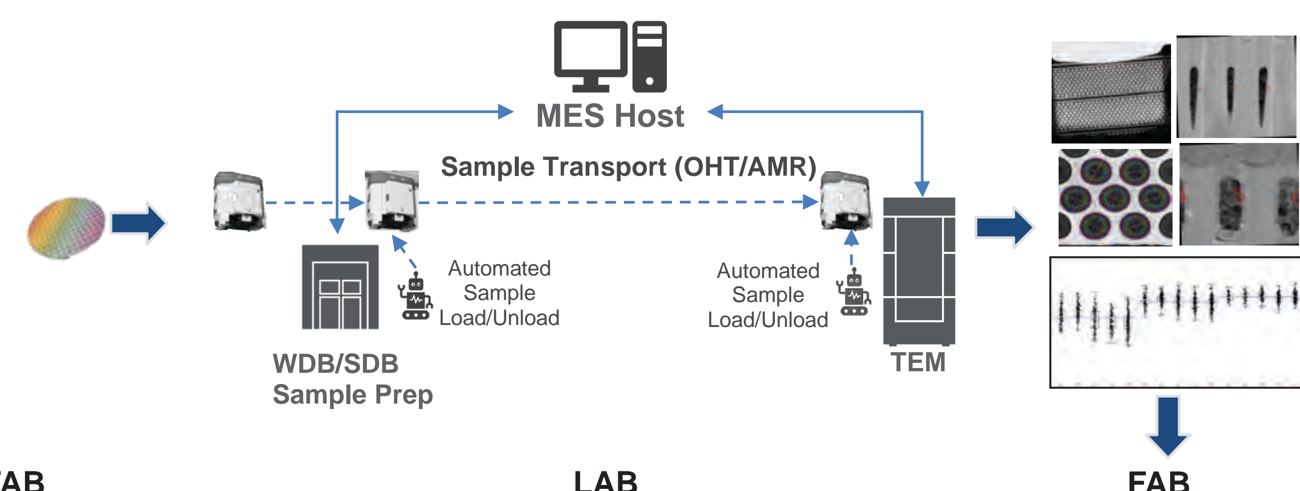

FIGURE 1. Workflow elements in the Vulcan Automated Lab.

When selecting/preparing a region for cross-sectional imaging in the S/TEM two figures of merit are used to describe the physical characteristics of the sample production process: Lamella Centering Accuracy (LCA) describing the measurement of the target feature relative to the center of the produced lamella, and Lamella Thickness Accuracy (LTA) relating the overall lamella thickness variation in the region of interest.

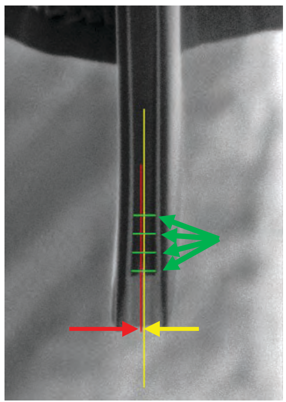

FIGURE 2. Cross-section image of a TEM lamella showing LTA (green) and LCA (yellow-red) measurements

Historical approaches to cut placement relied on passive control of the cut face, where the milling system is aligned, a cut is called for, and the resultant cut face incorporates both placement error and any subsequent drift that occurs during the mill. The combination of cut face inaccuracy on both sides of the lamella contribute to both LCA and LTA error. These placement and thickness errors in turn have implications for the maximum allowable thickness to ensure the full removal of any neighboring obscuring material.[3] Vulcan Automated Lab introduces active cut face control during sample preparation steps to reduce LCA and LTA figures, allowing better control of sampling volume needed for smaller process geometries. Active, AI-guided endpointing has demonstrated significant improvement in cut placement control and associated LCA/LTA figures compared to historical capabilities.

TABLE 1. Typical Cut Placement Capabilities for TEM sample preparation

Preparation Method/System	Typical LCA	Typical LTA
Manual Sample Preparation on Helios EXL	6nm, high operator dependance	6nm, high operator dependance
ExSolve G2 Automated TEM Sample Preparation	<4.4nm	<3.6nm
Vulcan Active Endpointing	<1.7nm	<1.5nm

Fully automated, AI-driven sample preparation has been demonstrated down to <18nm final thicknesses with automated endpointing at lowkV FIB polishing steps on both memory[4] and logic devices. In addition to overall process performance, high levels of process automation improve data reliability and mitigation of human errors. [5]

CONCLUSION

The Thermo Scientific Vulcan Automated Lab represents a significant advancement in the field of atomic-scale transmission electron microscopy (TEM) data acquisition. By integrating AI-driven automation and advanced materials handling, Vulcan Automated Laboratory addresses the critical challenges of scaling laboratory operations while maintaining high efficiency and productivity. The seamless integration of automated sample preparation,

imaging, and data traceability enhances lab productivity and enables scalable data production for modern semiconductor manufacturers.

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KEYWORDS

Automated, Workflow, Sample Preparation, TEM, process control, TEM metrology, Machine learning, Material Handling

Balancing Speed, Damage, and Fidelity: A FourMethod TEM Prep Study on GaN Devices

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INTRODUCTION

IIIV materials such as GaN, GaAs, InAs and InP offer electronic and optical properties far superior to silicon for certain applications. These materials have direct bandgaps, high electron mobility, and tunable properties, making them ideal for optoelectronics (LEDs, lasers) and highfrequency devices[1] . While silicon is cheap and the silicon wafer infrastructure is already well developed, III–V materials are taking over in places where performance, speed, and efficiency matter more than cost. They're the foundation of nextgen communications, power electronics, photonics, and quantum devices, the fields shaping the future of technology.
Gallium nitride (GaN) has emerged as one of the most important III–V semiconductors due to its exceptional combination of wide bandgap strength, high electron mobility, and thermal stability[2] . These attributes enable efficient, highvoltage operation and support compact, highpower device architectures. Its ability to sustain a twodimensional electron gas at the AlGaN/GaN interface provides fast switching speeds and low onresistance, making it ideal for highfrequency and highefficiency electronics. Additionally, GaN's direct bandgap and blueUV emission capability underpin its dominance in solidstate lighting, laser diodes, and microLED displays. Combined with its thermal robustness, radiation resistance, and compatibility with silicon and SiC substrates, GaN has become a key material driving innovation across power electronics, RF communications, optoelectronics, and nextgeneration display technologies.
Transmission electron microscopy (TEM) is a vital tool for evaluating the structural integrity, defect density, and interfacial quality of GaN films. However, achieving artifactfree TEM lamellae with conventional preparation methods remains challenging. Focused ion beam (FIB) thinning using a traditional gallium liquid metal ion source (LMIS) can introduce redeposition and elemental contamination[3] .
To minimize these artifacts, many researchers have turned to plasma FIB (PFIB) systems using xenon (Xe) or argon (Ar) ions, which eliminate gallium implantation and related defects. In fact, manufacturers of PFIB instruments often highlight GaN TEM preparation as one of the most compelling value propositions for adopting PFIB technology[4] . However, due to the larger beam spot size, PFIB methods are slower, more difficult to control, and can increase curtaining artifacts. Like attempting to draw a fine line with a thick marker, the PFIB beam is inherently less precise for the delicate final thinning stages of TEM preparation.
Despite these challenges, both LMIS FIB and PFIB approaches can produce highquality lamellae on GaN samples that reveal structural information with atomic resolution. This study directly compares four preparation workflows using both PFIB and Ga LMIS FIB instruments on a sample which consists of a multichannel epitaxial stack alternating between nAlGaN and UIDGaN, grown by NTT. Multichannel GaN transistors are important for nextgeneration power and RF electronics due to their reduced sheet resistance versus single channel devices. The sample represents technology at the forefront of GaN device research. The aim of this study is to determine whether PFIBbased TEM preparation truly provides meaningful improvements over optimized Ga FIB workflows.

BACKGROUND

When a focused gallium ion beam irradiates a GaN substrate, metallic droplets can form on the surface. Previous studies have reported similar droplet formation across a range of III–V compound semiconductors, including GaAs, InAs, InP, and GaN[5,6] . This phenomenon occurs because group V elements are preferentially sputtered during ion milling, leaving behind an excess of group III elements. Once the local concentration of group III atoms on the surface exceeds a critical threshold, the focused ion beam promotes their recombination into metallic droplets. These droplets have been confirmed to consist of highpurity gallium or indium.[6]

Ion Source Comparison

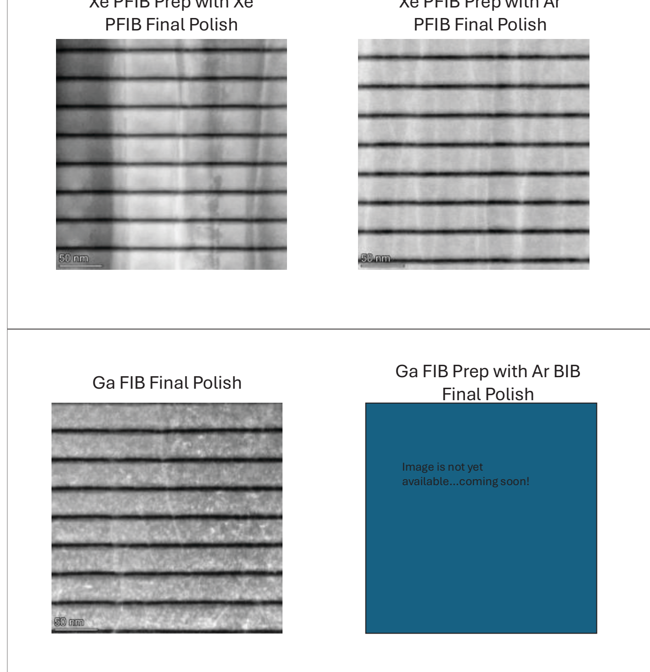
Different ion sources alter the balance between speed, damage, and contamination:

Source for Final Polish	Key Benefits	Key Drawbacks
Ga FIB	Precise, fast, widely available	Surface droplets
Xe PFIB	No Ga contamination, fast bulk milling	Larger beam, slow thinning, curtaining artifacts
Ar PFIB	Gentle, reduced amorphization	Slow sputter rate, curtaining artifacts
Ar BIB	Gentle post-polish for large areas	Not site-specific, low throughput

PFIB vendors frequently promote TEM preparation of GaN samples as a “killer application” for the technology. While PFIB-prepared GaN lamellae can indeed exhibit cleaner surfaces and reduced implantation damage, the overall process is more time-consuming, fine-thinning is more difficult, and curtaining artifacts remain common due to the inherently larger beam spot size of PFIB systems. This study investigates whether PFIB is really necessary for GaN devices or whether well optimized methods on a Ga FIB will suffice. We also investigate the impact of preferential milling of certain chemicals from each different ion species.

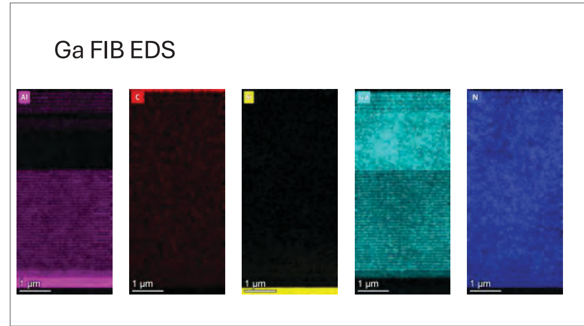
Results and Discussion

STEM Image Comparison



The figures above compare representative STEM micrographs for the four workflows. Xe PFIB finishing yields a fairly thick sample with some dramatic curtaining artifacts. Ar PFIB finishing mitigates some of the curtaining artifacts to create a relatively smooth final surface this is thinner. Ga FIB finishing yields a thin sample with no curtaining artifacts, however droplet artifacts are apparent on the surface. Ga FIB prep with Ar BIB polishing is likely to yield the smoothest, thinnest, least damaged lamella, with the least amount of operator time.

EDS Comparison



Argon BIB EDS Results

- Result not available yet...coming soon!

When comparing the EDS maps from the two PFIB-prepared lamellae to those from the Ga FIB lamella, the Ga FIB sample appears noticeably grainier and exhibits distinct gallium droplets on the surface. This difference may partly result from the Ga FIB lamella being thinner than the PFIB-prepared ones. While thinner lamellae are advantageous for achieving high-resolution STEM imaging, EDS analysis benefits from a somewhat greater sample thickness, which provides sufficient interaction volume for X-ray generation and results in smoother, higher-quality elemental maps.
Surprisingly, the Xe-PFIB lamella produced a noticeably crisper nitrogen EDS map when compared to the Ar-PFIB lamella. This improvement could arise from the higher mass of Xe ions, which remove material more efficiently and with reduced preferential sputtering of nitrogen compared to Ar. Xe's higher mass gives it a more balanced sputtering yield for both Ga and N, removing them more stoichiometrically.
Low-energy Ar milling is excellent for surface cleaning, but if it's applied at an angle or for too long, the preferential sputtering of N reduces the N signal uniformly and makes maps look "washed out."
Alternatively, the Al map looks much crisper in the Ar-PFIB lamella. This follows logically from the conclusion we drew above about preferential sputtering of N by Ar. After Ar polishing, the surface becomes slightly N-depleted and Al-enriched. That local enrichment of Al at the surface gives a stronger and more surface-localized Al signal, making the EDS Al map appear crisper.

CONCLUSIONS

This study compared four TEM lamella preparation workflows for GaN devices using Ga FIB, Xe PFIB, Xe PFIB with Ar PFIB final polishing and Ga FIB with Ar BIB final polishing. Each approach presented a distinct balance between speed, precision, and surface integrity. The Ga FIB workflow produced the thinnest lamellae with high imaging resolution but suffered from surface gallium droplets and elemental contamination. Adding an Ar BIB post-polish effectively mitigated these effects, yielding the smoothest and least damaged lamellae with minimal operator time.

Among the PFIB-based methods, Xe and Ar produced markedly different chemical mapping results. Xe PFIB finishing generated the crispest nitrogen EDS maps, attributed to the high mass and inert nature of Xe ions, which sputter Ga and N more stoichiometrically and minimize nitrogen depletion. In contrast, Ar PFIB finishing yielded

sharper aluminum maps, likely due to preferential sputtering of nitrogen that produced slight Al enrichment at the surface.

Overall, Xe PFIB provided the most chemically faithful lamellae, while Ar PFIB and Ar BIB finishes offered valuable advantages for reducing curtaining artifacts and smoothing surfaces. For high-throughput imaging or general failure analysis, Ga FIB with Ar BIB polishing remains the most practical workflow. However, for chemically sensitive studies of GaN interfaces and stoichiometry, Xe PFIB finishing provides the highest fidelity in elemental contrast.

Acknowledgments
We thank CAMCOR and Covalent Metrology for access to FIB, PFIB and TEM instrumentation, and MIT for providing the sample.

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KEYWORDS

GaN, AlGaN, III–V semiconductors, focused ion beam (FIB), plasma focused ion beam (PFIB), gallium contamination, Xe PFIB, Ar PFIB, Ar broad ion beam (BIB), TEM sample preparation, lamella thinning, EDS mapping, sputtering yield, curtaining artifacts, gallium droplets

Interlaboratory Evaluation of Optical Homogeneity in Two-Dimensional Semiconductors

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INTRODUCTION

Two-dimensional (2D) semiconductors feature prominently on industry roadmaps as channel materials in advanced-node CMOS within the next decade [1]. Their adoption requires the development of novel deposition and processing techniques, supported by appropriate metrology for characterization and quality assurance. Measuring optical homogeneity at scale is a critical challenge that must be addressed quantitatively and standardized to enable process optimization and supply chain reliability. Photoluminescence (PL) spectroscopy is a key optical technique for probing carrier dynamics and material quality in 2D materials, including transition metal dichalcogenides. Current PL characterization relies on point spectroscopy, which cannot easily capture spatial variability across large areas. To meet industry needs, metrology must evolve towards imaging-based approaches that provide comprehensive spatial and spectral insights.

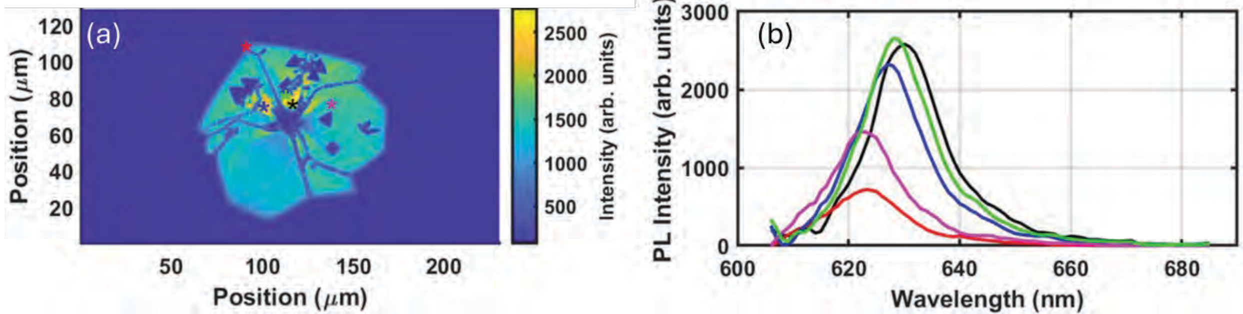

Figure 1 Spectral imaging measurement of CVD-grown WS_2, (a) image of peak intensity per pixel, (b) photoluminescence spectra for individual pixels, where colored stars indicate locations in (a) plotted in (b).

Hyperspectral imaging marks a major shift in metrology, delivering micrometer spatial resolution and nanometer spectral resolution at wafer scale. Using an in-house hyperspectral imaging system, we recently demonstrated rapid and spectrally resolved PL-imaging for 2D materials. Figure 1(a), shows a CVD-grown WS_2 monolayer, flake diameter approximately 100 µm with sub-domain defects separated by line boundaries, imaged at 50x magnification. The dataset contains over two million spectra, each with ~100 wavelength channels, five example are shown in Figure 1(b). Such high-dimensional data cube demands statistical and data-driven tools to extract parameters relevant to material quality and device performance. Measurement conditions such as laser power and integration time also influence results and must be standardized. Current international standards [2] require only point spectroscopy at three sample areas, offering no guidance on quantifying spatial variations critical for assessing 2D materials quality.

Posters

INTERCOMPARISON STUDY

In response to this challenge, an interlaboratory round-robin comparison project was initiated to understand the repeatability of a recently proposed method [3] for measuring spatial homogeneity in 2D materials, via spectral analysis of PL maps. Homogeneity metrics are statistically derived from confocal PL mapping [4]. This study is supported by the Versailles project on Advanced Materials and Standards (VAMAS). Several CVD-grown WS_2 flakes were distributed along two parallel paths: Europe/UK and Asia/Americas, engaging 14 institutions, including metrology institutes, tool suppliers and universities. Each lab received two flakes, one for measurement and one as a reference, the latter measured only at the start and end to capture transport-related degradation.

PL mapping was performed under controlled, pre-agreed conditions, including laser wavelength and power, spectral range, grating, objective NA, integration time, spectral accumulation number, mapping area and step size, with instrument-specific spectral corrections applied. Figure 2(a-c) shows a PL intensity map from a flake measured on the Europe/UK path and two representative spectra. Each pixel spectrum was fitted using a two-Voigt model to

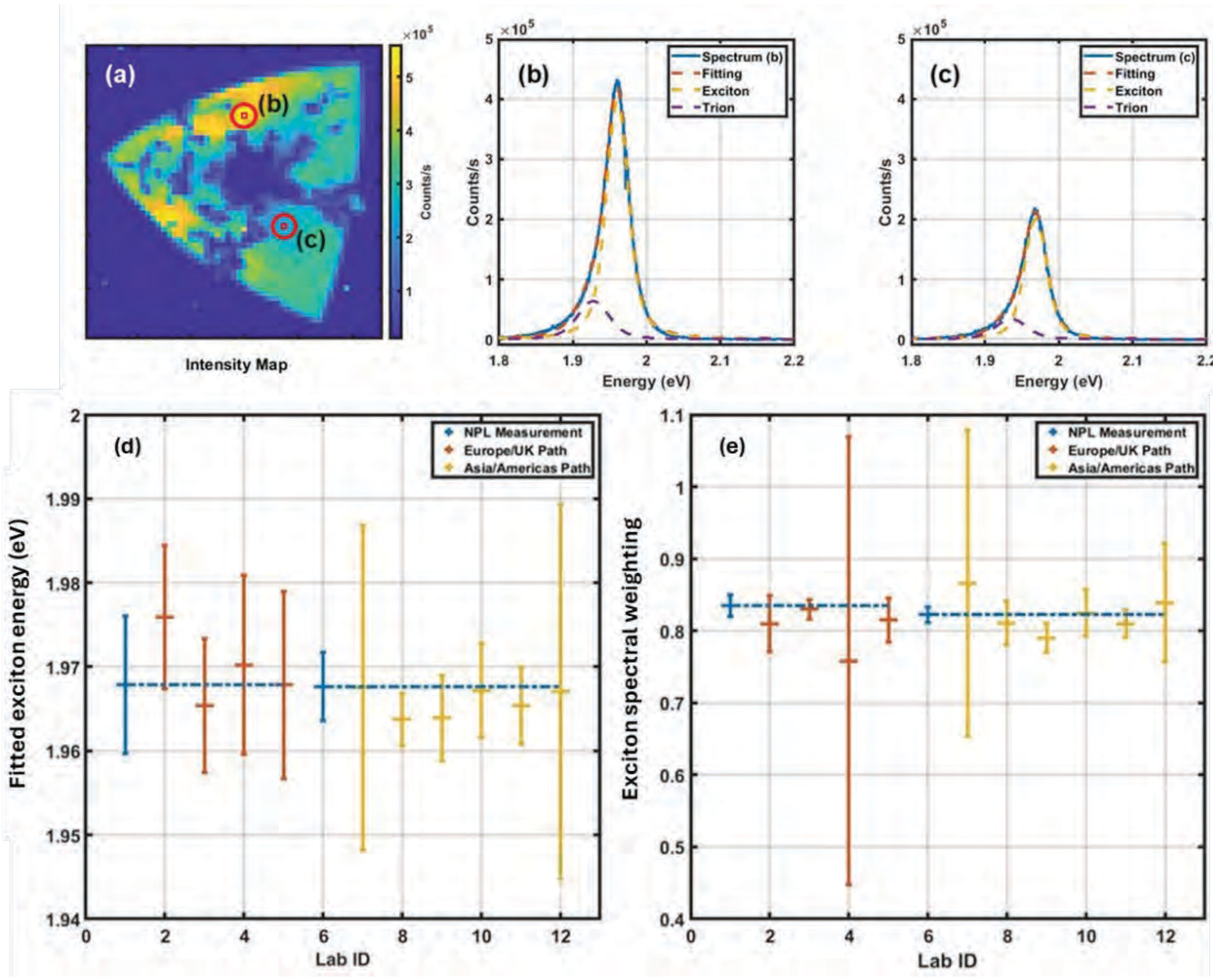

Figure 2 (a) Map of peak PL intensity for the sample used on the Europe/UK path (scale bar corresponds to 10 μm), with full spectra from two selected pixels plotted in (b) and (c), the fittings in each plot correspond to exciton and trion emission peak modelling using a Voigt function. Statistical quantities (mean as data point, standard deviation as error bars) of the fitted exciton energy and exciton spectral weighting from each lab-measurement, in order of progression, are represented in scatter plots (d) and (e) respectively, in each case the first measurement taken at NPL is used for reference data (indicated with the blue dashed line).

account for lifetime and inhomogeneous broadening, yielding parameters such as exciton energy and spectral weighting. Aggregating these fits across all mapped positions produced homogeneity metrics (mean and standard deviation) for each lab. Figure 2(d,e) plots exciton energy and spectral weighting homogeneity against lab sequence. This study has spanned 2.5 years and will conclude in early 2026. Variations in the measurand, shown in Figure 2(d,e), reflect instrument differences, deviations from agreed conditions, and sample degradation from measurement stresses as well as environment exposure. Despite these factors, results remain consistent across both homogeneity metrics, validating the protocol and laying the groundwork for future standardization.

This interlaboratory study represents a first step towards next-generation metrology for 2D semiconductors. By establishing reproducible protocols and identifying sources of variability in point-scanning PL mapping, we have created a benchmark for future high-throughput approaches. Hyperspectral imaging, combined with advanced statistical methods and data-driven analytics, will enable wafer-scale characterization sensitive to spatial and spectral defects and inhomogeneities. Insights from this study will inform the development of standardized protocols and data models, ensuring that wafer-scale metrology can deliver actionable metrics for process control and device integration, addressing critical metrology challenges essential for scaling 2D materials into volume manufacturing.

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KEYWORDS

2D materials, hyperspectral imaging, international standards, photoluminescence spectroscopy

Scanning X-ray Diffraction Microscopy for Strain Mapping and Defect Characterization in Semiconductor Microdevices

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INTRODUCTION

As semiconductor devices continue to scale toward highly integrated 3D architectures, controlling strain, crystalline quality, and defect distributions becomes increasingly critical for achieving high performance and reliability. Lattice strain plays a central role in determining electronic band structure, charge-carrier mobility, optical transition energies, and the reliability of nanoscale devices. These effects become even more critical in next-generation architectures such as single-electron transistors, semiconductor spin qubits, suspended micro-resonators, and CMOS-compatible light emitters. Conventional metrology methods often lack the spatial resolution, penetration depth, or sensitivity needed to characterize nanoscale distortions and defect structures within buried layers or encapsulated device regions. Techniques such as Transmission Electron Microscopy (TEM), Raman spectroscopy, or Scanning Probe Microscopy (SPM) derived mechanical mapping provide only partial, surface-limited, or model-dependent information, and may require destructive sample preparation. Scanning X-ray Diffraction Microscopy (SXDM) has emerged as a powerful synchrotron-based tool capable of providing high-resolution, non-destructive structural information from complex semiconductor architectures, enabling industry-focused optimization of advanced microelectronic components.

This work demonstrates the application of SXDM, performed at beamline ID01/ESRF, for strain mapping, defect analysis, and buried-layer characterization in a range of semiconductor materials and microdevices. With its ability to probe local lattice distortions with a spatial resolution down to ~30 nm, SXDM provides a quantitative platform for understanding process-induced strain fields, identifying defect formation pathways, and evaluating structural integrity in real device geometries.

SCANNING X-RAY DIFFRACTION MICROSCOPY (SXDM)

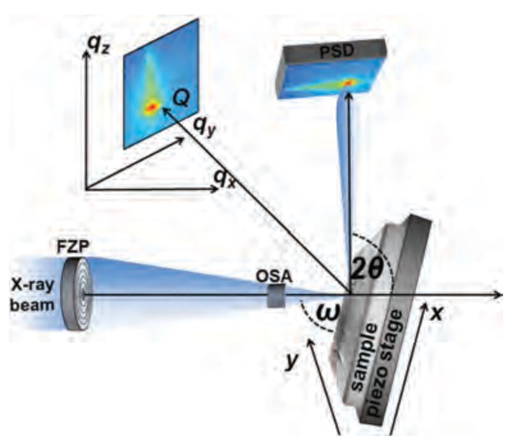

FIGURE 1 Schematic of SXDM setup, reproduced with permission from [1].

SXDM employs a tightly focused X-ray beam, typically below 100 nm in diameter, across which the sample is continuously raster-scanned while diffraction from a chosen Bragg reflection is recorded with an area detector. Because only regions of the material satisfying the Bragg condition contribute to the signal, SXDM provides highly localized structural information even from thin, deeply buried layers.

To probe three-dimensional (3D) reciprocal space, the spatial raster scans are performed repeatedly while the sample is rocked through the beam incidence angle ω. From this, a three-dimensional reciprocal-space map is reconstructed for every scanned (x, y) position, yielding in total a five-dimensional (5D) dataset linking real-space location to reciprocal-space structure at each point.

The position and shape of the Bragg peak in each 3D map reflect the local elastic and crystallographic state of the material. Automatized peak fitting provides the the scattering vector Q, which is directly related to the lattice spacing. Even sub-0.01% variations in the lattice parameters can be detected, enabling quantitative strain measurement with excellent sensitivity. At the same time, deviations in the orientation of Q reveal local lattice tilts and curvature, critical indicators of process-induced stress, interface quality, and the presence of defects or relaxation pathways. Moreover, the linear combination of the maps of the scattering vectors obtained in this way for several asymmetric Bragg reflections enables to locally calculate all six lattice parameters of the deformed unit cell, from which the complete strain tensor $\underline{\boldsymbol{\varepsilon}}$ is determined.

EXPERIMENTAL DEMONSTRATIONS

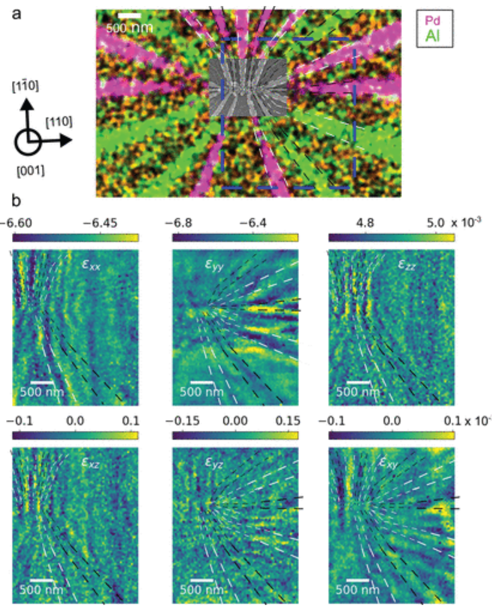

FIGURE 2 (a) EDX map overlayed with the SEM image of the qubit device. (b) Maps of all six strain tensor components after application of a Fourier high-pass filter. The dashed black and white lines outline the positions of the electrodes. Reproduced with permission from [1].

Spin Qubit Nanostructures

To evaluate how nanoscopic strain modulations affect the performance and uniformity of semiconductor spin qubits, the SXDM was applied to the very first set of two hole-spin qubits ever realized in a $Ge/Si_{0.2}Ge_{0.8}$ Quantum Well (QW). Using diffraction maps from three {335} Bragg reflections and a lateral resolution of 40 nm, SXDM enabled full reconstruction of all Bravais lattice parameters within the 16 nm-thin Ge QW, providing spatially resolved maps of the entire strain tensor. The measurements reveal two distinct classes of strain fluctuations around the qubits: short-range variations of ~100 nm extent, and long-range distortions extending over several micrometers. The short-range component aligns closely with the stress imposed onto the epitaxial layers by the lithographic metal gate electrodes controlling the device. In contrast, the larger-scale strain field, on the order of 10^{-3}, is linked to the misfit dislocation network within the plastically relaxed SiGe virtual substrate beneath the quantum well. These combined effects lead to spatial variations in the heavy-hole and light-hole band-edge energies of > 1 meV. For the current device, the measured fluctuations do not impair basic qubit functionality, but they highlight potential scaling challenges for extended qubit arrays that rely on uniform energy landscapes and shared gate architectures. Overall, this case study demonstrates how SXDM provides a powerful, non-destructive diagnostic for quantifying “strain noise” in quantum devices.

3D Strain and Composition Mapping in a GeSn/Ge Microdisk

To illustrate the power of SXDM for 3D semiconductor device analysis, a GeSn/Ge microdisk was investigated specifically designed to explore strain-engineering strategies for group-IV optoelectronics. Using the complete 5D diffraction data, it was possible to partition the sample in both real and reciprocal space and reconstruct the complete strain and rotation tensor fields of the 20 µm disk. This gave unprecedented insight into the interplay between elastic deformation, plastic relaxation, geometric constraints, and local alloy composition. By separating the reciprocal-space signals of individual layers, a tomographic view of how these defect-induced strain fields propagate across the depth of the sublayers of the microdisk was obtained. Because the microdisk contains both a free-standing rim and a center region pinned to a Ge pillar, the structure provides a unique testbed for assessing hydrostatic stress assumptions commonly used to infer alloy stoichiometry from diffraction data. These measurements reveal that the through-film average of the σ_{zz} stress component can be significant near dislocations and pattern edges, meaning that its contribution cannot be neglected in compositional analysis. Overall, this case study demonstrates how SXDM delivers comprehensive and model-free 3D strain and composition information in complex patterned heterostructures, enabling improved micromechanical understanding of next-generation GeSn-based photonic and electronic devices.

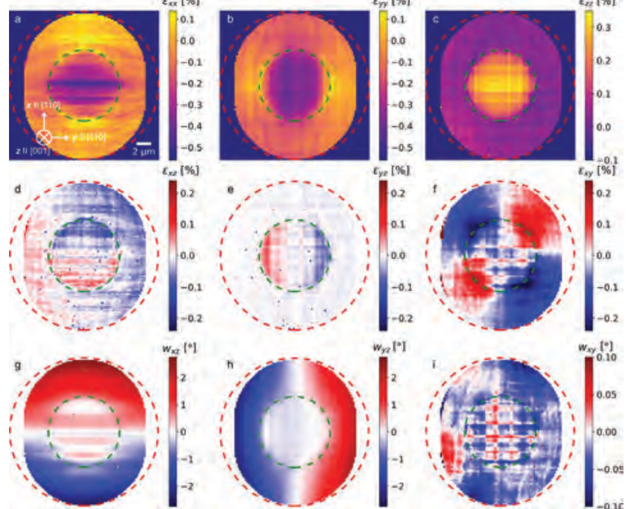

FIGURE 3 (a) Maps of lattice strain and rotation in a $Ge_{1-x}Sn_x$ microdisk. Reproduced with permission from [2].

Strain Relaxation in InGaN Mesas for Red-Emitting Micro-LEDs

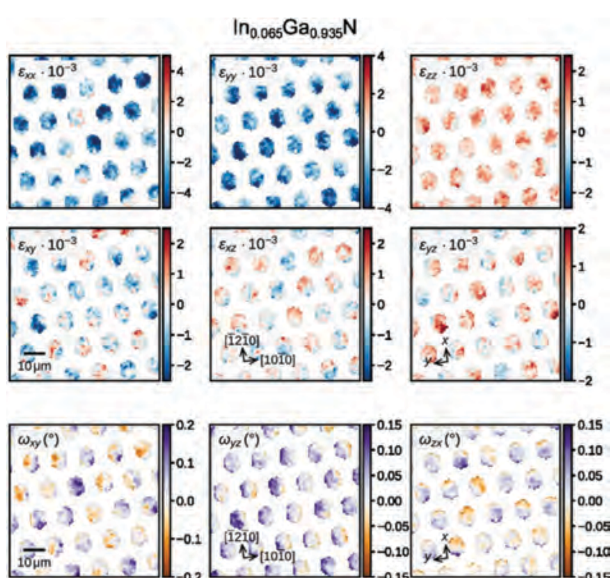

FIGURE 3 (a) Maps of lattice strain and rotation in an array of $In_{1-x}Ga_xN$ mesas. Reproduced with permission from [3].

Achieving efficient red-light emission in InGaN micro-Light Emitting Devices (LEDs) remains a central challenge for advanced AR/VR display technologies, primarily because the high indium concentrations required for red light cannot be incorporated into layers pseudomorphically strained to GaN. To address this issue, an engineering strategy based on patterning the InGaN heterostructure into isolated 10 µm mesas, with the goal of enabling partial strain relaxation in the $In_xGa_{1-x}N$ pseudosubstrate. The structure, composed of an $In_xGa_{1-x}N$ layer and an ($In_xGa_{1-x}N$/n-GaN) superlattice grown on GaN-on-sapphire, acts as a buffer intended to provide a larger effective in-plane lattice constant. Using SXDM with approximately 60 nm spatial resolution, lattice strain and tilt were mapped throughout individual and ensembles of patterned mesas. The measurements show that patterning induces substantial strain relaxation not only near the mesa edges, where elastic relaxation is expected, but uniformly throughout the entire mesa volume. This surprisingly homogeneous relaxation suggests the activation of a plastic relaxation mechanism, potentially involving dislocation glide, that becomes accessible only after micro-patterning. The resulting partially relaxed pseudosubstrate offers a significantly reduced mismatch with high-In-content quantum wells and does so without relying on porous buffer layers. These findings confirm that mesa patterning is a promising route toward enabling native RGB emission in next-generation micro-display technologies.

INDUSTRIAL RELEVANCE

The ongoing evolution of semiconductor manufacturing toward three-dimensional integration, aggressive strain engineering, and heterogeneous device architectures brings a growing need for metrology tools capable of probing structural properties deep within complex material stacks. As device geometries shrink and functional layers become increasingly buried or encapsulated, traditional surface-sensitive or destructive techniques fail to provide the complete and quantitative strain information required for reliable process optimization. In this context, SXDM offers a uniquely powerful solution by combining high strain sensitivity with non-destructive volumetric probing and full tensor reconstruction, e.g. for advanced CMOS technologies, optoelectronics, quantum devices, and power electronics.

This type of experimental feedback is crucial for improving fabrication protocols, validating design strategies, and predicting long-term device behavior, especially in architectures where strain plays a central role in determining band structure and charge-transport characteristics. Furthermore, the SXDM technique integrates naturally with modern simulation workflows. Experimentally measured strain fields serve as accurate inputs for FEM mechanical models and band-structure calculations, bridging the longstanding gap between real devices and theoretical predictions. This experimentally grounded modeling pipeline enhances the predictive power of simulations used for process development, reliability assessments, and design optimization across multiple semiconductor platforms.

ACKNOWLEDGEMENTS

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KEYWORDS

Strain engineering, X-ray Microscopy, Epitaxial Layers, Quantum Technology, Optoelectronics

Moiré Atomic Force Sensors for Robust Nanoscale Sensing

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INTRODUCTION

The accuracy of length measurement affects the precision of length measuring devices and also nanofabrication technologies [1, 2]. Due to its high accuracy and non-contact-operation, optical methods are widely used. The resolution of optical encoders is already in the order of nanometer and beyond. Due to the limitation by diffraction a further progress in this field is very difficult and new methods for high precision encoders are necessary. Using an atom force microscope (AFM) as encoder for improvement of measurement resolution existed already [3, 4] but show several disadvantages. Therefore, a new method based on using nanostructures as a material scale, which inspired from the optical moiré effect and so-called moiré atomic force sensors, would be proposed in this presentation.

METHOD

This approach utilizes a fabricated Moiré pattern on the AFM cantilever tip, which scans a grating sample of same pitch. The system comprises a second cantilever of the same type, arranged at a phase shift of 90° relative to the first, for up-down counting (Figure 1). The fundamental principle is: the detected deflection of cantilever, caused by interaction between cantilever tip and sample, is at minimum when the ridges of one grating align with the grooves of the other. Conversely, the signal reaches its maximum when the ridges of both gratings are in alignment. During scanning process, the signal exhibits a sinusoidal variation with a specific period. To enhance signal contrast, a large effective contact area on the tip is required. We address this by using spherical-tipped cantilevers with diameters up to 85 µm, which also mitigates the tilting issues often associated with plateau tips.

The advantages of this method are: firstly, the measurement resolution for side wall height could be improved significantly with 16-bit AD conversion. Secondly, tip-wear as a major limitation of traditional AFM would not be a problem for long-time scanning in this case.

MEASUREMENT AND RESULTS

At Institute for Process Measurement and Sensor Technology at the Technische Universität Ilmenau an atomic force microscope from company NanoAnalytik GmbH is available, which equipped with a precision bottom scanner within range of 50 µm×50 µm×20 µm along the xyz-axes, respectively and self-actuating and self-sensing active microcantilever probs. Since there are no commercially manufactured active cantilever probes with spherical tips, we have custom-fabricated them by mounting microspheres onto the cantilevers. The chosen SiO_2 spheres, sourced from micro particles GmbH, have diameters of 20 µm, 50 µm, and 85 µm and were attached using UV-curing adhesive NOA61 from Thorlabs.

Force-displacement measurements were firstly conducted using these custom cantilevers to confirm the expected increase in interaction force with larger sphere diameters. The result in Figure 2 and Table 1 shows that compared to a commercial reference tip with 130 nm diameter, the pull-off force measured by force spectrometer increased by about 250 times with 20 µm-sphere-tip, by about 23 times with 50 µm-sphere-tip and by around 500 times with 85

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µm-sphere-tip. The suboptimal performance of the 50 µm tip was attributed to surface contamination with small particles, detected via scanning electron microscopy (SEM). Nevertheless, the results demonstrate the potential of larger spheres for maximizing interaction forces.

As the next step, a 300 nm pitch grating was fabricated on these spherical tips of cantilevers by focused ion beam (FIB) with operation parameters of 240 pA current and 5 kV voltage for 1690 s. The key part, scanning with 300 nm-pitch Moiré cantilever of a prepared 300 nm-pitch sample should be operated and detected signal would be analysed more in detail.

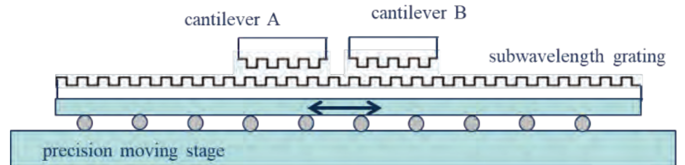

FIGURE 1. Concept of force changing during scan process with Moiré atomic force sensors.

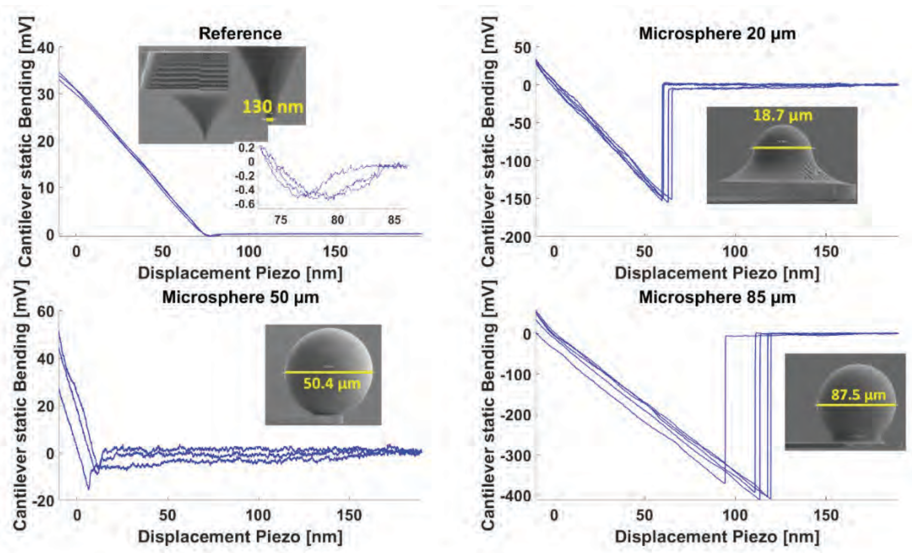

FIGURE 2. Force displacement measurements with different-sized cantilever tips. Test sample is cleaned silicon wafer.

TABLE 1. Result of Force Displacement Measurement with different cantilevers

Parameter	Reference Tip	20 µm Sphere-Tip	50 µm Sphere-Tip	85 µm Sphere-Tip
Pull-Off Voltage	0.367 mV	0.151 V	0.011 V	0.397 V
Measurement Sensibility	1.2 mV/nm	2.7 mV/nm	2.6 mV/nm	3.6 mV/nm
Pull-off Deflection	0.3 nm	55 nm	4.2 nm	110 nm
Spring Constant	20 N/m	22 N/m	25 N/m	22 N/m
Pull-Off Force	0.0045 µN	1.21 µN	0.105 µN	2.24 µN

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KEYWORDS

Force sensor, Atom force microscope, Moiré effect, Subwavelength scanning

Non-Destructive Depth Profiling By Variable Energy Parallel Angle Resolved XPS (VE-PARXPS)

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INTRODUCTION

Chemical analysis of contemporary materials often entails characterizing surface and bulk compositions. **EnviroMETROS LAB** and **FAB** tools equipped with a monochromatic, small-spot X-ray source with up to three different photon energies, provide different surface and bulk sensitivities due to the variation in the kinetic energy of the emitted photoelectrons. Moreover, the angle-resolving, wide-angle electron analyzer **AEOLOS 150 AD-CMOS**, together with the software, enables high sensitivity and high-resolution analysis with direct non-destructive depth profiling.

Variable Energy X-ray photoelectron spectroscopy (VE–XPS) employs tunable X-ray sources, such as synchrotrons or laboratory-based monochromators, to adjust the photon energy. This adjustment enables depth profiling and enhanced sensitivity to different core levels. Tuning the photon energy allows to control the kinetic energy of emitted photoelectrons and effectively change the inelastic mean free path (IMFP), see Fig. 1. This capability allows for analysis of surface, subsurface, and bulk regions.

Parallel Angle-Resolved XPS (PARXPS) allows to collect photoelectrons at various emission angles simultaneously using a wide-angle analyzer. This method facilitates the concurrent acquisition of spectra from multiple angles in a single shot, thereby enhancing the efficacy and precision of probing depth and electronic structure. PARXPS allows to create concentration depth profiles from data that was taken for different photoelectron emission angles, see Fig. 2. A parallel spectra collection of individual angle channels is possible with the **AEOLOS 150 AD-CMOS** analyzer, developed especially for performing high-transmission PARXPS measurements.

VE-XPS allows for the adjustment of probing and information depth, while PARXPS provides angular-resolved data, enabling non-destructive depth profiling with enhanced accuracy. By varying the energy and emission angle, more detailed information can be extracted, which is crucial for materials such as multilayer stacks and semiconductors. The combination of tunable energy with angular resolution enables the differentiation between surface, interface, and bulk states, thereby facilitating the acquisition of comprehensive structural information. The capacity to adjust depth sensitivity minimizes the occurrence of misinterpretation arising from charging effects or contributions from deeper layers, ensuring the reliability and precision of the measurement process. The combination of VE-XPS and PARXPS allows for gaining a much richer dataset, enabling a more precise and comprehensive understanding of material surfaces and interfaces.

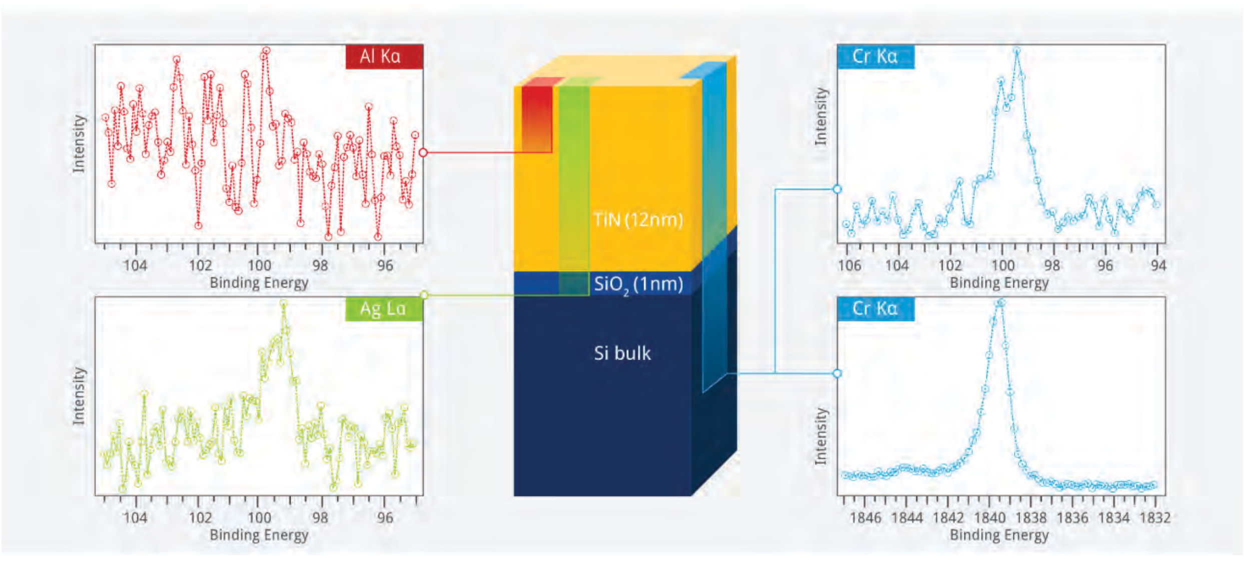

FIGURE 1. High-resolution Si 2p (and Si 1s) core-level spectra of a 12 nm thick TiN sample measured with Al Kα, Ag Lα, and Cr Kα excitation.

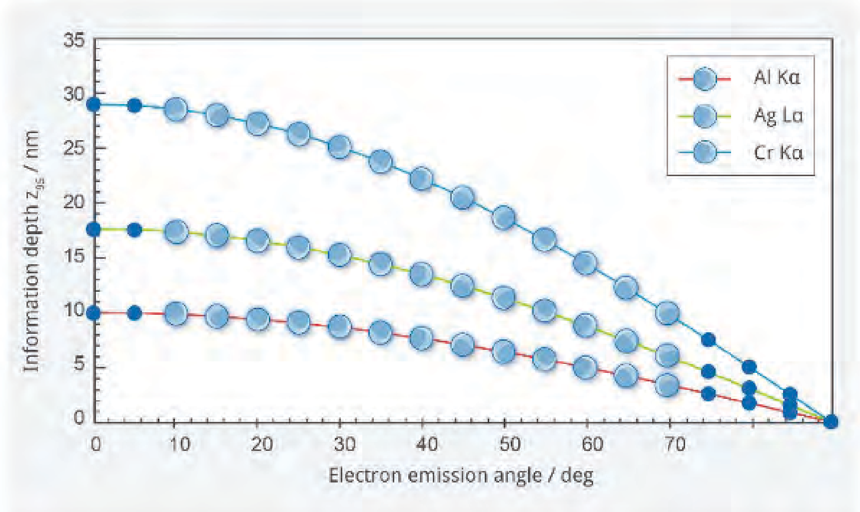

FIGURE 2. The diagram illustrates the XPS information depth z_{95} for silicon photoelectrons versus the photoelectron emission angle ranging from 0° to 90° when using Al Kα, Ag Lα, or Cr Kα excitation.

KEYWORDS

PARXPS, non-destructive depth profiling, multilayer stacks, thin films, HAXPES, metrology, semiconductor

Quantification of Carbon Concentration in GAA Inner Spacer Gapfill by TEM/EELS

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INTRODUCTION

As semiconductor technology advances towards increasingly smaller and more intricate architectures, such as Gate-All-Around (GAA) transistors, quantifying the carbon composition within the tiny (~few nm) inner spacer gapfill materials has become essential for process control. Carbon (C) is pivotal in enhancing the electrical isolation and etch resistance of the gapfill, yet quantifying it at the sub-nanometer scale presents significant challenges due to the complexities of isolating the gapfill from the sidewalls and eliminating carbon contamination. In this work, we employed Electron Energy Loss Spectroscopy (EELS) to achieve precise carbon quantification in the gapfill regions. By optimizing Focused Ion Beam (FIB) specimen preparation and minimizing carbon contamination, we demonstrate a reliable method for quantifying carbon concentration for gapfill films surrounding GAA structures at the sub-nanometer scale.

DESCRIPTION OF APPROACH

To quantify carbon concentration in nanoscale semiconductor materials, two main challenges must be addressed: removing silicon nitride (SiN) sidewalls and eliminating carbon contamination. To achieve complete removal of SiN sidewalls, the target structure was modified from smaller Bar1 structures (20 nm CD) to larger Bar2 variants (30 nm CD), while still meeting customer specifications. This adjustment enabled thorough removal of SiN sidewalls by milling the lamella below 30 nm thick, preventing the nitrogen signal from the sidewall from overlapping with that of the gapfill. Additionally, hafnium oxide (HfO_2) was coated prior to FIB specimen preparation to separate the epoxy protective coating from the inner spacer. A 2 kV low-energy rock-milling method was employed at the final stage of FIB to minimize ion beam damage and carbon contamination from the protective epoxy coating to the specimen. To further eliminate carbon contamination on the specimens, a 5-minute electron beam shower in the TEM was used to remove surface carbon contaminants. During a beam shower, a high-current electron beam is directed at the specimen to remove surface carbon, ensuring that the measured carbon concentration originates solely from the specimen and not from environmental hydrocarbons. EELS measurements were subsequently conducted under 200 keV TEM in Scanning Transmission Electron Microscopy (STEM) mode with 0.1 nA beam current for 5 minutes, achieving a good signal-to-noise ratio of the EELS spectrum without causing beam damage to the specimen. The resulting carbon concentration from the EELS spectrum on specimens with high-carbon gapfill film was cross-verified with inline Energy Dispersive X-ray Spectroscopy (EDS) results for validation.

EVALUATION OF RESULTS

Figure 1 presents three EELS characterization attempts of the gapfill film around the GAA structure, highlighting two failures followed by one success. In Figure 1A, EELS maps of the GAA structure with gapfill at the Bar1 structure reveal distinct nitrogen signals that do not conform to the shape of the gapfill surrounding the Si/SiGe channels, suggesting nitrogen originates from the frontside or backside SiN spacers rather than the gapfill. The Bar1 structure is too thin (20 nm CD), requiring the specimen to be milled below 20 nm thick to fully remove sidewall residues, but milling this thin causes bending, hindering TEM imaging. Figure 1B shows EELS maps of the GAA gapfill at the Bar2 (30 nm CD) structure, where switching from Bar1 to Bar2 effectively removes the SiN residue. However, carbon residues from the TEM column were deposited on the specimen, impeding carbon

quantification. Figure 1C demonstrates successful EELS quantification at the Bar2 structure after sufficient beam shower, showing removal of SiN residues and elimination of carbon contamination, with the gapfill clearly visible surrounding the Si/SiGe channels. The quantifying precision of carbon concentration was improved from 10% to 2%.

Figure 2A presents EELS maps of the GAA structure with a high-carbon gapfill specimen, showing the sample is free of nitrogen residues and carbon contamination, with a spatial resolution of 5 Å. Figure 2B illustrates the line scan profile of the top trench, following the direction of the white arrow, revealing approximately 40% carbon concentration in the gapfill film, which is 4-5 nm thick and positioned outside the native oxide layer of the SiGe channels and inside the HfO2 coating layer. Figure 2C depicts carbon concentration variations across three different trenches: top, middle, and bottom. The carbon concentration increases from 40% to 50%, while the thickness increases from 4 nm to 6 nm from the top trench to the bottom trench. The carbon concentration aligns well with inline EDS results, validating the EELS carbon characterization method and serving as a baseline for further EELS studies. Figure 3A presents EELS maps of the GAA structure with a moderate carbon gapfill specimen, showing no nitrogen residues or carbon contamination, with a spatial resolution of 1 nm. Figure 3B illustrates the line scan profile at the top trench (white arrow), revealing approximately 30% carbon concentration in the gapfill film of 4 nm thickness. Figure 3C shows carbon concentration increasing from 20% to 30%, with thickness rising from 4 nm to 5 nm from the top to the bottom trench.

In summary, we developed a reliable EELS method for quantifying carbon concentration in GAA Inner Spacer Gapfill at sub-nanometer scale, offering potential for improved quality control and device performance.

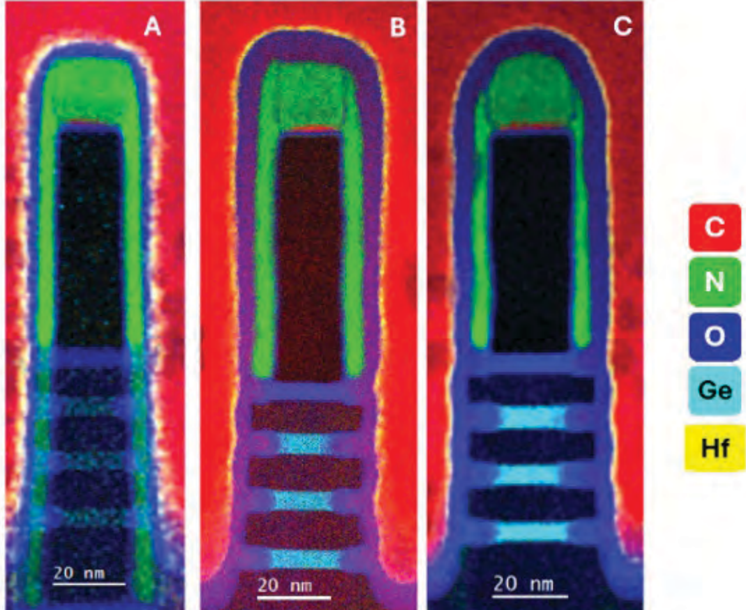

FIGURE 1. Three EELS characterization attempts of the gapfill film surrounding the GAA structure, with two failures (A, B) and one success (C). Silicon maps are omitted for clarity. A) Gapfill film at the Bar1 structure showing nitrogen residue signals. B) Gapfill film at the Bar2 structure showing no nitrogen residue signals but carbon contamination. C) Gapfill film at the Bar2 structure successfully free of nitrogen residues and carbon contamination.

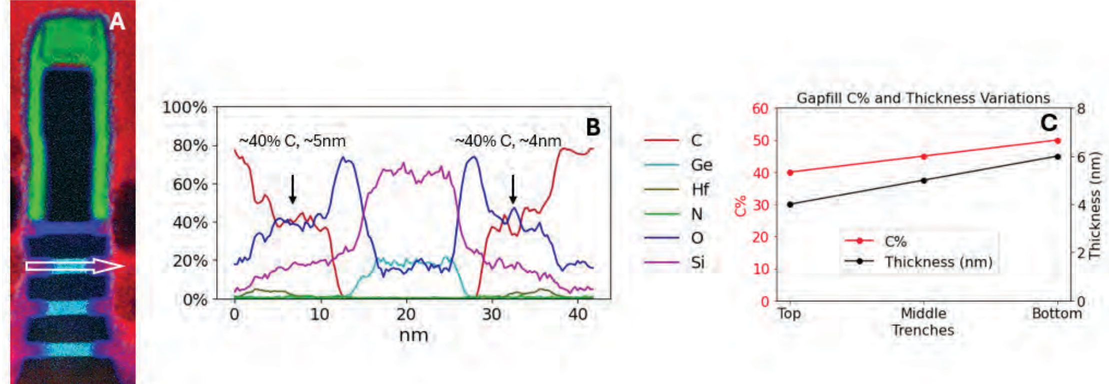

FIGURE 2. A) EELS maps of the GAA structure with a high-carbon concentration gapfill film with spatial resolution of 5 Å. The silicon map is omitted for clarity. B) Line scan profile at the top trench, following the direction of the white arrow in Figure 2A. C) Carbon concentration and thickness variations across three different trenches (top, middle, bottom).

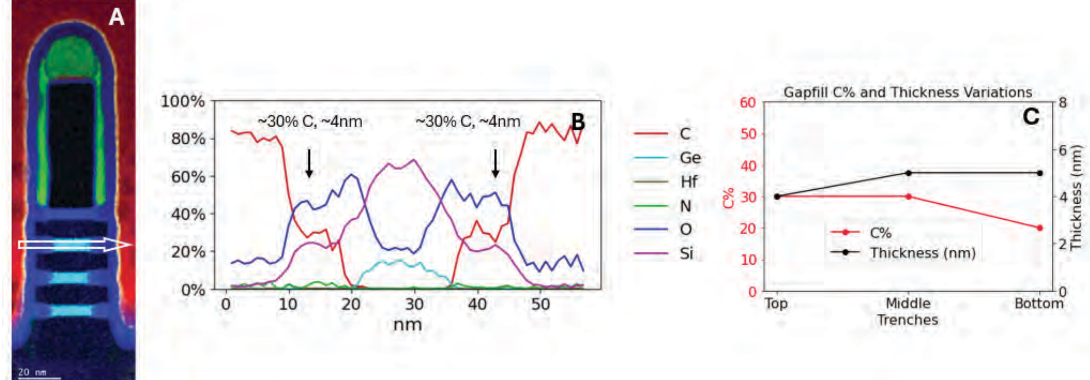

FIGURE 3. A) EELS maps of the GAA structure with a moderate-carbon concentration gapfill film with spatial resolution of 1 nm. The silicon map is omitted for clarity. B) Line scan profile at the top trench, following the direction of the white arrow in Figure 3A. C) Carbon concentration and thickness variations across three different trenches (top, middle, bottom).

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KEYWORDS

Electron Energy Loss Spectroscopy (EELS), Gate-All-Around (GAA) transistors, inner-spacer gapfill

Advanced X-ray Techniques for Multi-Scale Semiconductor Characterization and Device alternation

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Introduction

With the continued miniaturization of transistor features and the adoption of stacked 3D architectures, nondestructive metrology must simultaneously achieve high spatial resolution and large-area coverage. X-ray techniques, due to their ability to probe through opaque materials and image buried interfaces, have become indispensable in advanced device analysis and failure localization. [1] However, conventional microtomography (micro-CT) systems often require trade-offs between field of view, resolution, and throughput, limiting their scalability for large packages or wafer-level analysis. [2]

Computed Laminography (CL) has emerged as a complementary technique, optimized for planar geometries such as wafers, advanced packages, and interposers. Recent advancements in X-ray source design, detector technology, and reconstruction algorithms have pushed these methods toward both higher resolution and faster acquisition speeds—bridging the gap between R&D characterization and production-scale inspection. [2]

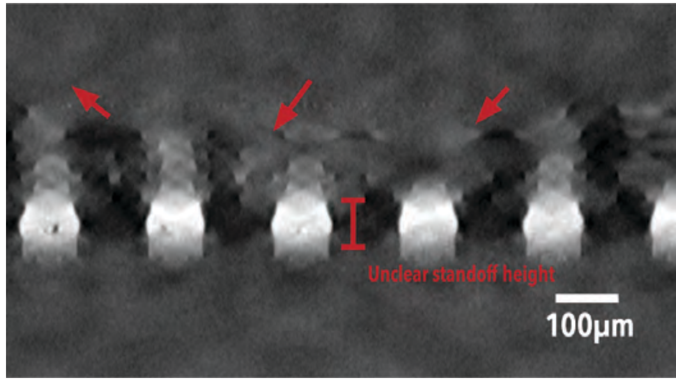
Dual-Mode 3D X-ray Imaging

We present a dual-mode 3D X-ray platform that integrates computed tomography (CT) and Precision Angle Laminography (PAL) into a single instrument. This hybrid approach provides continuously tunable geometries, allowing users to select the optimal imaging configuration for a given sample, from normal-incidence CT for small dies to high-angle laminography for large, planar assemblies.

By combining submicron-resolution imaging (<0.4 µm) with flexible angular control, this architecture reduces laminographic artifacts and enhances visualization of vertical features such as through-silicon vias (TSVs), hybrid bonds, and backside interconnects. The result is a system capable of non-destructively revealing fine-scale defects, such as voids, delamination, non-wets, or misalignment, while maintaining high throughput suitable for lab or inline metrology workflows.

Experimental validation on commercial 3D-stacked CPU devices demonstrates quantitative 3D analysis of thermal interface material (TIM) voiding, hybrid Cu–Cu bond quality, and solder bump uniformity, achieved without destructive cross-sectioning. The hybrid mode also enables rapid switching between wide-area survey scans and high-resolution region-of-interest imaging, improving overall FA and yield-learning efficiency.

By enabling adjustable slant angles and leveraging precision motion control, such systems reduce common laminographic artifacts and improve the clarity of vertical structures (such as through-silicon vias / TSVs and hybrid bonds) that are critical to modern packaging. This capability is particularly beneficial for identifying subtle defects such as delamination, bridging, or stand-off height variation (as shown in Fig. 1), which may otherwise be obscured in conventional 2D or high-angle 3D scans. For FA engineers, these advancements translate into faster root-cause analysis, greater confidence in defect localization, and the ability to evaluate more samples in less time.



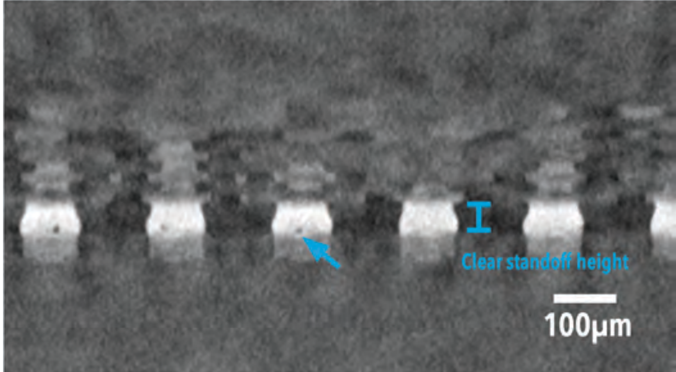


FIGURE 1. Comparison of conventional laminography (top) to Precision Angle Laminography (PAL) (bottom). The PAL approach provides much clearer cross-sectional image data as compared to conventional laminography, leading to dramatically-increased accuracy of automated, quantitative reports.

Emerging Analytical Extension

Beyond structural imaging, X-ray fluorescence (XRF) and spectroscopic tomography are now being integrated to provide elemental and chemical contrast within the same 3D datasets. These multimodal approaches yield both structural and compositional information, critical for correlating process variations with electrical performance in advanced nodes.

In addition, the paper introduces a conceptual framework for X-ray Assisted Device Alteration (XADA). Analogous to traditional Laser Assisted Device Alteration (LADA), XADA exploits the penetrative and selective absorption properties of focused X-rays to locally induce photoelectric or thermal effects in 3D device stacks. Unlike LADA, which is limited to frontside optical access, XADA provides backside or buried-layer selectivity, enabling potential new approaches to fault isolation, power delivery mapping, and subsurface device tuning in future 3D architectures.

Conclusion

Advanced X-ray methods are redefining nondestructive metrology across 2D, 2.5D, and 3D device generations. The combination of high-resolution CT and laminography in a single hybrid system provides unmatched flexibility for inspecting complex assemblies, from die-level defects to wafer-scale integration, without compromising speed or resolution.

Emerging analytical extensions such as spectroscopic XRF tomography and XADA promise to expand X-ray capabilities beyond imaging, offering new routes for electrical, thermal, and material characterization deep within

multilayer structures. Together, these advances position X-ray-based platforms as cornerstone technologies for next-generation failure analysis, process control, and 3D device metrology.

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Keywords

X-ray microscopy, computed laminography, computed tomography, failure analysis, hybrid bonding, 3D integration, X-ray fluorescence (XRF), X-ray Assisted Device Alteration (XADA), backside power delivery, nondestructive metrology

High resolution SIMS Nanoanalytics for Semiconductor Process Control

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INTRODUCTION

Advanced semiconductor manufacturing relies on precise nanoscale imaging and elemental analysis to ensure process stability, yield, and device reliability. Secondary Ion Mass Spectrometry (SIMS) provides high chemical sensitivity and isotopic resolution but traditionally faces challenges in lateral resolution and integration with in-line process control. This work introduces an integrated ion microscope platform that combines a Liquid Metal Alloy Ion Source (LMAIS), magnetic sector SIMS, and a laser-interferometer stage for high-resolution, quantitative nanoanalytics.

SYSTEM OVERVIEW

The instrument features a vertical focused ion beam (FIB) column equipped with a LMAIS providing multiple ion species, selectable via a Wien filter. The system integrates a magnetic sector SIMS for high-sensitivity elemental detection and a laser-interferometer stage for nanometer-accurate navigation. Heavy ions (e.g., Bi^+, Bi_3^+) are used for sputtering and delayering, while light ions (e.g., Li^+) enable sub-2 nm imaging resolution. The setup supports automated wafer navigation using CAD or KLARF data, making it suitable for process control applications.

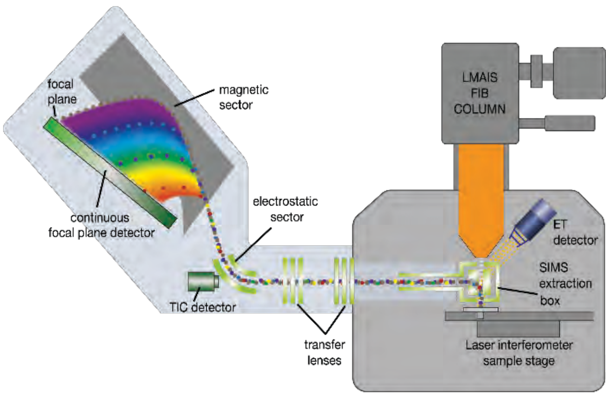

Figure 1. Schematic setup of the ion microscope with LMAIS, interferometer stage, and magnetic sector SIMS unit.

SIMS NANOANALYTICS AND RESULTS

The magnetic sector SIMS enables full-mass-spectrum acquisition per pixel, providing detailed 2D and 3D chemical maps of advanced semiconductor devices. High secondary ion yields achieved with Bi^+ and Bi_3^+ beams enable sensitive dopant profiling and contamination analysis, while Li^+ imaging delivers sub-2 nm resolution for precise structural correlation. Alternating milling and imaging cycles produce high-fidelity 3D reconstructions of buried features and interfaces.

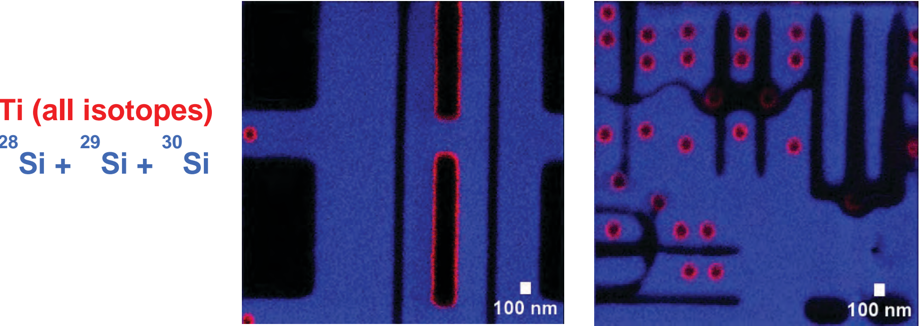

Figure 2. High-resolution SIMS maps showing elemental variations in a 65 nm CMOS device (35 keV Bi^+, 5 pA).

CONCLUSIONS

The presented ion microscope platform combines multi-species LMAIS, magnetic sector SIMS, and interferometer-based positioning to provide high-resolution chemical mapping and imaging for semiconductor process control. The system supports automated workflows, defect review, and compositional analysis at nanometer resolution, addressing the metrology demands of advanced semiconductor nodes.

KEYWORDS

SIMS, ion microscopy, semiconductor metrology, process control, nanoanalytics, LMAIS

Advances in Nanoscale Dopant Metrology of Silicon-Based Materials using Atom Probe Tomography

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INTRODUCTION

The characterization of dopants within confined volumes is one of the most challenging, yet pressing needs in semiconductor metrology[1]. Indeed, the concentration and spatial distribution of these impurities modulate the electrical and optical properties of a device, making this information critical whether for advancing operational efficiency, understanding material-property relationships, or performing failure analyses.

Atom probe tomography (APT) is a materials characterization technique that has the potential to meet the industry need for reliable and accurate dopant metrology. This technique provides three-dimensional, chemical mapping with sub-nanometer spatial resolution and atomic parts per million sensitivity[2]. However, among other reasons, the routine application of APT is still hindered by compositional biases[3] and field evaporation artifacts[4], which may lead to preferential detection losses for certain elemental species and distorted spatial distributions. For the purpose of enabling routine application of APT for dopant metrology in p- and n-type silicon (Si)-based devices, this work presents a holistic investigation into measurement artifacts and mitigation strategies through an assessment of key experimental parameters. In addition, a cross-instrument investigation provides insight into instrument-related artifacts so as to ensure wide applicability. Lastly, a novel sample preparation technique is demonstrated, whereby focused ion beam (FIB) redeposition is exploited for in situ, site-specific coatings, enabling near-surface dopant analysis.

DOPANT ARTIFACT MECHANISMS IN APT

p-Type Si Dopant Metrology

Boron (B) is the most widely used p-type dopant in Si-based semiconductor devices, yet its quantification by APT has long been hindered by measurement errors/inaccuracies[5,6]. These challenges stem primarily from the complex field evaporation behavior of B, which has a higher evaporation field threshold than Si. As a result, B atoms tend to retain on the specimen surface during analysis and evaporate non-stoichiometrically, producing depth profiles that are artificially elongated. This artifact is often accompanied by surface migration of retained B atoms, leading to degraded lateral resolution, and apparent signal contributions outside the true doped region. Further complications arise from the tendency of B to co-evaporate in burst events, where multiple ions arrive nearly simultaneously at the detector. The limited spatial and temporal resolving power of conventional three-anode, delay-line detectors prevents accurate identification of these closely spaced ions, resulting in undercounting of B. The extent of these artifacts is strongly influenced by the applied experimental conditions, particularly the specimen's apex electric field during analysis. To address these artifacts, this study presents a systematic evaluation of detection efficiency and dopant profile fidelity across a range of electric field conditions using the National Institute of Standard and Technology (NIST) Standard Reference Material (SRM) 2137, a well-characterized B implant in Si with a certified dopant dose and defined concentration profile[7]. As shown in Figure 1(B), increasing the apex electric field substantially improves quantification accuracy. Enhanced field conditions also yield improved profile shape integrity and lateral resolution (Figure 1(A)). Conversely, analyses conducted at lower electric fields reveal extensive surface migration, as evidenced by desorption maps showing highly inhomogeneous B emission localized near the detector center. These findings establish clear correlations between experimental field conditions and B quantification fidelity in APT. In the broader context of semiconductor metrology, they offer practical guidance toward establishing best practices for achieving accurate and reproducible nanoscale dopant measurements in Si-based materials.

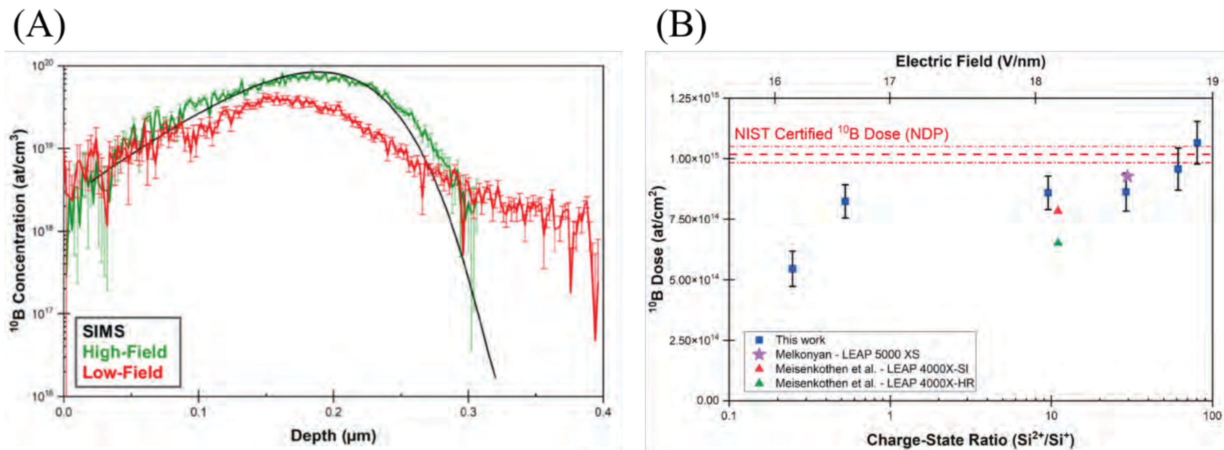

FIGURE 1. (A) B Concentration Profiles at Low and High Field Strengths. (B) Measured B Dose as a Function of Field Strength.

n-Type Si Dopant Metrology

While B exemplifies the complexities of p-type dopant analysis in silicon, n-type dopants such as phosphorus (P) and arsenic (As) present their own distinct but complementary challenges. In APT, both species frequently field evaporate as complex, high-order molecular ions (e.g., P_2^+, As_2^+, and larger clusters), leading to significant mass spectral overlaps and deconvolution ambiguities. Additional complications arise from the potential formation of neutral species and field dependent retention or surface migration, all of which contribute to dopant undercounting and spatial distortion within reconstructed volumes. To quantitatively assess these effects, the present study uses the NIST phosphorus (NIST SRM 2133) and arsenic (NIST SRM 2134) reference materials. The results demonstrate that increasing the specimen's apex electric field and reducing laser pulse energy substantially suppress the formation of complex high-order ions, thereby mitigating unresolved mass spectral overlaps. By systematically mapping these dependencies across a matrix of field and laser parameters, this work identifies operational windows that maximize quantitative accuracy for each dopant species. Together with the B analysis, these findings establish a unified understanding of field-dependent evaporation behavior across both p- and n-type dopants. They also provide practical guidance for optimizing APT acquisition parameters to achieve accurate and reproducible nanoscale dopant metrology in Si-based materials.

Cross-Instrument Correlative Investigation

Differences in instrument architecture (e.g., straight flight-path vs. reflectron-equipped designs) impact ion trajectories, detection efficiencies, and mass resolutions and, therefore, contribute to systematic compositional biases. To complement the evaluation of the NIST SRMs, we further explore dopant metrology through a cross-instrument evaluation of three low-resistivity silicon samples on three instruments representing distinct flight path and optic configurations (i.e., CAMECA LEAP 5000 XS, LEAP 5000 XR, and INVIZO 6000). Experimental parameters are varied widely to explore the parameter space and to identify instrument dependent biases that influence dopant quantification.

IN SITU REDEPOSITION COATINGS AND SPECIMEN STABILITY

Lastly, as shown in Figure 2, a novel sample preparation technique is demonstrated to complement this work. This method takes advantage of FIB redeposition for site-specific coatings in order to facilitate near-surface dopant metrology[8]. It is shown to protect the ROI from FIB damage and to moderate field threshold differences at the specimen cap interface, which markedly improves specimen stability for near surface dopant measurements while permitting site specific preparation. Advantages and limitations of the method are discussed together with metrics for routine applicability across silicon-based systems.

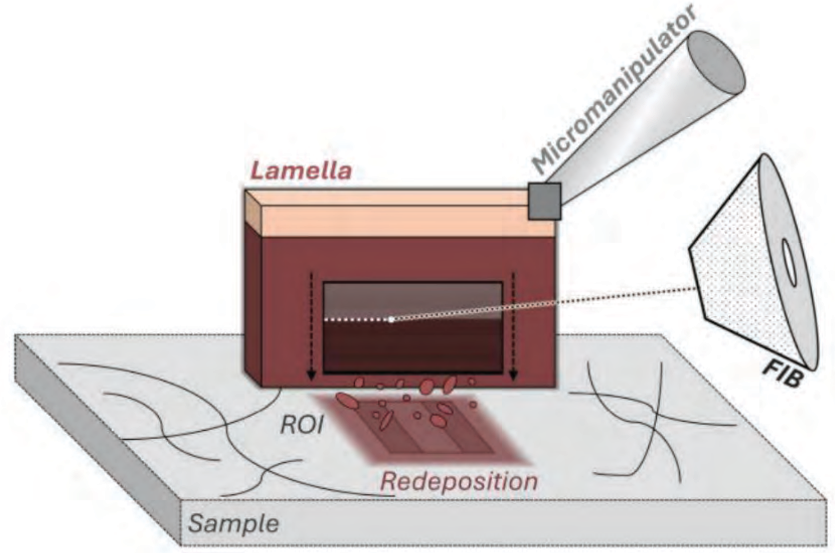

FIGURE 2. A Schematic of the Site-Specific FIB Redeposition Coating Technique.

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KEYWORDS

Dopant Metrology, Atom Probe Tomography, Secondary Ion Mass Spectrometry, Silicon

Widefield quantum diamond magnetic microscope for semiconductor failure analysis

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INTRODUCTION

The semiconductor industry faces critical challenges in fault detection and metrology as it transitions to advanced 3D integrated circuits and system-in-package designs. Traditional metrology and failure analysis (FA) methods have difficulties to reliably detect faults within complex, stacked architectures [1]. Existing methods are either destructive, too slow, or blind to defects in stacked devices. Here, we present a quantum diamond magnetic microscope (QDMM) based on nitrogen vacancies (NVs) in diamond, which allows for non-invasive, real-time inspection even of buried structures like TSVs, RDL and 3D interconnects [2,3]. Our novel design including a novel detector and patented readout algorithms allows us to break the sensitivity and speed barriers that have limited QDMMs so far. Our design will enable a 100-1000x improvement in measurement sensitivity, corresponding to up to a million times faster imaging times compared to existing systems.

LEVERAGING QUANTUM SENSING WITH NITROGEN VACANCIES

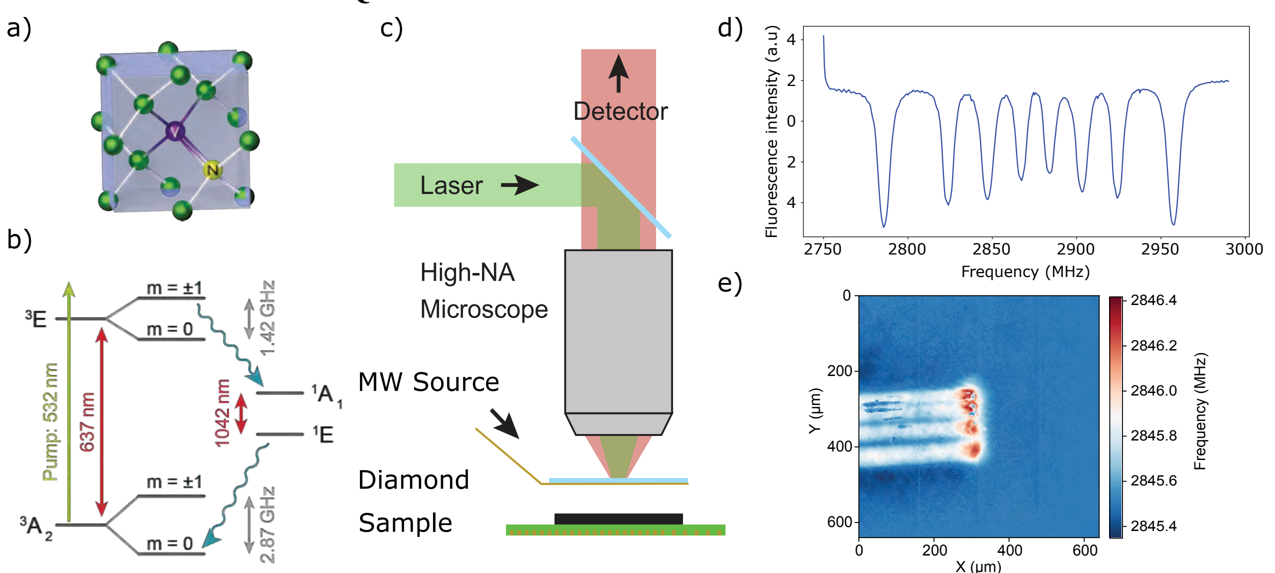

Figure 1 ***a)*** *Schematic of a nitrogen vacancy (NV) center in the diamond lattice structure.* ***b)*** *Level spectrum of the NV center, showing fluorescence in the visible spectrum or infrared, depending on the spin state.* ***c)*** *Schematic of the measurement configuration.* ***d)*** *Optically detected magnetic resonance (ODMR) curve, showing fluorescence intensity with respect to applied microwave frequency. Four different NV orientations and two spin orientations give rise to 8 peaks.* ***e)*** *Spatial display of the frequency shift of the ODMR when measuring the magnetic field of a test structure.*

We employ nitrogen–vacancy (NV) centers in diamond—atomic-scale defects where a nitrogen atom sits adjacent to a lattice vacancy (see Fig. 1a)—as magnetic field sensors for magnetic current imaging (MCI). NV centers combine long spin coherence times and nanoscale sensing volumes, offering both high magnetic sensitivity and sub-micrometer spatial resolution. Their four crystallographic orientations allow measurement of all three magnetic field vector components in a single acquisition, enabling full 3D current reconstruction essential for advanced semiconductor FA and metrology [2-4].

Under green laser excitation, the NV spin state modulates fluorescence intensity, while microwave driving reveals magnetic resonance shifts proportional to the local magnetic field through the Zeeman effect. Mapping these frequency shifts across the field of view yields a vector magnetic field image and, by inversion of the Biot–Savart law, the underlying current distribution in 2D or 3D (see Fig. 1b-e).

At DiaSense, we have established a first laboratory prototype of the Quantum Diamond Magnetic Microscope (QDMM), validating all key performance metrics. The system achieves single-pixel magnetic sensitivity of 5–10 nT/√Hz and has successfully mapped magnetic fields from test currents on semiconductor samples. Initial current reconstructions demonstrate micrometer-scale spatial resolution, confirming the viability of NV-based wide-field magnetometry for chip failure analysis. Ongoing developments focus on increasing acquisition speed and extending sensitivity across the full field of view, paving the way for real-time, non-invasive 3D current imaging in FA workflows.

FROM QUANTUM DATA TO ELECTRICAL INSIGHT

As a proof of concept, we present first magnetic measurements with our prototype performed on a test chip. The chip consists of several gold wire structures patterned on a silicon wafer, designed to characterize key performance parameters of our microscope (Fig. 2a). We map the resonance frequencies of all NV center transitions across the field of view while driving a current of ~50 mA through a meandering 10 µm wide wire structure. To extract the vector components of the magnetic field (Fig. 2b), we fit the full NV spin Hamiltonian for all four crystallographic orientations to the measured transition frequencies.

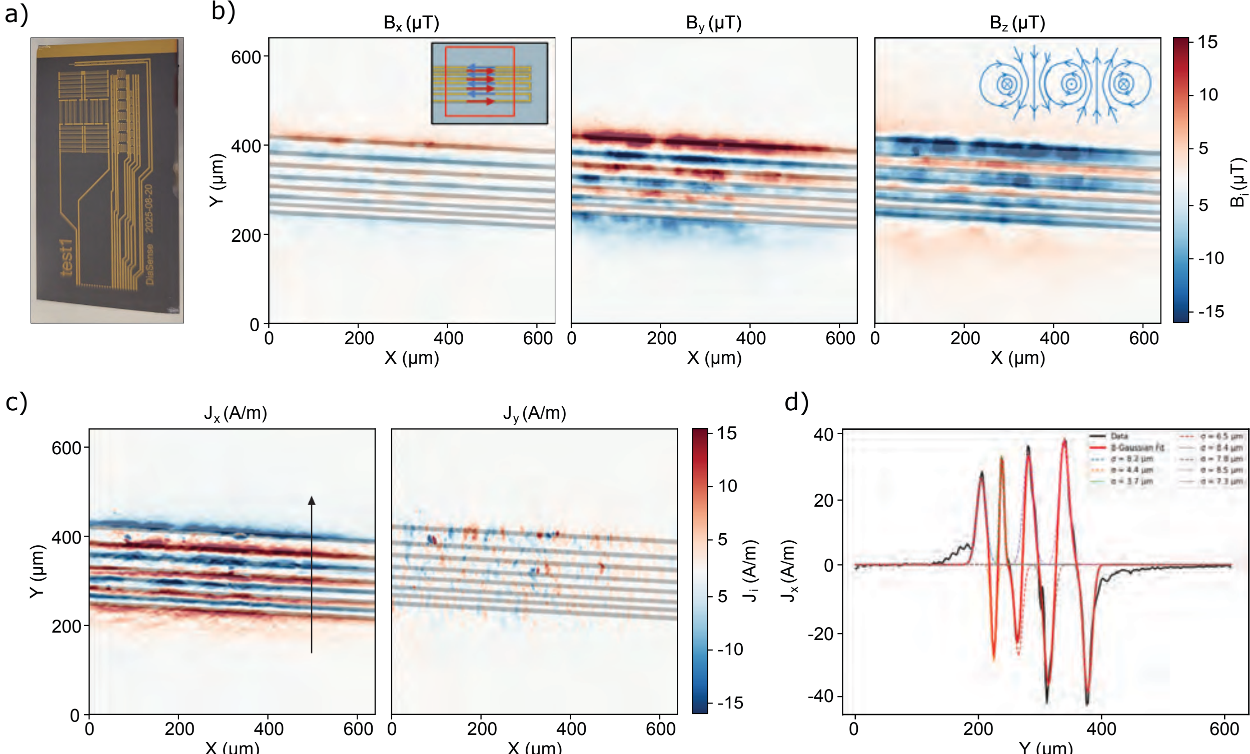

Figure 2 ***a)*** *Chip with test structures with smallest features size 10 µm.* ***b)*** *Vector components of magnetic field, with the meandering test structure in gray in the background. Inset shows the test structure and current directions* ***c)*** *Reconstructed current density in x- and y- direction in test structure, obtained from data in b).* ***d)*** *Line-cut along the y-axis in of the current density in x-direction in c), fitted with 8 gaussians (as there are 8 wires), demonstrating a spatial resolution of ~5µm.*

The corresponding current distribution is reconstructed by inverting the Biot–Savart law following established magnetic inverse methods [5,6]. The resulting map (Fig. 2c) accurately reproduces the expected current path. Gaussian fits to line profiles perpendicular to the wire yield a spatial resolution of approximately 5 µm (Fig. 2d), limited primarily by the optical system and standoff distance in this prototype.

These results demonstrate the feasibility of wide-field NV magnetometry for semiconductor current mapping and lay the foundation for our upcoming system upgrades.

OUTLOOK

The next-generation Quantum Diamond Magnetic Microscope (QDMM) will combine enhanced NV diamond sensors, high-bandwidth quantum control, and advanced signal processing electronics to achieve magnetic sensitivities below 10 nT/√Hz, spatial resolutions below 500 nm, and real-time full-frame imaging (<10 ms). By overcoming the traditional sensitivity limits, our QDMM will enable non-invasive, high-throughput mapping of 3D current flow and magnetic fields in complex integrated circuits. These capabilities position quantum diamond microscopy as a powerful emerging tool for semiconductor failure analysis and process monitoring, addressing the growing need for reliable, depth-resolved diagnostics in advanced 3D microelectronics.

***Table 1** Target specifications of final QDMM device*

Property	Target Specification	Prototype Specification
Magnetic field sensitivity	10 – 100 nT/$\sqrt{Hz}$	< 1µT /$\sqrt{Hz}$
Current sensitivity (100µm standoff)	1µA/$\sqrt{Hz}$	1mA/$\sqrt{Hz}$
Spatial resolution	< 500 nm	< 5µm
Field of view	3*3 mm^2	0.6*0.6 mm^2
Measurement time	< 1 µs < 10 ms (full image)	< 1 min

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KEYWORDS

Quantum sensing, magnetic field imaging, nitrogen–vacancy centers, optically detected magnetic resonance (ODMR), widefield magnetometry, semiconductor failure analysis, 3D current reconstruction, non-invasive metrology, diamond quantum sensors, advanced packaging, 3D ICs, nanoscale current mapping, quantum metrology, magnetic microscopy, fault localization.

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Critical Review of Electron-beam-based Junction Examination Techniques in Power Semiconductors

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Abstract— **In In recent decades, the development of Wide Band Gap (WBG) semiconductors has enabled the design and fabrication of increasingly high-performance power devices capable of operating at voltages above 2000 V. Moreover, thanks to their superior heat dissipation characteristics, these devices have been made smaller compared to silicon (Si) devices operating at lower voltages. However, this progress has posed challenges for the field of failure analysis and fault isolation, which must now move beyond traditional techniques effective for Si devices but less suitable for WBG devices. Among these challenges, it is particularly important to identify issues in the p-n junctions of WBG devices to better understand harmful effects that, while evident electrically, remain difficult to detect through fault isolation methods. In this paper, we addressed junction issues in 4H-SiC and Si devices using electron-beam-based techniques EBIC, knowing their inherent ability to image at higher resolution than traditional and OBIRCH techniques based on infrared or green wavelengths.**

I. INTRODUCTION

Power MOSFETs are fundamental components in power electronics due to their ability to handle high voltages and currents with fast switching speeds and high efficiency. The device operation critically depends on the threshold voltage (Vth), which defines the gate voltage required to form a conductive channel between the source and drain terminals. The source-drain junction, a key element of the device structure, must maintain a robust high-voltage reverse bias to prevent leakage currents and breakdown phenomena within the specified device limits. Understanding the electrical behavior and integrity of this junction is essential for optimizing device performance and reliability, especially in wide bandgap semiconductor technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN), where higher breakdown voltages and thermal stability are achieved [1].

A generic power MOS is shown in Figure 1, where the terminals Source (S), Gate (G), and Drain (D) can be clearly identified. This image highlights the important role of the Source-Body *p-n* junction in forming the channel that allows current to flow from Source to Drain.

The current flow between source and drain is indicated with red arrows in Figure 1.

Another *p-n* junction of fundamental importance is the source-drain junction, which is responsible for maintaining the high-voltage reverse bias so that, within the device's datasheet limits, no leakage or device breakdown occurs [2].

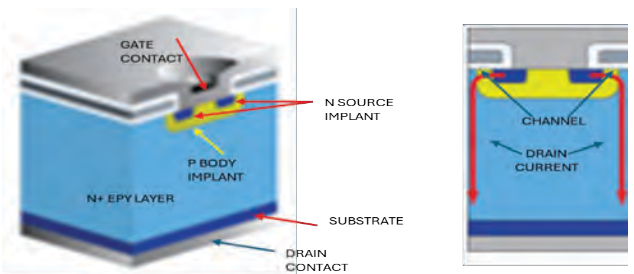

FIGURE 1: Power MOS Structure

Understanding whether the junctions of a SiC PMOS exhibit defects is essential for several critical aspects affecting the device's performance and reliability.

Regarding electrical performance, the junctions (such as the *p-n* junction) are key elements in the operation of the PMOS. Defects or problems in the junctions can cause unwanted leakage currents, which reduce device efficiency, variations in the threshold voltage, compromising channel control, and reduced carrier mobility, worsening conductivity.

They can also lead to reliability problems such as accelerated device degradation during operation, premature failures due to phenomena like junction breakdown or hot spot formation, and increased sensitivity to thermal and electrical stress, which are typical in SiC devices used in harsh environments.

From an energy efficiency standpoint, it is also important that the junctions are free of defects. Indeed, a device with faulty junctions consumes more energy, resulting in both static and dynamic losses, thereby reducing the overall efficiency of the system in which it is integrated.

Moreover, fault isolation on the junctions must be able to verify their quality and proper functioning. Therefore, we can affirm that in power devices like PMOS on SiC, the quality of the junctions influences fundamental parameters such as switching speed, switching losses, and the ability to handle high voltages and currents, all parameters that are essential in power electronics and automotive applications [3].

II. EXPERIMENTAL

The beneficial results and experimental difficulties of a number of ways of accessing the buried junctions in silicon-based Insulated Gate Bipolar Transistors (IGBT) and SiC MOSFETS was undertaken, using a Kleindiek Nanotechnik PS8e Prober Shuttle setup which included an EBIC amplifier and was inserted into a ZEISS GeminiSEM 300 field emission SEM for imaging and stimulation with an electron beam. Electron Beam Induced Current measurements were made [4].

st such examination was simply dropping a single probe on the top surface of an IGBT chip, obtained as a bare die. [5] (See Figure 2). At higher acceleration potentials, there was enough beam penetration to access buried junctions. This was not true, however, for all areas of the chip, nor for SiC MOSFETs, which had slightly thicker surface metal.

Secondly, a cleave of the chip provided a surface from which EBIC images could be obtained from the surface. This provided the convenience of being able to see across the full thickness, but provided some limitations in areas with useful data because of the roughness of the surface. Two view of EBIC are here shown in Figure 3.

Thirdly, other papers have tried using an etching technique to remove the surface metal, often used in order to provide a surface through which OBIRCH [6] measurements could be made, as shown in Figure . Then, EBIC was attempted through these areas. There was some difficulty in getting a good ohmic landing to the areas of interest, which provided irregular EBIC signal, as well as some difficulties in interpretation. These results on a SiC MOSFET [7] are shown in Figure 4.

Fourthly, a technique of partial delayering was attempted on some IGBTs. [8] This technique proved powerful in being able to access the buried junctions, such that prediction of the exact depth of the surface of the p-n junction were possible. A subset of these results are shown in Figure 5. This work has yet to be evaluated on a SiC device with a fail.

Fifthly, the method of preparing a FIB-milled window in a device has found some success on both IGBT's [9] and SiC MOSFETs [10]. Figure 6 demonstrates how a single needle placed on the surface may provide electrical contact to the N+ diffusions of the emitter areas of the device, which provide a clear EBIC signal of the depletion zones between the P-body and the bulk N of the device.

With additional probing, these windows have demonstrated a view into the actual working of the devices. Results have been shown for both the Si IGBT and the SiC MOSFET. One such result is shown in Figure 7. As the gate bias is changed, the depletion zone betwee P-body and N bulk gradually fades away, then the zones between the body and the N+ emitter become visible, and they to fade away. This is an observation of device turn-on.

FIGURE 2. EBIC measurements, top-down, on IGBT device. At higher beam landing energy, imaging of sub-surface depletion zones is possible.

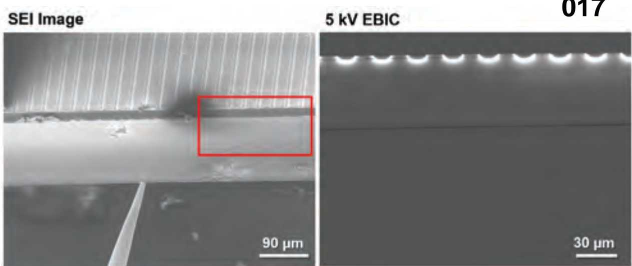

FIGURE 3. EBIC analysis on a cleave of an IGBT device.

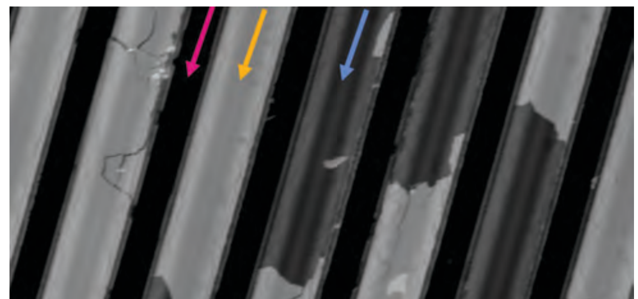

FIGURE 4. EBIC analysis, topdown, on partially-acid-etched SiC MOSFET. Red: gap between gates. Yellow: Region of gates with surface metal still on surface. Blue: the true EBIC signal depletion zones under the gates.

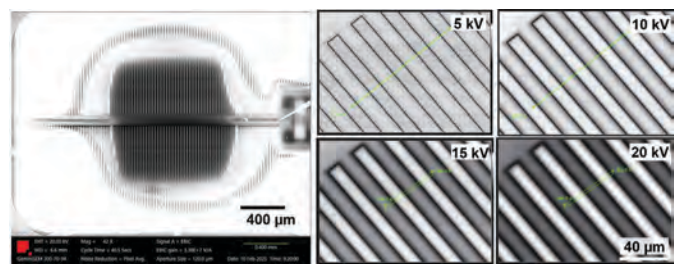

FIGURE 5. Investigation of buried *p-n* junctions on a partially-delayered chip, as a function of kV.

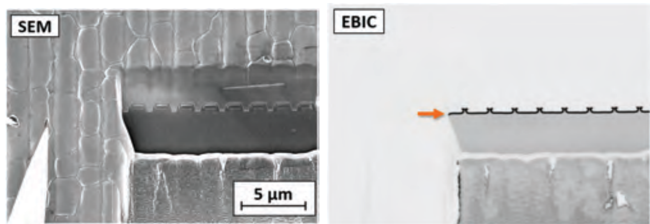

FIGURE 6. EBIC measurement on the SiC device through a FIB-milled window. Top: Inlens SEM image. Bottom: EBIC. Note some EBIC artifacts due to Ga^+ milling in the rough polished region, but a strong EBIC signal which defines the depletion zone of the devices in the area which was finely polished.

III. Conclusions

From what has been observed so far, we can deduce that despite the better resolution of EBIC compared to OBIRCH, for practical reasons we have used the two techniques complementarily. In fact, through OBIRCH analysis on the entire device [6], we isolated the area likely to contain the defect, which we then analyzed using EBIC. In this way, we

combined the practicality of the OBIRCH technique for analyzing the entire device to identify the anomalous area with the superior resolution of EBIC, due to stimulation by the electron beam, for detection in a specific region. Therefore, to summarize and justify what was observed in these tests, we can say that OBIRCH can be used as the primary screening technique because it is relatively fast and non-invasive, allows mapping of large areas of the device to identify suspicious or defective regions, and provides a qualitative indication of resistance variations related to defects or anomalies. Meanwhile, EBIC can be employed as a focused and detailed analysis technique because it offers high spatial resolution and electrical sensitivity, allows precise characterization of nature and impact of defects in the junctions, but is more time-consuming and resource intensive.

Further investigation will be to examine a device with *Vth* or *BVdss* issues and to verify, through the process flow just described, whether we will be able to detect differences in the junctions that could explain the electrically measured discard.

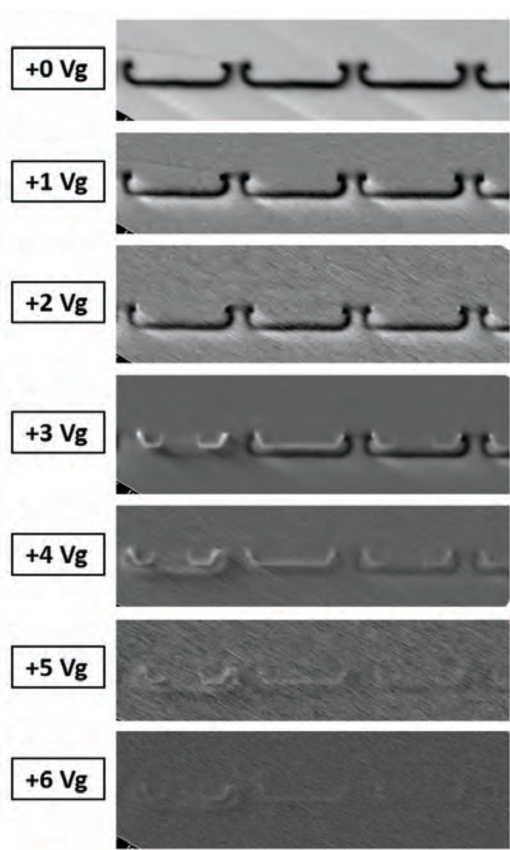

FIGURE 7. View of a series of EBIC measurements on three nearby devices in the field of view, seen, from the FIB-milled window on the surface of a SiC MOSFET. As the gate voltage increases, the depletion zone between the P-well and N regions disappears, indicating inversion of the channel. Eventually at higher gates, no depletion zones are observed.

Keywords—WBG, Fault isolation, Failure analysis, EBIC, OBIRCH, PVC, SEM

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Comprehensive Failure Analysis Workflow for Wafer to Wafer Bonding Vias

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INTRODUCTION

The future of complex packaging for data centers and the like relies on Heterogeneous Integration [1] [2]. Through-Silicon Vias (TSVs) and Wafer-to-Wafer (W2W) interconnects [3] [4] are key device elements for this progress. Failure analysis methods [5] must keep pace with these developments. The optically-based techniques of OBIRCH and LICA have shown great value in the ability to provide on-wafer localizations but are becoming increasingly inadequate for cases with more aggressive bonding pitches (<0.5 µm) where the diffraction limit of light imposes fundamental constraints [6] [7].

SAMPLE AND PROCEDURE

Electrical measurements were conducted on interwoven daisy chain structures across the wafer. The critical designs consisted of three long, interwoven pairs with the smallest PAD pitch of 400 nm and a minimum critical dimension (CD) of 200 nm. Circular PADs and hexagonal grid design were implemented to enhance process control, as described in prior work [6] [8][14]. Sites with resistances in the range of GΩ, as opposed to expected levels in kΩ, were chosen for analysis. The top silicon of specific areas, such as those around these daisy chains, were selectively etched from the top wafer, stopping close to the pre-metallization dielectric (PMD) layer. As is clear from Figure 1, considerable material is still above the active via chains, on the order of 600 nm (300 nm PMD + 300 nm SiO_2).

The failing chips were examined by a combination of XRM (X-ray Microscopy), EBAC (Electron Beam Absorbed Current), and FIB-SEM tomography.

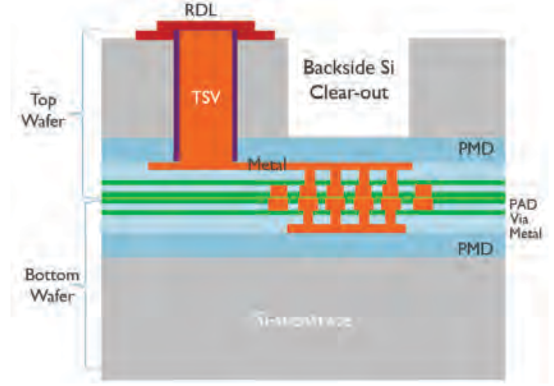

FIGURE 1. Cross sectional view of the sample. After bonding, backside Redistribution Layer (RDL) on the TSV are implemented to provide the necessary electrical measurement pads.

ANALYTICAL APPROACH

A. EBAC isolation of a buried, 400-nm pitch chain

Samples were bench-verified and then examined by EBAC [10] [11] [12] [13] with a Kleindiek Nanotechnik PS8e Prober Shuttle setup in a GeminiSEM 300 electron microscope. The state of the sample surface provided several challenges in the analysis. With 600 nm of dielectric over the chain of interest, a 5 kV beam landing energy was required to penetrate deep enough into the sample to image the chain. Nevertheless, EBAC isolation across a net on the mm-sized array was possible, as shown Figure 2. Open isolated from both ends.

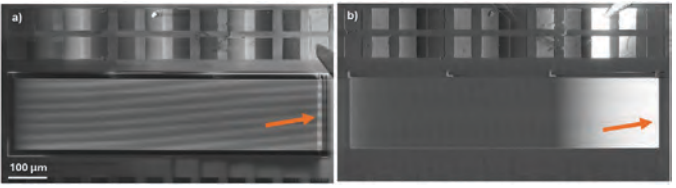

FIGURE 2. Two EBAC analyses of the chain. A) EBAC isolation from the right side. B) Isolation from the left side, highlighting the same link, providing assurance there was a single failure.

Figure 3 reveals the EBAC isolation on the chain of interest. Because of the three, intertwined chains, a complicated counting system had to be undertaken, shown in the right half of the figure.

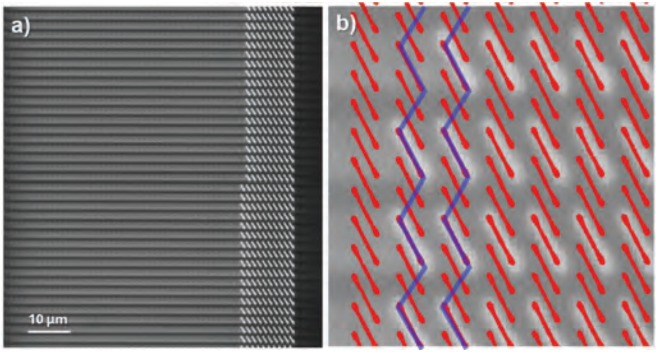

FIGURE 3. EBAC localization on a GΩ-resistance chain. A) raw EBAC data. B) A working aid for identifying the exact failing vias, based on a combination of EBAC (grey) SEM image of the top surface (red), and the stitch of the chain (purple)

B. FIB-SEM of failed site on 400-nm pitch chain

Results from a FIB cross section in a ZEISS Crossbeam 550L are shown in Figure 4. Electron-beam deposited Pt markers were applied to the top surface, a lamella prepared, and the area of interest examined with STEM imaging at 30 kV. Line foreshortening was seen.

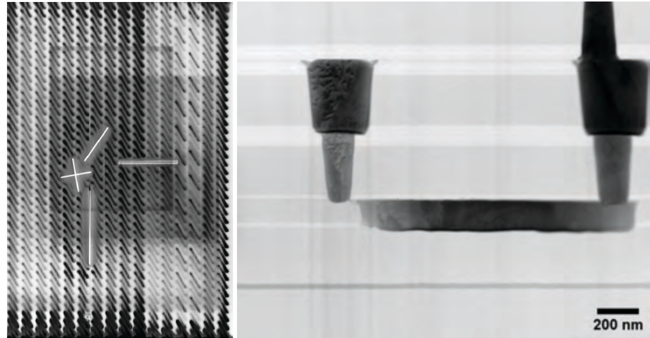

FIGURE 4. Sample prep and STEM results of the open isolated in Figure 3. Foreshortening of a line is seen.

Given the significant amount of time and operator skill required for such a targeted lamella preparation, the possibility of using FIB-SEM tomography to characterize such interconnect structures was examined. To this end, a FIB-SEM tomography dataset was acquired on a chain close to the lamella site. The dataset was produced with 5 x 5 x 10 nm voxels, Although voxels of 1 x 1 x 0.5 nm are possible, the larger voxel size was chosen to avoid excessive data acquisition time The acquisition time depends on the ratio of voxel size to volume size), while still providing sufficient 3D detail. This sample showed strong surface charging but could still be used for data acquisition without metallizing it. Residual charging induced image distortions were removed in post-processing. From these results, a more thorough examination of bonding overlay, detect etch problem, variability of CD across the array (center to edge, etc.), overlay, pitch walking, etc. may be obtained. A tomographic, fly-through video is available. The resolution of the resulting tomographic reconstruction are shown in Figure 5. The 3D resolution appears sufficient to verify the integrity of the array. It may also be the case that some complicated structures, there could be difficulties in creating a lamella that precisely captures the open link.

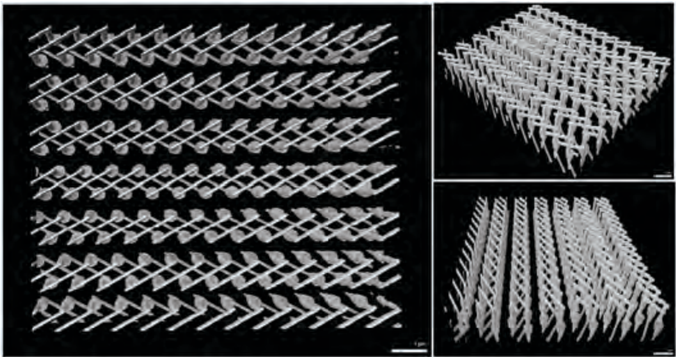

FIGURE 5. FIB-SEM tomographic reconstructions of the area nearby the failure allows examination for various problems with alignment or foreshortening.

C. X-Ray Microscopy on 1-µm pitch chain

As an added step to consider the overlay in the sample, a separate sample from a different test site on the defective reticle was examined with X-Ray microscopy [14] . First, an 80 µm pillar was FIB milled out of an array chain in a ZEISS Crossbeam 550L. The 1 µm-pitch chain from a region of the sample was chosen for this purpose. The dimensions were small enough that a near-conical structure could be shaped in a few hours. The resulting structure is shown in Figure 6.

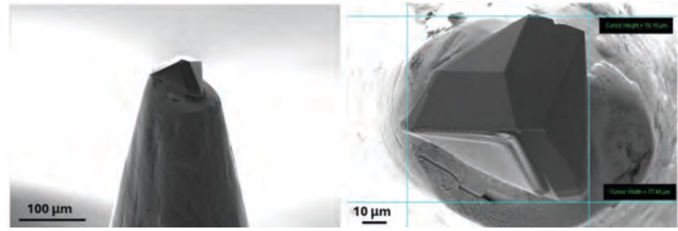

FIGURE 6. Low and high-magnification SEM views of the conical sample constructed from a nearby via chain for the purpose examination in the Ultra XRM.

This pillar was then examined in a ZEISS UltraXRM 9.2 KeV, X-ray microscope. Large field of view images were taken at 19.5 nm/voxel (FoV 38.2µm) and displayed in Figure 7. Precise measurements of overlay and foreshortening are possible. A tomographic, fly-through video is available.

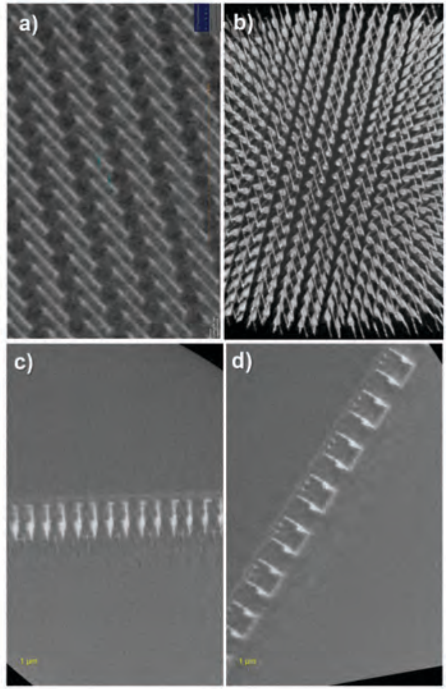

FIGURE 7. XRM results on a random view of the 1 µm-pitch chain. A) plan view of a slice, concentrating on the bottom links B) 3-D visualization of the chains C), D) Virtual cross-sectional views of the links in two different directions.

IMPACT OF WORK

This multi-modal analysis builds on the work earlier reported in **[15]**, the finding will helps to further understand the challenges of the hybrid bonding pitch scaling and to help to improve the yield from the process and design. It also demonstrates the range of techniques capable on a small scale.

KEYWORDS

EBAC, vias, XRM, FIB, tomography W2W, bonding, PAD, microscopy

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TEM/STEM observation and Analysis for Advanced Characterization of 2 nm process and below

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INTRODUCTION

The continuous scaling of semiconductor devices has led to the introduction of complex three-dimensional architectures such as gate-all-around (GAA) transistors. As device dimensions shrink to the nanometer regime, critical dimension (CD) measurements that were traditionally performed by CD-SEM are increasingly being carried out using transmission electron microscopy (TEM) to achieve higher spatial accuracy and structural fidelity[1]. Consequently, the number of TEM observation required for device qualification and process monitoring has grown explosively, creating a strong demand for higher throughput and measurement reproducibility. In addition, it is important to acquire the TEM and STEM image with appropriate conditions, such as convergence angle, detection angle, probe current and so on. We propose observation methods to efficiently manage these parameters and ensure consistent and reliable data acquisition for next-generation device characterization, and we deploy these methods in an automated system for data acquisition.

AUTOMATED OBSERVATION FRAMWORK

We developed a smart automated TEM workflow that dynamically controls key imaging parameters – such as convergence angle, detection angle, probe current and so on – to optimize imaging conditions for complex device structures. The automation system was implemented on a JEM-ACE200F with STEM Cs corrector. For cross sectional GAA-type samples, the automation routine adjusts the imaging mode according to the target information. It performs high – resolution and high – contrast imaging. Furthermore, automated transition between imaging and alignment, EDS analysis was integrated, enabling seamless analysis with changing probe current without operator intervention.

Issue in STEM observation of advanced semiconductor devices

The JEM-ACE200F is equipped with STEM Cs aberration corrector and can be installed with an electrostatic dose modulator[2] (EDM) that can control the electron dose. STEM Cs aberration corrector is an indispensable tool for materials analysis because it can achieve high STEM image resolution and high probe current density. This is achieved by increasing the electron beam convergence angle. However, as the convergence angle increases, the depth of focus decreases. As cutting-edge semiconductor devices become increasingly miniaturized, observation is increasingly being performed at high magnifications, and this shortens the depth of focus, resulting in different focus point shifts. This is due to slight differences in height between the constituent materials. While this allows for high-resolution observation, it may not be possible to clearly observe interface, which are important for CD measurement. Furthermore, the high probe current density raises concerns about radiation damage to the sample. Therefore, we

considered the electron optical conditions suitable for CD measurement under STEM Cs aberration corrected conditions, and also considered the effect of EDM on damage suppression.

Results and discussion

Because the transistors in advanced devices is small, the sample thickness for TEM/STEM analysis is 20 nm to 30 nm. As a result, fewer electrons are scattered through the sample, which tends to reduce the contrast of the HAADF image. Fig. 1 shows STEM HAADF image using the commercially semiconductor sample. Using JEM-ACE200F equipped with STEM Cs aberration corrector, HAADF images were acquired by changing the convergence angle. Focus was adjusted using the gate insulating film. STEM Cs aberration corrector is typically used with a convergence semi angle of around 20 mrad. Under these conditions, the amorphous/single-crystal interface is unclear. On the other hand, the contrast in this region improves at convergence semi angle of 7.5 mrad or less. Fig. 2 shows the line profile of the HAADF image shown in Fig. 1. This result also confirms that the material interface contrast improves at a convergence semi angle of around 7.5 mrad. In addition, the lattice of the single crystal was observed more clearly under conditions with smaller convergence angle, suggesting that the increased depth of focus is effective for acquiring field of view containing various materials in the same area. However, if the convergence angle becomes too small, as in the case of a convergence semi angle of 5 mrad, the STEM resolution may be significantly degraded due to the effects of diffraction aberration. Improving contrast and ensuring that materials within the field of view have the same focal position are important for achieving precise CD measurements.

As the sample thickness became thinner, the observation area became more prone to bending. Accurate alignment of the crystal zone axis at the region of interest is crucial for high-resolution imaging and reliable CD measurements. There is a function that performs automatic crystal zone axis alignment near the observation area. However, there is a risk that damage caused by electron beam irradiation will be included within the observation area. EDM systems can easily change the electron dose. Fig. 3 shows an example of irradiating Si single crystal with an electron dose of 20% for 1 minute. No contrast due to electron beam damage was observed. This is just one example, but we believe that the EDM system is effective for samples that are easily affected by electron beam.

Conclusion

It was found that by temporarily and instantaneously changing the convergence angle and electron beam dose during observation using a STEM Cs aberration corrector, it is possible to achieve precise CD measurements for some sample types. These parameters can be linked to JEOL automated data acquisition system, enabling optimized observation and analysis.

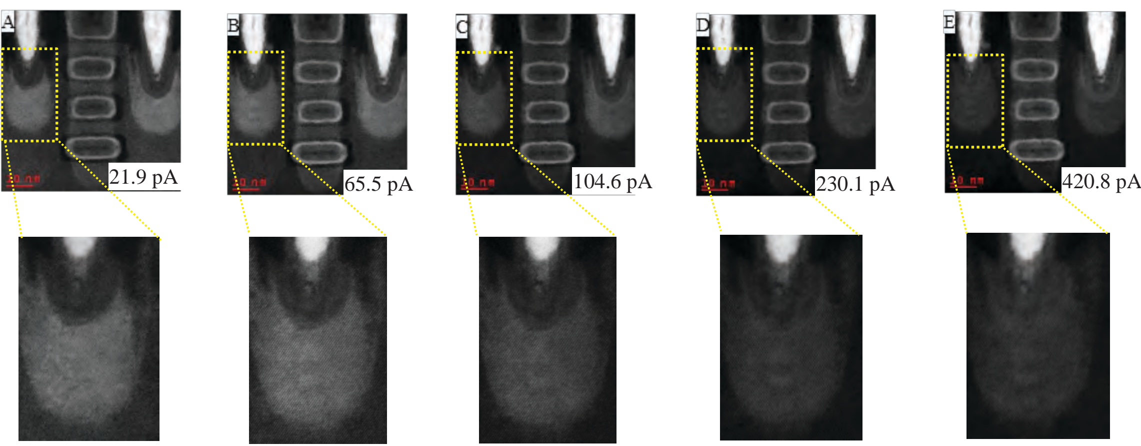

Fig. 1 HAADF images acquired by changing the convergence angle
(Convergence semi-angle, A:5mrad, B: 7.5mrad, C: 10 mrad, D: 15 mrad, E: 20 mrad)

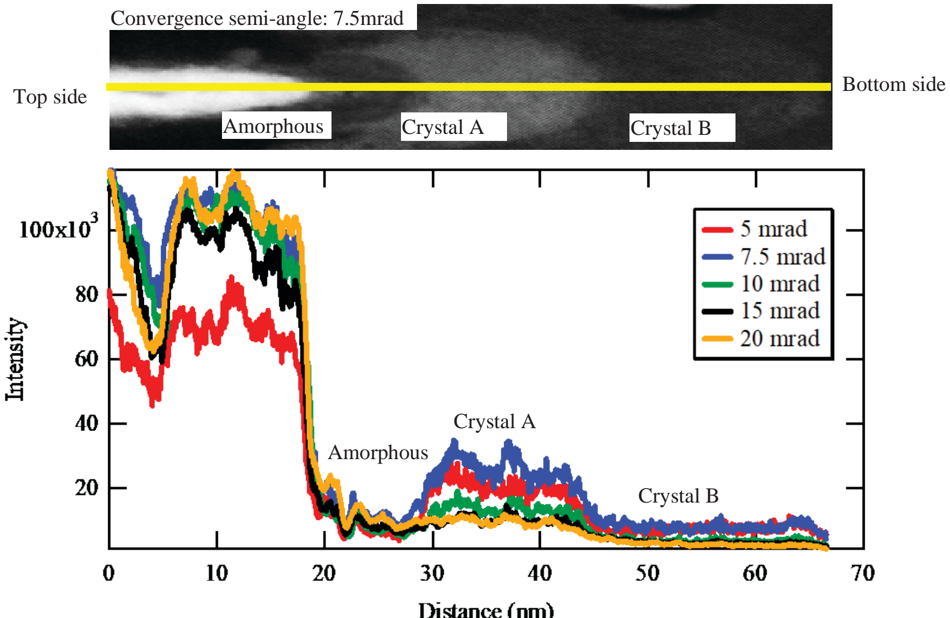

Fig. 2 Line profile of the HAADF image shown in Fig. 1

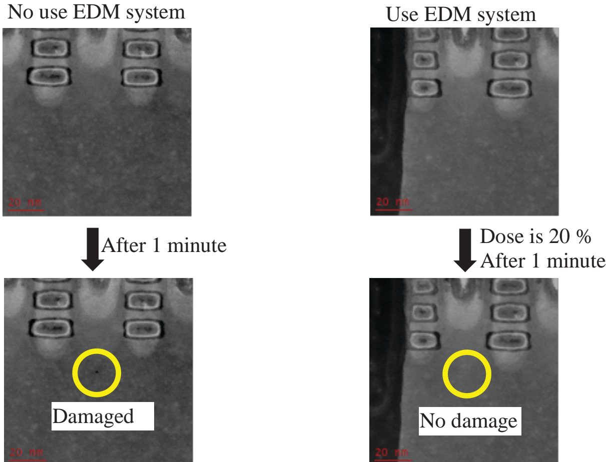

Fig. 3 Example of the effect of the EDM system
(Original beam current is 65 pA)

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KEYWORDS

Convergence angle, low contrast, CD measurement, EDM, low dose, Automation

Probing Defects in Commercial Power Devices Using Laser-Based Photoemission Electron Microscopy

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Withstanding higher internal critical fields, SiC power devices are considered to be ideal candidate for high-power applications than their silicon counterparts [1]. Devices fabricated on SiC epilayers hold advantages in high temperature operations, high current density, and fast switching which results in low power consumption, thus, leading to higher energy conversion efficiency [2, 3]. Different types of defects, namely micropipe, carrot, triangular, stacking faults (SFs), basal plane dislocations (BPDs), etc. can cause varying levels of degradation in device performance and may even result in total device failure [4]. Among these defects, BPDs are and critical in 4H-SiC, exerting a significant influence on device lifetime. BPDs can degrade device performance primarily because they may transform into Shockley stacking faults (SSFs) resulting in carrier recombination, leading to unpredictable forward voltage drift during operation [5, 6]. Therefore, over the past decade, significant research and metrology development have been devoted to identifying and mitigating BPDs and SFs. In parallel, body diode reliability studies are actively investigating whether extended defects in the epitaxial drift region of MOSFETs [7] contribute to device behavior. and reliability.

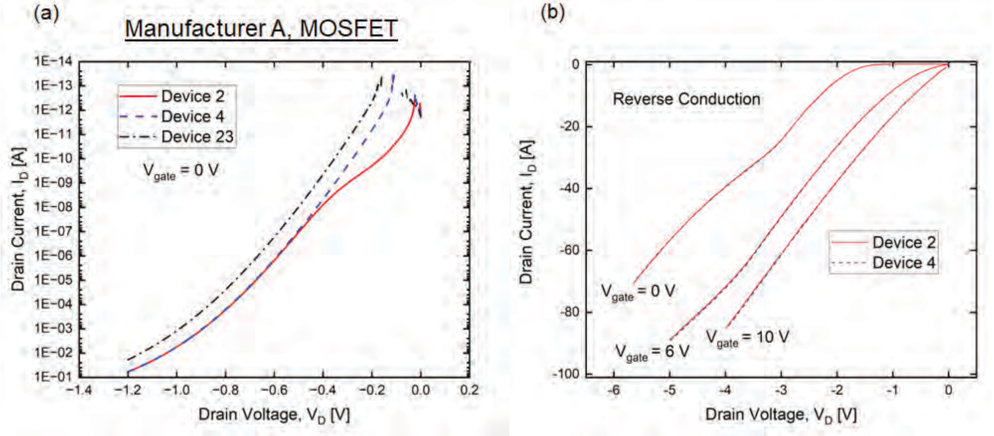

FIGURE 1. SiC MOSFET from manufacturer A. Electrical characteristics of the planar devices (a) at low V and low I, and (b) pulsed I – V at reverse conduction. Device 2 shows increased onset conduction at low voltages.

Posters

Commercial SiC planar metal oxide semiconductor field effect transistor (MOSFET) devices rated at 750 V and 3 A were procured, and initially screened at 3rd quadrant drain current – drain voltage (I_D- V_D) at low V and low I at gate voltage (Vg) of 0 V (Fig. 1a). In one instance, we observed a planar device that showed an increased onset conduction current of the body diode, differing from others that we probed (device #2 in Fig. 1a). It has been previously reported that a device demonstrating similar behavior had contained a carrot-like defect [7]. However, the device with the increased onset conduction current did not show differing traits at reverse conduction at high currents (Fig. 1b).

To further investigate the origin of this characteristic, we use photoemission electron microscopy (PEEM) to identify extended defects. Various inspection techniques are available that extract structural information from the sample surface or underneath [4]. These can be destructive such as KOH etching or scanning transmission electron microscope (STEM). Additionally, various microscopic techniques, such as scanning electron microscopy (SEM), atomic force microscopy (AFM), and optical microscopy (OM), can be used to examine the wafer surface and identify defects [8]. However, such methods have limitations, as it is challenging to accurately detect and classify various types of defects as they cannot reveal defects within the epilayer, such as BPDs and SFs. Photoluminescence (PL) allows intrinsic characterization of the substrate and epitaxial layers which included triangular defects, plane dislocations and SFs [9]. However, the high doping concentration of the 4H-SiC substrate often poses challenges for PL imaging, leading to low defect contrast and indistinct boundaries [10]. More recently, studies have been reported employing laser-based photoemission electron microscopy (laser-PEEM) to investigate and identify the defects in GaN [11] and β-Ga_2O_3 [12], and the technique shows promise for observing features that are not easily discerned by other microscopy techniques [11]. PEEM is a non-destructive technique that gives information about the electronic and chemical states of material surface based on the photoelectric effect. PEEM uses either UV light or synchrotron radiation for excitation of the electrons and collects primary and secondary electrons generated during the electron cascade that follows the creation of the primary core hole in the absorption process. In comparison to PEEM, scanning electron microscopy (SEM) and transmission electron microscopy (TEM) use focused beam of electrons that interact with the atoms of the sample.

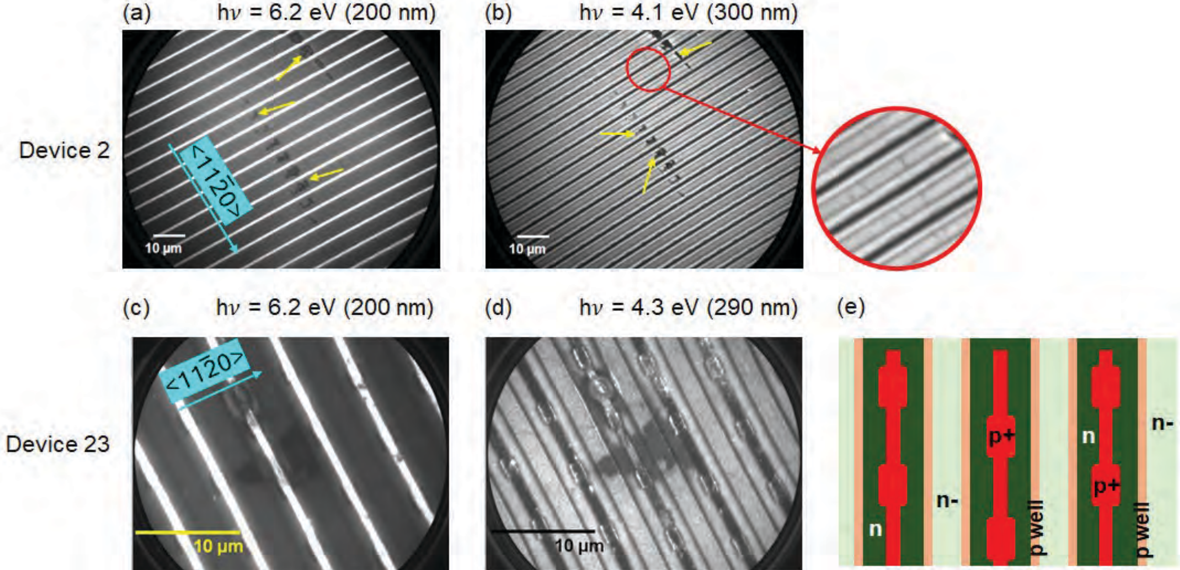

FIGURE 2. Laser-PEEM images of SiC device (a), (b) # 2 and (c), (d) #23. The images have been obtained at different laser wavelengths of which show the contrast enhancement of the defects. The scale bar is 10 µm. (e) represents the schematic of the different doping regions of the SiC device surface.

De-packaging was carried out using hot nitric acid, while de-layering was performed with dilute hydrofluoric acid. The devices were subsequently treated with a piranha solution – a mixture of concentrated sulfuric acid and hydrogen peroxide – to remove any remaining organic residues from the surface, as PEEM is highly sensitive to surface contamination. Fig. 2(a-d) shows the surface of the commercial SiC MOSFET where the source pads, dielectric oxide and polygate were removed by the de-packaging and de-layering procedure. The doping contrast is enhanced and inverted when imaging between 200 nm and 300 nm due to the work function contrast, which highlights that such regions are electronically different The different doping regions of the SiC surface is easier to discern at

wavelengths closer to 300 nm, and the n- epitaxy, n, p well, and p+ regions are identified from MOSFET device design [14] and shown schematically in Fig. 2e.

Laser-PEEM analysis of device #2 revealed multiple elongated features, highlighted with yellow arrows in Figs. 2(a-b), occurring at five different locations within the device structure. An example of such feature has been depicted in Fig. 2a which has been obtained at the laser wavelength of 200 nm (6.2 eV). Upon increasing the laser wavelength, i.e. 300 nm (4.1 eV), the image contrast was enhanced which further sharpened the features (Fig. 2b). Similar features have been reported as bar-shaped stacking faults [8, 13] observed by PL. In addition to these bar-shaped features, another set of elongated needle-like features were observed within the device (circled in red, Fig 2b) and evident at an increased wavelength. Both the bar-like and needle-like features are found close to each other in the form of clusters such that they are aligned closely along the $\langle 11\bar{2}0 \rangle$. The energy analysis is ongoing which can help us to unravel the presence of multiple electronic states within these areas in comparison to surrounding regions.

For the planar device that did not display an onset of conduction current of the body diode (i.e. device #23), we were able to detect (1) triangular-shaped feature by PEEM that is about 10 µm in extent on its longest edge in Figs. 2c and 2d. In contrast to the surface of device #2, no other feature was detected on the device #23 surface. Preliminary results indicate that the surface electronic structure of the triangular feature is similar to its surroundings. Like the rectangular bar-like defects seen in device #2, this triangular-shaped defect is also enhanced when exciting between 280 nm and 310 nm and the 290 nm excitation is shown in Fig. 2d. In SiC epitaxy, triangle-shaped extended defects have been detected in SiC epitaxy films like the triangular defect (e.g., 3C polytype inclusion), carrot (also referred to as comet), and Shockley stacking fault (SSF, where between two partial dislocations) [14]. The UV PL, SEM, and TEM are ongoing to further identify the triangle-shaped feature in device #23 and other features in device #2 to identify the physical origin of these features seen in PEEM. To date, this is one of the smallest triangle-like features imaged using a non-destructive technique. The triangular feature observed in device #23 and the elongated features in device #2 appear to originate from the n^- epitaxial layer and thus lie beneath the n, p-well, and p^+ regions. This observation supports the likelihood that these features correspond to extended defects.

The work presented here demonstrates the utility of PEEM for imaging such features, which are otherwise difficult to detect or require destructive methods using conventional SiC manufacturing techniques and investigates the physical origin of the increased onset conduction observed in the body diode.

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KEYWORDS

Photoemission electron microscopy, SiC MOSFET, laser excitation, surface cleaning, defects, BPDs, SFs

Scale calibration of AFM and characterization of AFM tip properties using a nano-structured certified reference material

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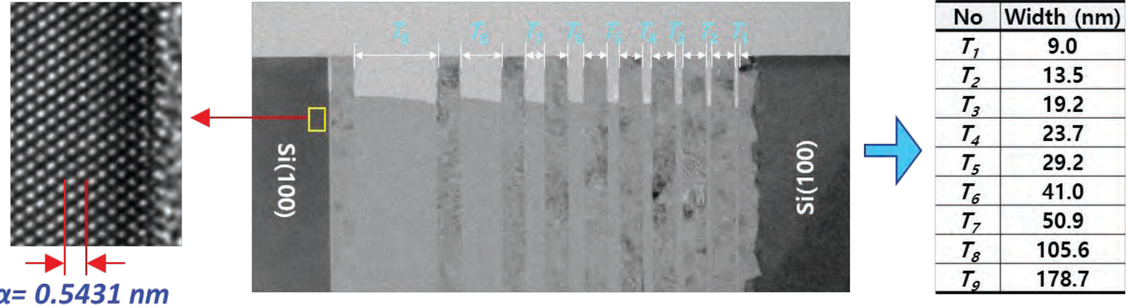
INTRODUCTION

Measurement of critical dimension (CD) for the nanopatterns is one of the most important metrology issues in the manufacturing process of the next-generation semiconductor devices. Recently, CD-scanning electron microscopy (CD-SEM) and CD-atomic force microscopy (CD-AFM) are the representative techniques for 2- and 3-dimensional CD measurements. AFM measurements analyze nano-scale materials differently from their real values, depending on the radius(r) and cone angle(α) of the tips used. To ensure the reliability of AFM images by correcting the offset value, we need to precisely determine the characteristics of AFM tips. The various trench widths (10-200 nm) of the certified reference material (CRM) are traceably certified via high-resolution transmission electron microscopy in reference to the Si (110) plane's lattice constant within the Si (100) substrate. For the reliable AFM measurements, the tip radius and the cone angle of the tip should be determined using a certified reference materials.

FABRICATION OF REFERENCE MATERIAL

A nanostructure AFM tip characterizer for the measurement of radius and cone angle of tips was fabricated by the process including bonding of the Si (100) wafer with the multilayer film, dicing to small chips with the size of 4 mm × 2 mm, fine polishing and selective etching of the SiO_2 layers by HF solution. This type of fabrication method has been well known. The nine trenches (T_1 to T_9) with trench widths between 10 and 200 nm were formed by selective etching of SiO_2 layers by the HF solution between the polycrystalline Si layers. The line widths between trenches and depth of the polycrystalline Si layers are 50 and 100 nm, respectively.

The trench widths of the AFM tip characterizer were certified from the lattice constant of a single-crystal silicon measured with the nanostructure using high-resolution transmission electron microscopy (HR-TEM). The silicon lattice constant was accurately determined using X-ray and laser interferometry during the Avogadro constant redefinition project to maintain the SI unit system in 2019.



No	Width (nm)
T_1	9.0
T_2	13.5
T_3	19.2
T_4	23.7
T_5	29.2
T_6	41.0
T_7	50.9
T_8	105.6
T_9	178.7

FIGURE 1. TEM image of the AFM tip characterizer for the characterization of AFM tips and a certification result.

The measurement traceability of the trench widths is available from the image scale calibration by the lattice constant under the same magnification. The Si unit cell is clearly observed in the Si (110) plane with the multilayer structure in the cross-sectional HR-TEM measurement. The Si lattice constant is the height of the Si unit cell composed of four d_{100} spacings and is 5.431 020 511 × 10^{-10} m with the standard uncertainty of 0.000 000 089 x 10^{-10} m. The certified trench widths of the reference material are traceable to the SI unit of length with a relative uncertainty of 1%.

RESULTS AND DISCUSSIONS

The AFM tip characterizer can be used to calibrate the AFM measurement scale in the horizontal direction. The reference pitch value (P_R) shown in FIGURE 2 can be used as the reference to calibrate the measurement scale by comparison the measured pitch value and certified pitch value.

The AFM tip characterizer can be also used to characterize the properties of the AFM tips as shown in FIGURE 2. Tip radius and cone angle can be intuitively estimated from the line profiles of an AFM tip characterizer. (1) Tip radius can be estimated from the penetration depth of the tip. If the penetration depth is deeper than the half value (W/2) of the trench width (W), it means that the diameter of the tip is smaller than the trench width. (2) Cone angle can be estimated from the "V shape" in the narrow trenches when the tip is closing to the bottom of the trenches. If the trench width is wider than the tip radius, the cone angle can be precisely determined by the Pythagorean theorem from the trench width and step-height. (3) AFM tips should be timely replaced for the reliable measurement. As shown in FIGURE 3, if the trench where the normal tip reaches the bottom can be set as a reference trench (T_6), the used tip is recommended to replace when it touches the bottom of a wider trench (T_8) due to damage or contamination. (4) If the certified linewidth is subtracted from the line profile of a Si line with wide trenches, the shape of the tip can be directly visualized. The reconstructed shape of the tip allows us to obtain the radius and cone angle of the tip.

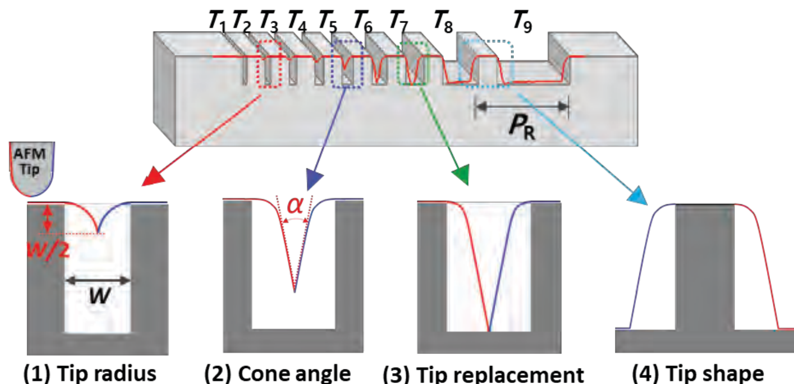


FIGURE 2. The applications of AFM tip characterizer to characterize the properties of the AFM tips

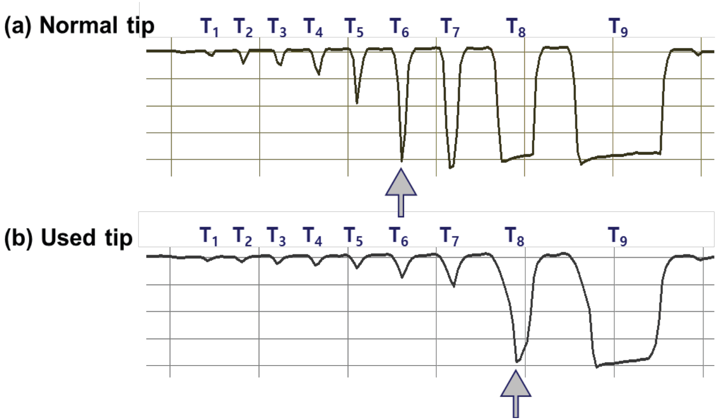


FIGURE 3. Comparison of the AFM line profiles by measured (a) a normal tip and (b) a used tip

To evaluate the tip characterizer, the shapes of various AFM tips measured by AFM were compared with those obtained through SEM. The SEM images of the tips were measured using the GEMINI 360 (ZEISS, Germany) with the acceleration voltage of 1.0 kV to investigate the shapes and sizes of four types of AFM tips. These tips, with different specifications were analyzed to discern their characteristics and to compare the results. SEM images, along with the radius and cone angle values for each tip, are presented in Table 1. FIGURE 4 shows the AFM line profiles of the AFM tip characterizer measured by the four different tips.

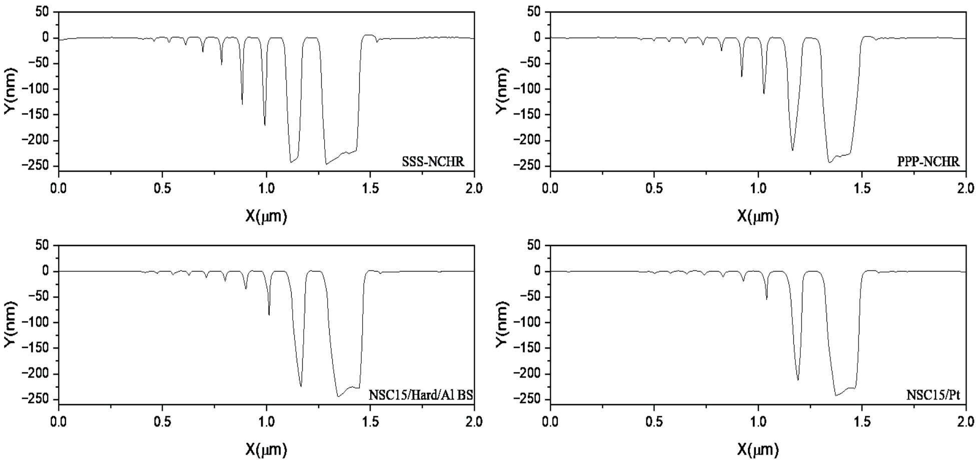


FIGURE 4. AFM line profiles of the AFM tip characterizer by four different tips

Both AFM and SEM measurements of cone angles show similar values, indicating their reliability. In contrast, discrepancies in the radius measurements were observed. This variance can be attributed to the limitation of SEM measurements of rounded nano objects. The signal from the rounded side area significantly decreases due to the emission pattern of secondary electrons, which follows a Gaussian distribution on the surface. As a result, it can be concluded that the tip radius and cone angle of the sharp tip by AFM are more reliable than those by SEM.

Table 1. The SEM images of four different tips and the measured tip radius and cone angles by SEM and AFM

Tip Name		SSS-NCHR	PPP-NCHR	NSC15/Hard/Al BS	NSC15/Pt
Manufacturer		NANO SENSORS	NANO SENSORS	Mikro Masch	Mikro Masch
SEM Image					
Radius (nm)	SEM	5.5	4.4	17.9	20.3
	AFM	5.5	7.3	14.8	16.3
Cone Angle (°)	SEM	10.2	16.2	13.6	15.2
	AFM	10.4	16.3	14.7	14.9

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KEYWORDS

AFM tip, Radius, Cone angle, Scale Calibration

Dispersion compensation in Multiwavelength dark-field Digital Holographic Microscopy for Overlay Metrology

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INTRODUCTION

The scaling of semiconductor chips imposes stringent requirements on overlay (OV) metrology, which measures lateral misalignment between successive layers of substrate on a wafer. Achieving sub-nanometer reproducibility is essential for maintaining robust process windows in optical lithography and enabling scanner corrections based on accurate overlay field maps[1]. Conventional diffraction-based overlay (DBO) metrology, widely adopted in industry to satisfy such demands, utilizes dedicated grating targets and derives overlay error from the intensity imbalance between the +1st and -1st diffraction orders of two biased overlapping gratings-a relationship that scales linearly with overlay. To address the limitations of DBO, recent work introduced dark-field digital holographic microscopy (df-DHM) with angular multiplexing, which leverages a reference arm for coherent complex-wave retrieval (Fig. 1). This approach enables advanced capabilities such as aberration correction, pupil apodization, and flexible pupil filtering[2]. While computational techniques for df-DHM have primarily focused on single-wavelength operation, multi-wavelength strategies are critical in current industrial DBO standards for swing-curve analysis[3] and material-dependent transmission effects, enhancing measurement robustness against process stack variations. Furthermore, multi-wavelength techniques open the path towards depth-resolved imaging which is beneficial for 3D-device detection schemes. These developments position df-DHM as a promising platform for next-generation overlay metrology across visible and infrared regimes.

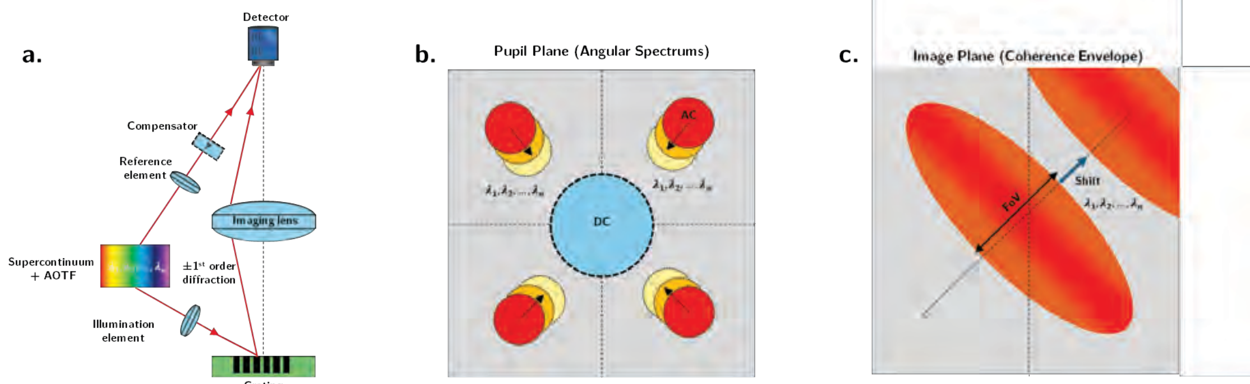

FIGURE 1. Illustration of multi-wavelength off-axis holographic recording of a DBO target. **a.** schematics of the df-DHM with supercontinuum source and acousto-optic tunable filter for wavelength scan. **b.** The angular spectrums in the Fourier space shifts when the wavelength changes. **c.** The coherence envelope in the retrieved image has a narrow width (FoV) due to the low coherence of the light source, which shifts as the wavelength is swept.

MULTI-WAVELENGTH DF-DHM

It was found that the light source originally intended for df-DHM requires a broadband supercontinuum source combined with an acousto-optic tunable filter (AOTF) to enable wavelength sweeping[4]. This configuration introduces a coherent envelope-manifested as washed-out fringes-in the interference pattern of captured holograms as shown in Fig.1c. The effect arises from the low temporal coherence of the broadband source combined with the

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angular difference between object and reference beams (off-axis configuration). Using the standard sideband-selection retrieval process (Fig.1b), the reconstructed hologram amplitude exhibits a narrow coherence envelope, which limits the suitability for large field-of-view imaging of diffraction gratings. This limitation can be mitigated by reducing the source bandwidth albeit at the cost of reduced optical power.

SHIFT OF COHERENCE ENVELOPE DUE TO RESIDUAL OPTICAL DISPERSION

Broadband interferometric techniques such as swept-source optical coherence tomography (SS-OCT) typically employ symmetric interferometer designs (e.g. Linnik or Mirau interferometry) to minimize optical dispersion between the object and reference arms. In contrast, our df-DHM setup was designed with minimal glass components for simplicity and efficiency. As a result of this approach, our holographic microscope has a difference in the number of glass elements between object and reference arms. This difference introduces a dispersion mismatch, resulting in a significant wavelength-dependent shift of the coherence envelope in the retrieved image (Fig. 1b and c). This shift is problematic for multi-wavelength DBO measurements, since it leads to a very large wavelength-dependent signal level variation. It is therefore necessary that we minimize this effect through dispersion compensation.

DISPERSION COMPENSATION VIA GLASS ELEMENT OPTIMIZATION

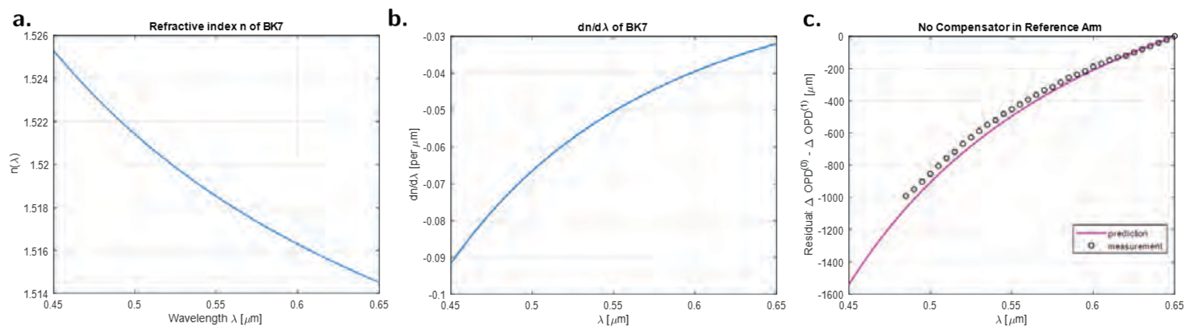

FIGURE 2. **a.** refractive index *n* of an example glass component (N-BK7) in the setup as a function of wavelength. **b.** first-order derivative of refractive index with respect to wavelength. **c.** total residual OPD between the object and reference arms without a compensator, showing both predicted and measured values to verify the model.

To stabilize the coherence envelope across wavelengths, the total OPD between the object and reference arms must be minimized. It can be shown[2] that dispersive OPD in broadband df-DHM mainly consists of two main contributions, $\mathrm{OPD}^{(0)}$: $\Delta \mathrm{S}^{(0)}(\lambda) = \sum_i W_i \cdot n_i(\lambda)$ and $\mathrm{OPD}^{(1)}$: $\Delta S^{(1)}(\lambda) = \sum_i W_i \cdot \lambda \cdot \mathrm{dn_i}/\mathrm{d}\lambda$, where W_i is the thickness of the i-th optical element, and $n_i(\lambda)$ is its refractive index as a function of wavelength, from which we can compute the analytical derivatives using Sellmeier's equation. In our setup, the object arm contains four glass elements, while the reference arm contains only one, leading to more dispersion in the object path. To compensate, we introduce a dispersive glass element (e.g. N-BK7) in the reference arm (Fig.1a and Fig. 2). By computing the OPD contributions of each component and applying a least-squares optimization (Fig. 3a and b), we determine the optimal thickness of the compensator that minimizes the residual OPD across the wavelength sweep. Fig. 3c and d show the OPD contributions both dispersion terms and the resulting residual OPD after compensation using a standard N-BK7 glass plate available in the lab. The measured points in Fig. 3c are in good agreement with the dispersion model. However, this available glass plate did not have the optimal thickness, hence not ideal for full compensation. Therefore, the optimization approach can be extended to alternative glass types with custom-fabricated thicknesses, where a near-complete dispersion compensation is expected.

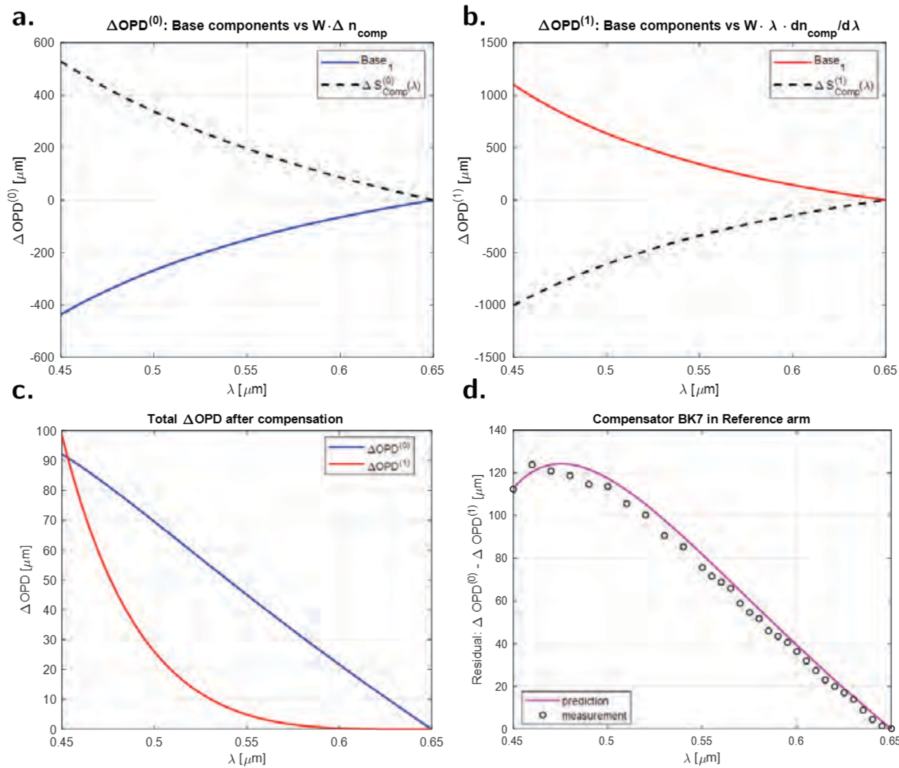

FIGURE 3. Least-squares optimization of compensator thickness for dispersion correction. **a.** and **b.** total $\mathrm{OPD}^{(0)}$ and $\mathrm{OPD}^{(1)}$ contributions from the original glass elements (base) and the compensator (with its optimized thickness). **c.** Combined OPD contributions from both terms after the compensation. **d.** The predicted and measured total residual OPD curves after the compensation with N-BK7.

CONCLUSION

We have demonstrated that a difference in glass elements between object and reference beams in multi-wavelength df-DHM introduces wavelength-dependent shifts in the coherence envelope due to the residual dispersion. By analyzing the materials and thicknesses of glass elements in both arms, we applied a least-squares optimization to minimize the residual wavelength-dependent OPD. While an exemplary standard N-BK7 glass plate provides partial correction, the remaining OPD suggests more dispersive materials (e.g. Schott SF) and computational methods may be required for full compensation. These findings establish a foundation for dispersion control in multi-wavelength df-DHM, enabling stable coherence envelopes and minimal phase drift, which are essential for achieving high-precision and robust multi-wavelength overlay metrology in advanced semiconductor manufacturing.

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KEYWORDS

Semiconductor metrology, digital holographic microscopy, dispersion, overlay, multiwavelength imaging

New perspectives to Thin Film Metrology using Ultra- High Aspect Ratio test structures

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INTRODUCTION

The increasing use of high-aspect-ratio (HAR) structures in 3D NAND, DRAM and logic devices places new demands on atomic layer deposition. Even though ALD provides self-limiting growth, its performance inside HAR features can be affected by precursor condition, source stability and flow dynamics. These influences often remain undetected in traditional process monitoring approaches, which rely on blanket wafers or cross-sectional TEM sampling. By contrast, PillarHall® test chips with ultra high aspect ratio (aspect ratios >1000) test structures offer a way to observe film growth under controlled transport geometry, revealing subtle shifts and anomalies that are relevant for real device fabrication. Although the current work does not aim to define full process windows, it provides early insight into the sensitivity of HAR structures to ALD variability and highlights phenomena that warrant further examination.

To explore these effects, lateral high aspect ratio (LHAR) structures with 100 nm and 500 nm gaps were used [1]. Standard ALD chemistries, including TiO_2 from $Ti(OiPr)_4$ and Al_2O_3 from TMA, were deposited under typical temperature and cycle conditions. Imaging ellipsometry and reflectometry were employed to characterize penetration-depth profiles, while SEM was used to visualize nanoscale features inside the cavity. Several cases were intentionally examined: fresh versus aged precursor, initial ALD cycles after precursor cylinder replacement, and conditions known to influence the faint secondary film formation deep inside LHAR channels. Such characterizations in HAR structures can also be mapped into wafer-level (up to 300 mm)by using the FEOL compatible pocket wafer concept.

PRECURSOR AGING

The TiO_2 ALD ($Ti(OiPr)_4$ + H2O) showed a clear, systematic differences between fresh, moderately aged and significantly degraded precursor bottles (Figure 1). Fresh precursor produced a relatively steep decay in thickness as a function of depth, whereas aged precursor resulted in both reduced thickness near the opening and increased penetration deeper into the LHAR cavity. Even moderate aging, invisible on blanket wafers, produced measurable changes in cavity-fill behavior, indicating that HAR features can act as sensitive indicators of precursor condition.

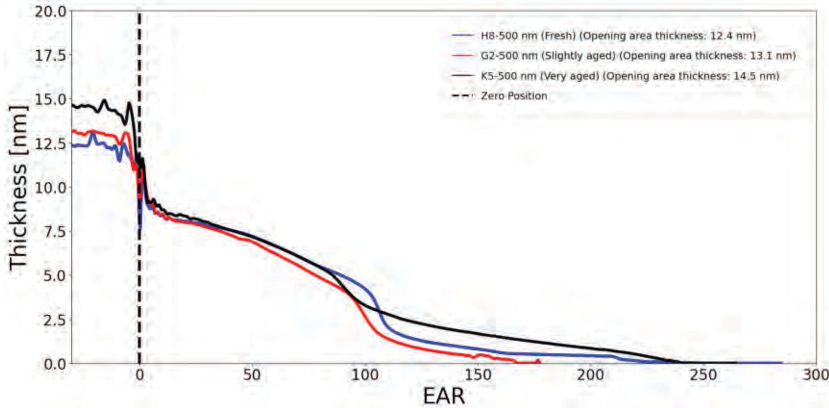

FIGURE 1. The penetration depth profiles of TiO2 deposition with different ages of $Ti(OiPr)_4$ precursor.

PRECURSOR REPLACEMENT

The Al_2O_3 ALD performed immediately after refilling a TMA cylinder revealed penetration-depth profiles that differed substantially from those measured after system stabilization (Figure 2). The first run showed shallower penetration and altered thickness gradients, while subsequent runs converged to a more stable shape. This observation, also seen in industrial reactors, highlights transient precursor-delivery variations that HAR structures can capture well before such shifts appear in conventional metrology.

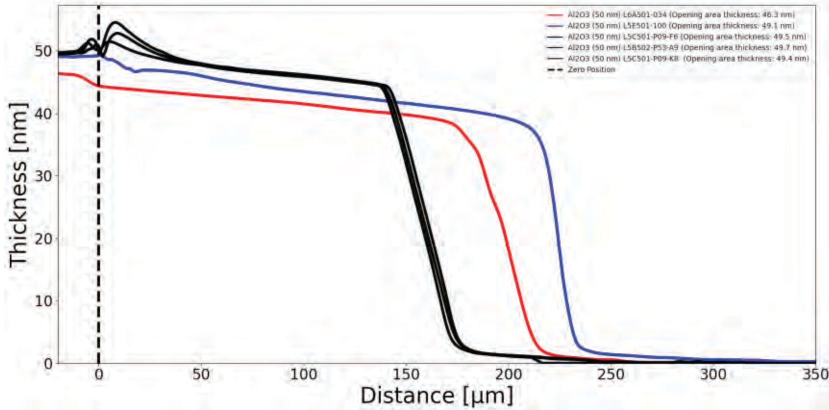

FIGURE 2 The penetration depth profiles of Al_2O_3 deposition right after the bottle change (blue), second run (red) and after multiple runs (black lines).

SECOND GROWTH FRONT

A third phenomenon consistently observed across different ALD conditions was the presence of an extremely thin film region deep inside the cavity, far beyond the main growth front (Figure 3). Although typically below one nanometer in thickness, this region was reproducible in top-view SEM and imaging ellipsometry. Its formation suggests that ALD films inside HAR structures can follow secondary reaction pathways under very low precursor pressure or low coverage conditions. While still under investigation, the presence of such faint film layers has implications for long HAR channels in advanced device architectures.

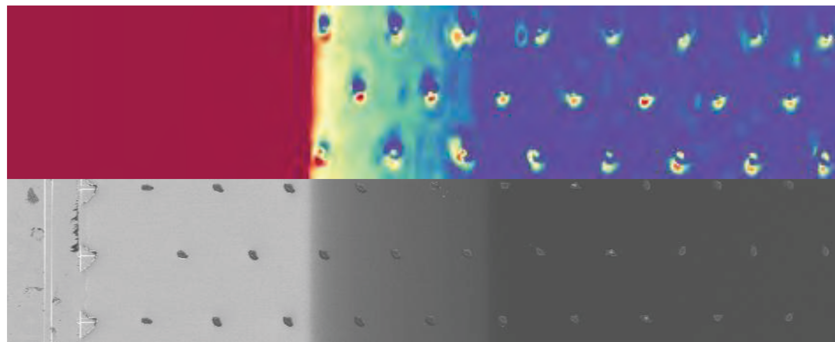

FIGURE 3. Imaging ellipsometer (top) and SEM (bottom) images of 12 nm Al2O3 penetration depths visualizing the second growth front deeper in the cavity (top: yellow, and bottom: dark gray). The dynamics of the color bar for the ellipsometer image is saturated (> 2 nm film = red) to enhance the visibility of second front.

POCKET WAFER

Experiments performed with the pocket wafer concept demonstrated that HAR testing can be integrated into wafer-level ALD workflows. Multiple LHAR chips were bonded to, e.g. a 300 mm carrier wafer, using FEOL-compatible materials, allowing measurements at various wafer locations in a production reactor. Even these early tests showed spatial differences in penetration depth and film thickness linked to reactor flow configuration, indicating that the pocket wafer approach can enable systematic HAR mapping across industrial-scale tools

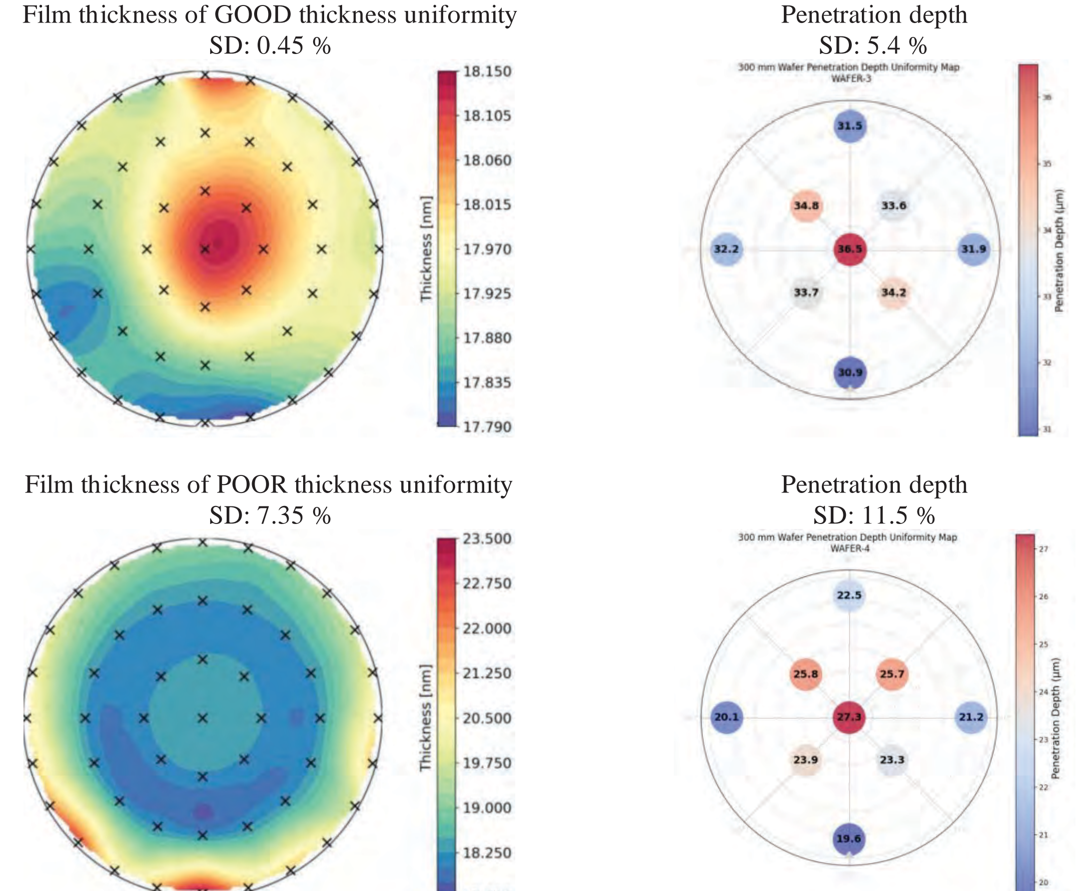

FIGURE 4. Film thickness mapping (left) and penetration depth distances PD50% (right) of two ALD processes.

DISCUSSION AND CONCLUSION

Collectively, these observations show that LHAR-based measurements can reveal ALD variability in ways highly relevant for advanced semiconductor manufacturing. Precursor aging, source stabilization after cylinder replacement and the formation of faint deep-cavity films all represent forms of process sensitivity that may influence HAR device structures but remain hidden in standard monitoring methods. The results underscore the value of having a controlled and repeatable HAR environment where such effects can be detected and compared in a practical way.

While these early findings do not yet establish comprehensive process-window boundaries, they highlight key mechanisms and instabilities that are important to understand as HAR dimensions continue to expand. The integration of LHAR chips into a 300 mm pocket wafer provides a promising path for applying these insights at the wafer scale, enabling more complete reactor-to-reactor comparisons and broader industrial evaluation. As the semiconductor industry moves further into complex 3D architectures, methods capable of capturing subtle ALD anomalies will become increasingly essential. HAR test structures provide a foundation for these efforts by revealing the nuanced behavior of ALD films under the constraints that define next-generation device geometries.

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KEYWORDS

High-Aspect-Ratio, Metrology, ALD, Process Window, Conformality

Failure Analysis and Fault Isolation Sample Preparation Technology for Integrated Circuits on Advanced Technology Nodes

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INTRODUCTION

Scaling trends in semiconductor process technologies are pushing the limit of failure analysis (FA) and fault isolation (FI). Breakthrough technologies such as Intel BSPD and GAA require novel approaches in addressing yield and reliability issues to optimize their process and performance goals. While optical probing methodologies continue to provide valuable insights, backside power delivery (BSPD) architecture has made defect isolation more dependent on nano-probing techniques to support fast, high volume, defect isolation flows. Correspondingly, increasingly high volume "prep for nano-probing" is a close partner in isolation activities. Focused ion beam systems (FIB) are frequently used for localized nano-probing sample preparation, particularly when signals of interest are within the device stack and must be "uncovered." A critical requirement of maintaining planarity across areas 0.01 – 10 mm^2 must be met to support downstream probing fault isolation flows. Challenges arising from very thick metal layers (~ 1 µm) abruptly transitioning to thin layers (~ 10 nm) with only a single intervening dielectric layer can result in significant difficulties in sample preparation achieving the required uniformity. Additional requirements such as ensuring good sample grounding, tensile or compressive stress distribution, thermal sensitivity and SEM sensitivity, can cause further complexities whenever BSPD power rails are removed. This poster aims to detail some of the choices and techniques required to prepare BSPD chips.

FRONTSIDE SIGNALS ARE BURIED

Next generation technology development and process scaling commonly begins with higher defectivity and previously unseen defect modes, especially in early process learnings. These defects must be addressed in a timely fashion to meet technology release timelines. Straightforward defect modes requiring isolation of the affected transistor(s) followed by a direct-to-TEM flow provide an ideal scenario. On the other hand, logic flows on test-chips and products often require more involved, iterative, FI and nano-probing flows to generate confidence and conclusive root-case FA of the defect. In many instances, specific fail modes at the device level, as in the case of resistive opens and others defect modes, can only be accessed through carrier silicon frontside preparation and probing flows.

On a "macro-prep" scale, accessing front-side signals requires silicon thinning. Bulk thinning of as-built silicon from ~300 µm to thickness < 1 µm by mechanical means requires sufficient care and robustness to ensure device integrity through the process. Common sample preparation techniques using silicon backers, rigid support films and frames, or even a package board generally provide sufficient support to maintain this integrity [1,2,3]. The main qualification for the support is the ability of the die to maintain its structural integrity through mechanical grinding

processes and if the die/support attachment method can withstand grinding and/or polishing wheel sheer forces [4]. Alternative process flows can involve chemical removal of silicon using standard techniques, well-known surface texturing methods, or a combination of the two approaches [5,6,7,8]. In some cases, it may be more favorable to only locally prepare the region of interest while retaining the die's silicon as the frame.

Once appropriate die support has been achieved, sample preparation can proceed using all the standard techniques of the technologies that preceded. Post mechanical preparation, sample mounting should ensure a conductive path to ground to prevent excessive charging under electron/ion beam processing. Grounding is typically achieved using conductive paints and adhesives [9]. Intel's first BSPD product, codename Panther Lake (PTL) has on the order of twenty combined metal layers [10] with the thickest of them pushing the limits of chemical assisted ion milling on a plasma FIB [11,12]. Fortunately, the most difficult aspect of frontside prep to maintain planarity is the carrier silicon bonding layer removal; the routing spacing and thickness is similar to monolithic architecture design rules thus no new techniques are needed.

PREPARATION FROM BACK METAL SIDE

Routinely, signals on the contacts side need to be accessible to provide additional localization of the failure to a smaller region of interest (ROI). Specific cases where front-side FI techniques more suitable to volume preparation are ineffective, such as subtle resistive gate or driver defect modes, require DC backside probing and therefore necessitate deprocessing through the BSPD power delivery routing. Power rails connected to transistors tend to have similar thickness and spacing to frontside metals layers; however, routings connected to micro bumps are much larger in comparison. Intel's 18A process backside power delivery rails comprise a stack of up to six metal layers, with approximately half large metal layers with thickness significantly larger than a micron and the remainder layers with thickness ~ 10-140 nm, with an abrupt transition between the two dimensionalities [10]. Large metal layers require macro-scale removal techniques typical of monolithic architecture bump-side deprocessing but, with BSPD, there is less wiggle room between the giant metals and the thinner metal layers than in previous technologies.

Further, the presence of a sensitive maxMIM capacitor layer between the top two giant back metals increases metal density variations locally and, correspondingly, increases the associated risks of standard prep techniques transferring topography which limit surface planarity for backside transistor probing. Integrated circuit (IC) designs, especially for large chips incorporating many blocks with distinct functions, can have significant variations in metal or via density at all device levels. Dynamic metal density must be considered when determining FA prep flows using bulk mechanical or selective chemical processes Additionally, preparation flows for defects requiring intact power delivery routing must take extreme care to avoid damage to critical areas. This requires high in-plane etch precision, in extreme cases removing material within 100 nm of critical signals for the ROI, and/or reconstruct critical traces removed by the preparation. Circuit-edit (CE) styled applications for reconstructing circuits can meet these precision and reconstruction requirements but frequently result in increased throughput times while also requiring a significant level of operator skill and expertise [13]. Both are prohibitive for high volume FIFA.

OTHER PREPARATION APPROACHES AND OUTLOOK

The previous sections detailed some of the critical challenges in FIFA sample preparation with BSPD. The complexity increases when backside probing identifies a frontside open that must be further isolated. The die must then be flipped with a solution to address resulting grounding and thin chip challenges are addressed before proceeding with frontside preparation. In general, the flip prep can be straightforward but may take advantage of circuit reconstruction. While these approaches provide a broad level of closure, the foundational shift resulting from BSPD and the reduced effectiveness of traditional optical FI methodologies have resulted in higher complexity front-side and backside FI. Packaging for optical FI is largely the same as it has been for monolithic architectures [15], but BSPD screens some of the optical and signals used in traditional FI and thus requires novel techniques. For example, electron beam probing of packaged parts requires complicated preparation processes combination of mechanical, PFIB, and selective chemical etch through a package hole. Secondary electron signal from toggling transistors on the packaged part requires a debug package and sample prep to have sufficient planarity to maximize

electron detection [16]. The added complexity demands significant effort and innovation, which further drives technique development and necessitates enablement of more specialized set of FI and FA tools [17].

Current challenges notwithstanding, FIFA improvements must keep pace with process technology development to support next generation IC manufacturing. Technical capabilities and skills are beginning to push the limits of physics, resulting in longer average FIFA time to defect required to fulfill defect isolation requests [16]. Developing specialized tooling and material selective approaches for yield labs must ensure these capabilities are able to address high volume and throughput requirements. Additionally, yield and FIFA engineers must continue to demonstrate skillset mastery over an array of macro, micro, and nano precision techniques to help them selectively implement the most effective technique for the job at hand.

The introduction of BSPD has already seen considerable development in multi-layer sample prep introducing multiple, intricate, front-side and back-side FIFA process flows. The current state of defect isolation allows relatively straightforward access to the transistors from either side, but must develop new techniques to support future technologies in enabling prep and isolation techniques requiring multiple localized access points and the introduction of different planes of prep. CFET process technology is expected to cause significant disruptions in traditional FA due to difficulties with precision isolation and routing reconstruction for stacked transistors[18]. As “one size fits all” preparation techniques lose efficacy for next generation ICs, planning for site preparation and probing complexities likewise increase. Computation will become a more critical part of the FIFA process with 3D CAD modeling, automated circuit tracing, and critical signal identification, and next generation bulk-ROI diagnosis will enable discussions and fill visualization gaps [18]. Prep will need to be able to manipulate transistor connections on frontside and backside[19] with more precision tooling. The techniques will rely on creative backside and/or frontside grounding schemes may make the prep not significantly different from other BSPD devices requiring flip and expand on the above grounding and circuit re-building techniques. Flips, which increases process flow time, will increase in frequency. With enough skill, more available computations, and precision tooling, many of the approaches developed for BSPD may also apply to future process nodes.

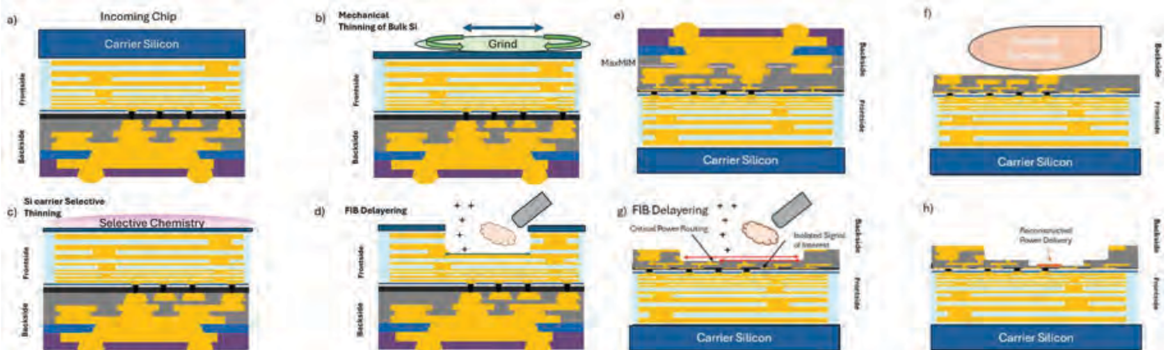

FIGURE 1. Overview of front-side sample preparation (a-d). All layers need a conductive bridging connection to ensure solid grounding (not pictured). a) Incoming chip with BSPD. Thick silicon covers frontside metal traces. b) Bulk silicon removal processes clear most of the silicon quickly by mechanical means. c) Silicon selective chemistry removes the remaining material to preserve planarity. d) Localized delayering using plasma FIB with gas injection assistance to even out differential mill rates using standard techniques. Overview of backside sample preparation techniques(e-h). e) Incoming ROI has bumps, backside metal, and MIM layer sandwiched between thick metal layers obfuscating. Back metals transition from ~1 µm to ~10 nm thick in various layers. f) Standard bumpstrip selective chemical etches removes any large unnecessary layers. g) PFIB techniques locally remove material. Tiered boxes avoid critical traces wherever possible. Standard gas assisted milling techniques are applied. h) Alternative to Critical power delivery covering the signal of interest is reconstructed in the appropriate FIB tool.

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KEYWORDS

Plasma Focused Ion Beam, ultrathin silicon, backside power delivery, sample preparation

Mineral Interface Doping: a safer alternative to doping silicon substrates with phosphorus/arsenic without hazardous chemicals

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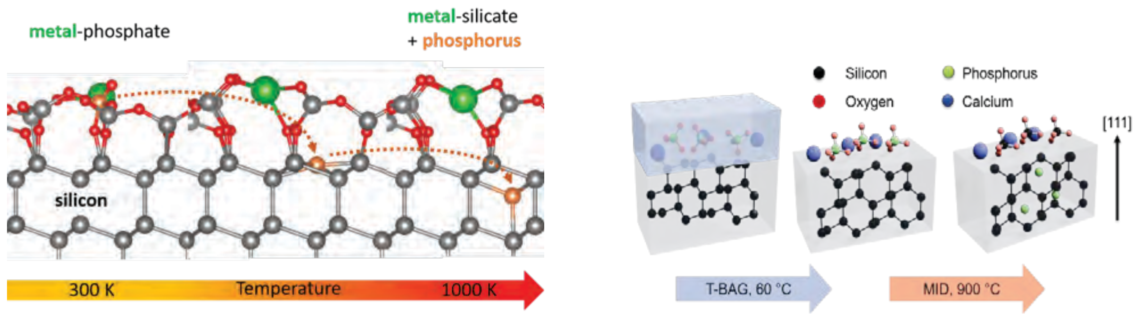
This work explores Mineral Interface Doping (MID): a safer alternative that offers a simple, reproducible, and industry-relevant approach to doping without hazardous chemicals. MID is an incipient method based on the deposition of a mineral containing the dopant of interest on a silicon wafer, followed by a rapid thermal annealing (RTA) step. MID can utilize a variety of minerals, that effectively form metal silicates in contact with silico , oxide. For this specific application, a mineral should consist of three components: a metal ion (K^{+}, Mg^{2+}, Ce^{3+} …), element that can be a source of electrons or holes in silicon bulk (such as P, As, B, etc) and oxygen/chlorine components.

The proposed method uses ultra-thin films of minerals, for example Hydroxyapatite ($Ca_5(PO_4)_3OH$), Struvite ($MgNH_4PO_4*6H_2O$), Cerium Orthophosphate ($CePO_4$), and Monopotassium Phosphate (KH_2PO_4), applied via the Tethering by aggregation and growth (T-BAG) process and activated by RTA. Infrared and Electrochemical mpedance Spectroscopy analyses confirm that phosphorus diffuses through native silicon oxide and into the silicon, altering its electrical properties. To further explain and investigate experimental doping processes using thin films of P-containing minerals, mineral interfaces were modelled and DFT calculations were performed. The Nudged Elastic Bands method provides us with the mechanism of phosphorus transport. Our findings reveal that the required doping temperature decreases with the charge density of metal ions, however there is a required minimum temperature to achieve diffusion of phosphorus into the silicon bulk. Finally, the metal silicates are emoved post-doping using non-toxic acids, thus making the process broadly applicable.



Figures (left): Side views of the phosphorus transport into a silicon (111) lattice, (right) Schematic description of 1) T-BAG @ 60 °C and 2) MID @ 900 °C.

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Keywords: phosphorus, doping, silicon, infrared, DFT, mineral

Effect of Strain on Morphology in CVD-grown Janus MoSeS Monolayers

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INTRODUCTION

In recent years, the family of naturally occurring transition metal dichalcogenides (TMDs) has been complemented by fundamentally man-made materials, so-called Janus monolayers in which the transition metal layer (e.g., Mo, W) is sandwiched between two different chalcogen layers (S and Se being the most popular). Lack of inversion symmetry in z-direction results in appearance of multiple fascinating and potentially useful optoelectronic, magnetooptical and catalytical properties in these 2D semiconductors. Understanding and ideally controlling the defects that may appear in Janus TMDs is of great importance for their future industrial applications.

Using cross-correlated AFM and TERS imaging, we will show how mechanical strain incurred during synthesis of the Janus precursor TMDs and the strain introduced by the Janus conversion process affect the morphology and chemical composition of the final Janus monolayers. Specifically, we will show that in case of Janus monolayers converted from $MoSe_2$ grown on SiO_2/Si substrate via room temperature atomic layer substitution, the original tensile strain of 0.6% is complemented by additional tensile strain of 1.8% at the conversion stage which results in physical rupture of the crystals into approximately 500-1000 nm wide domains, separated by gaps of 10-30 nm.

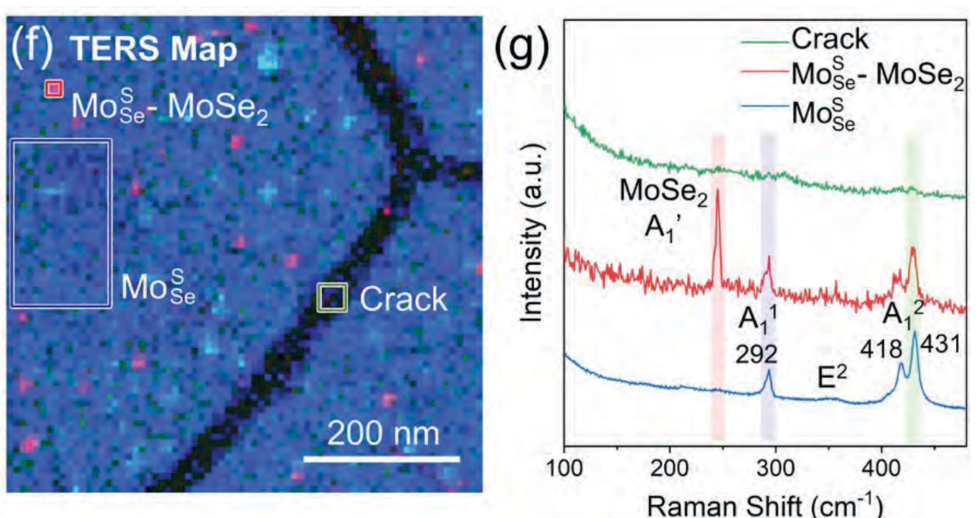

FIGURE 1. Deep-sub-diffraction-limit TERS image of MoSe on SiO2/SI, mostly converted to SeMoS, showing bare substrate in the cracks between the Janus film areas.

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In case of using MoS_2 grown on SiO_2/Si or fused quartz substrate as a precursor for Janus conversion, the original tensile strain incurred at the TMD growth stage is replaced by compressive strain at the conversion stage, which results in formation of wrinkles (in case of SiO_2/Si substrate) or nearly perfect Janus monolayers (in case of fused quartz substrate). In case of Janus conversion of $MoSe_2$ monolayers grown on annealed gold foil when the Se atoms layer at $MoSe_2$-gold interface is replaced with sulfur atoms [1, 2], the strain scenario is significantly different. Since gold has a much higher thermal expansion coefficient than $MoSe_2$, the precursor crystals experience a large compressive strain, which compensates for the tensile strain incurred at the conversion stage much better. The mechanical continuity of Janus crystals obtained via this synthetic route is preserved, though the crystals are divided into domains of similar size (500-1000 nm across) separated by narrow (10-30 nm) walls of fully converted MoS_2.

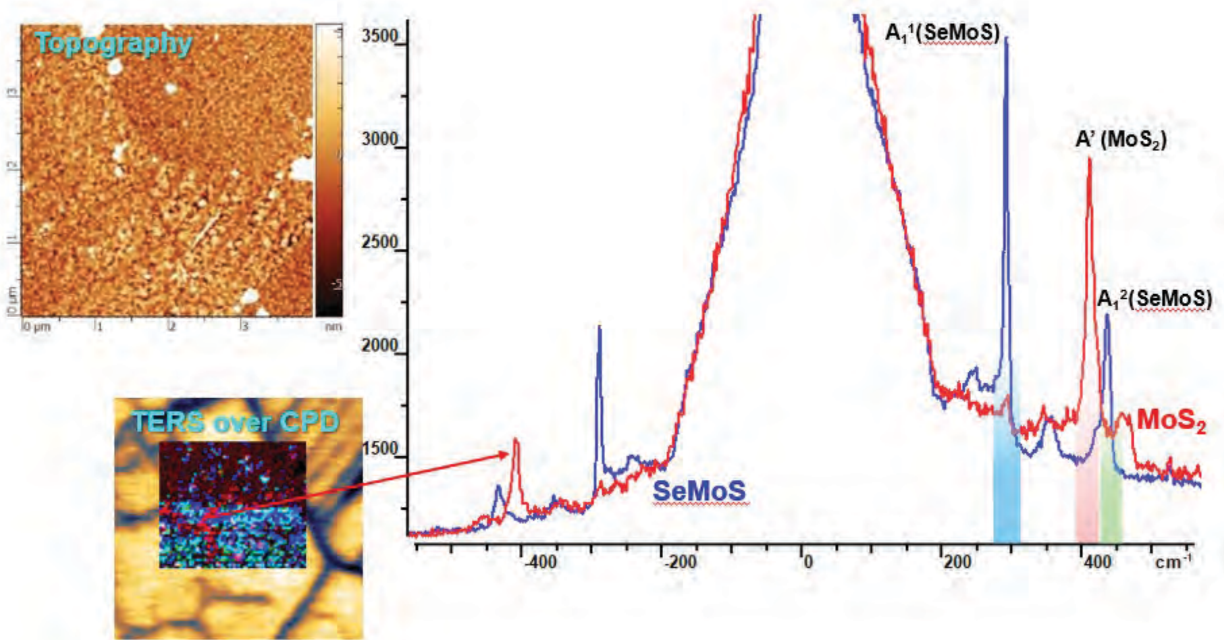

FIGURE 2. AFM topography and TERS image of MoSe on gold, superimposed over the AFM contact potential difference image, showing walls of fully converted MoS2 between the Janus film regions.

Fine peculiarities of Raman/TERS response of Janus monolayers obtained via two fundamentally different synthetic routes will also be discussed.

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KEYWORDS

AFM, TERS, TMDs, Janus films

Inline XPS and Raman Metrology for Evaluating Graphene Integrity During Thin Film Deposition

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INTRODUCTION

As semiconductor devices shrink below 2-nm, copper (Cu) interconnect reliability is increasingly constrained by electromigration and diffusion into surrounding dielectrics. Traditional capping layers such as Cobalt (Co) or Tantalum (Ta) provide protection but add unwanted parasitic resistance and limit further scaling. Graphene, a two-dimensional carbon material, offers a promising alternative due to its atomic thickness, high electrical conductivity, and impermeability [ref 1-2]. However, integration of graphene in the back-end-of-line (BEOL) stack requires protection of graphene structure and properties from the downstream processing steps such as thin film deposition, etching, cleaning, etc.

This work investigates the impact of plasma and thermally grown dielectric thin films on the graphene composition, thickness, and hybridization states using Inline VeraFlex (XPS) and Elipson (Raman) metrology. The study identifies key process–structure correlations and strategies to enable reliable graphene–dielectric integration in advanced interconnect technologies.

RESULTS AND DISCUSSION

Graphene films were deposited on silicon substrates coated with a 25 nm Cu layer. Patterned samples were fabricated by selectively depositing graphene on Cu surfaces with no deposition on the adjacent dielectric regions. To evaluate the effect of dielectric films deposition on graphene, dielectric layers were subsequently deposited using plasma-assisted (DL1) and thermal (DL2) processes. Characterization was performed using VeraFlex, an inline XPS/XRF metrology system, and Elipson, an inline Raman spectroscopy platform, both developed by Nova Ltd. These tools enable wafer-scale, non-destructive characterization of composition, thickness, crystallinity, and strain directly within high-volume manufacturing (HVM) environments.

Raman spectroscopy of graphene is a well-established topic in scientific research. Sensitivity for many graphene attributes, like layer-number identification, structural quality, defects and more, makes Raman spectroscopy a major characterization tool for process development [ref 3-4]. Structural quality is manifested strongly in all the Raman peaks-of-interest. For example, the 2D band is sharp and strong in perfectly ordered graphene, while in damaged, or polycrystalline graphene, the band is broader and with lower amplitude. More spectral attributes that are affected by structural damage to graphene layers are the G peak vibrational energy and the D band shape and amplitude. Plasma deposition, which uses ions bombardment of the surface, can lead to significant damage to the substrate layers [ref 5]. Here, we examine the extent of this effect in multiple scenarios.

In one experiment, Raman spectra measurement of graphene, with and without presence of the two different types of dielectric deposition processes i.e., thermal and plasma process. The spectra reveals that the thermal DL2 layer deposited directly over the Graphene layer had minimal impact on the Graphene's spectrum, while a plasma DL1 layer changed it significantly. The significant change in graphene quality by plasma-based deposition process is evident from the drop of the 2D peak intensity, indicating reduction in the quality of the graphene film as compared to pristine graphene and graphene_DL2 sample shown in FIGURE 1. Second experiment on patterned wafers

highlighted that the graphene layer quality deteriorates when exposed to the plasma deposition even when protected by one or few thermal layers. This damage is reflected in the reduction of the 2D peak amplitude, the peak broadening and many other spectral features. However, as the number of thermal layers increases, the extent of this damage diminishes, as illustrated in FIGURE 2. These findings suggest that a thermal layer can offer partial protection against plasma-induced damage, with the level of protection depending on its thickness.

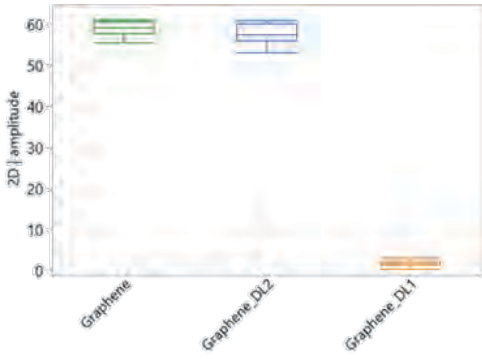


FIGURE 1. A pronounced reduction in the 2D peak intensity, suggesting damage to the graphene structure is seen for the plasma on Graphene case. The elevated Raman background signal for this case is attributed to photoluminescence, originating from the DL1 layer.

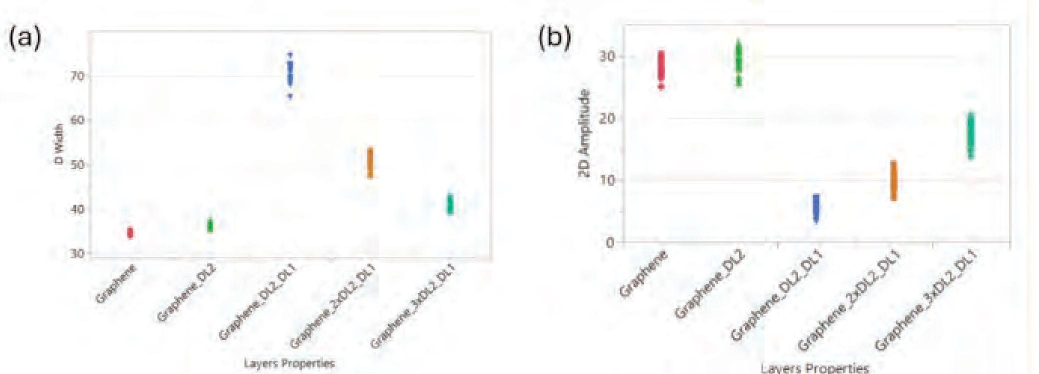
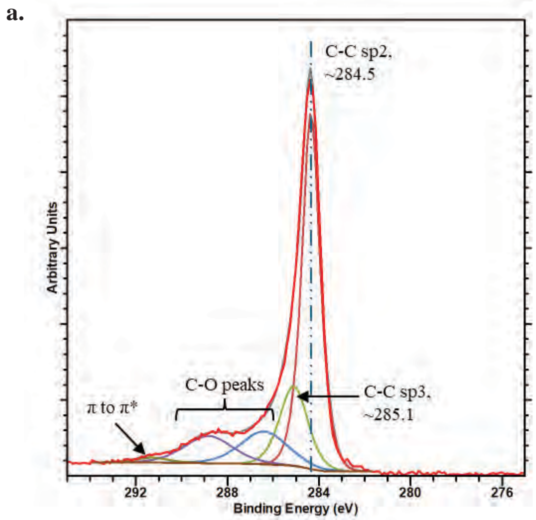


FIGURE 2. D peak's width (a), 2D peak's amplitude (b) and other (not plotted) spectral attributes across the wafer indicate that the thermal dielectric layers introduce an increasing level of protection for the graphene against the plasma deposition process, with DL2 thickness. However, for the three right-most samples, the thermal DL2 layers' thickness were not enough to completely prevent the plasma damage to graphene film.

Complementary XPS confirmed uniform deposition of both DL1 and DL2 and provided quantitative assessment of both layer thickness and bonding configuration. The sp^2/sp^3 ratio derived from C1s spectra indicated that optimized DL2 conditions preserve a higher fraction of sp^2 bonding, suggesting minimal lattice disruption. FIGURE 3 (a) shows C1s core-level spectrum of undamaged graphene and FIGURE 3 (b) shows the quantitative comparison of sp^2 and sp^3 components for various Cu/graphene/dielectric stacks. The sp^2/sp^3 ratio decreases with plasma or DL1 processing and improves with optimized thermal (DL2) layers. DL2 thickness variability across wafers for different Cu/graphene/dielectric stacks is shown in FIGURE 4. Each data point represents a measurement site on the wafer, showing consistent within-wafer uniformity and distinct mean thickness values for each process condition.

Overall, the combined XPS and Raman results demonstrate that applying an appropriately thick DL2 (thermal) layer prior to plasma based process effectively maintains graphene quality. This integrated inline approach potentially enables real-time SPC, supporting scalable, repeatable integration of graphene-based capping layers in HVM for advanced interconnect technologies.

a.



b.

Stack	*sp* 2	*sp* 3	*sp* 2/*sp* 3
Cu/graphene	51.8	15.9	3.26
Cu/graphene/DL1	24.2	25.8	0.94
Cu/graphene/DL2	50.0	27.8	1.80
Cu/graphene/DL2/DL1	54.9	33.0	1.66
Cu/graphene/2xDL2/DL1	54.9	35.6	1.54
Cu/graphene/3xDL2/DL1	51.3	38.7	1.33

FIGURE 3. (a) C1s core-level spectrum of undamaged graphene. The strong sp^2–C peak and minimal sp^3 or oxide-related contributions confirm that the film retains high-quality graphitic bonding before plasma processing. (b) Quantitative comparison of sp^2 and sp^3 components for various Cu/graphene stacks. The sp^2/sp^3 ratio decreases with plasma or DL1 processing and improves with optimized thermal (DL2) layers.

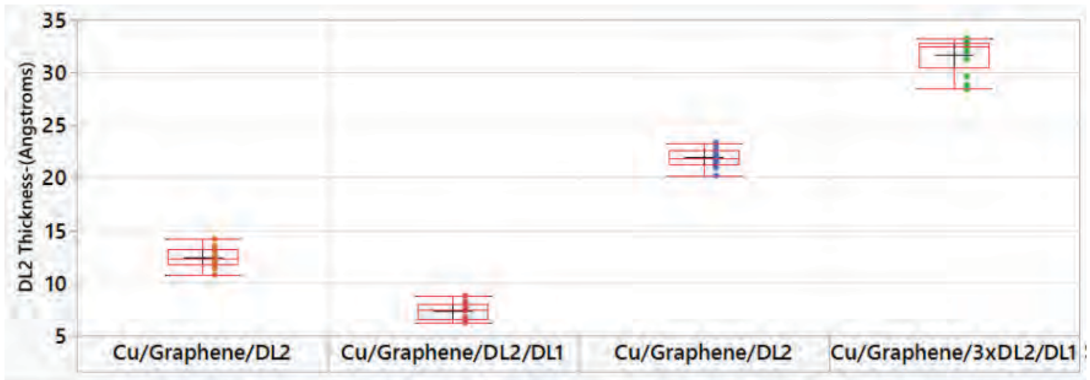


Figure 4. DL2 thickness variability across wafers for different Cu/graphene stacks. Each data point represents a measurement site on the wafer, showing consistent within-wafer uniformity and distinct mean thickness values for each process condition.

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KEYWORDS

Graphene, Inline XPS spectroscopy, Raman spectroscopy, Plasma damage, Di-electric films

Advancements In XPS Depth Profiling Using Femtosecond Laser Ablation (fs-LA) For Thin Film And Oxide Surfaces

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XPS depth profiling is a widely employed analytical technique to determine the chemical composition of thin films, coatings and multi-layered structures, due to its ease of quantification, good sensitivity and chemical state information. Since the introduction of XPS as a surface analytical technique more than 50 years ago, depth profiles have been performed using ion beam sputtering. However, many organic and inorganic materials suffer from ion beam damage, resulting in incorrect chemical compositions to be recorded during the depth profile. This problem has been resolved for most polymers by using argon gas cluster ion beams (GCIBs), but the use of GCIBs does not solve the issue for inorganics. We have introduced a novel XPS system, Hypulse, that employs a femtosecond laser rather than an ion beam for XPS depth profiling purposes. This novel technique has shown the capability of eradicating chemical damage during XPS depth profiling for all initial inorganic, compound semiconductor and organic materials examined. The technique is also capable of profiling to much greater depths (several 10s microns) and is much faster than traditional ion beam sputter depth profiling. fs-LA XPS depth profile results will be shown for selected thin films, coatings, multilayers and oxidized surfaces and the outlook for this new technique discussed.

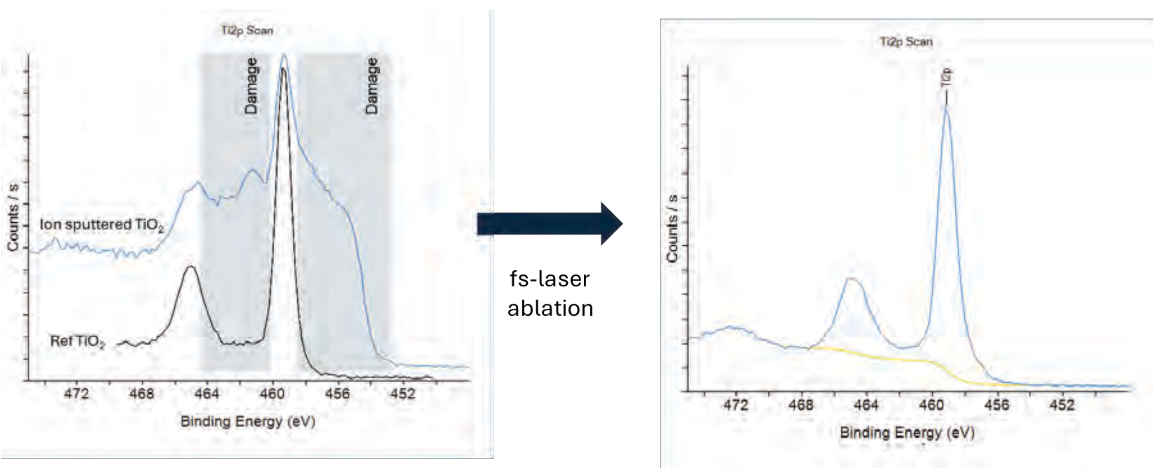

Figure 1 A TiO2 surface was exposed to 500eV monoatomic Ar Ion beam for 200 seconds, creating a damaged region of TiOx<2. Exposure to fs-Laser pulses removes the damaged material and retains the surface TiO2 stoichiometry.

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Keywords

Surface Analysis, Thin Films, XPS, Depth Profiles, Metal Oxides, Laser Ablation

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Advances in Atom Probe Tomography Analysis

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INTRODUCTION

In atom probe tomography (APT) [1], the path to knowledge can be divided into three main operations: specimen preparation, data acquisition, and data analysis. Over the past few decades, significant advancements in both hardware and software have reduced the time required for these operations from days or weeks to mere minutes, depending on the maturity of the application and the frequency of performing the same analysis. The obstacles on the path to knowledge vary greatly depending on the time distribution in each major step. For new applications, such as a finFET in a modern microelectronics device, specimen preparation may initially dominate the timeline. However, with each iteration, the time required for specimen preparation can be significantly reduced. Subsequently, optimizing data acquisition conditions to maximize success rates and data quality can become the primary focus. Once high-quality data is collected, data analysis can then become the most time-consuming and expertise-driven step.

SIMULTANEOUS VOLTAGE & LASER PULSING

Voltage and laser pulsing (VpL) in atom probe tomography has been proposed as a means to improve sensitivity and compositional accuracy [2,3]. In this pulsing scheme, background reduction [2,4] and mass spectral peak sharpening [3] may be achieved, especially for materials with poor thermal diffusivity as shown in Figure 1. Recently, background reduction was achieved for a variety of materials, including aluminum (~8X), stainless steel (~4X), silicon (~15X), and silicon dioxide (~2X) [4]. The amount of background reduction and the ability to reduce the peak tails is strongly dependent on the voltage pulse shape, duration, and amplitude. Efforts are ongoing to optimize the pulse shape as shown in Figure 2.

MASS SPECTRAL ANALYSIS

Identifying peak regions in the mass spectrum (commonly called “ranging”) and conducting three-dimensional data analysis are predominantly manual processes. The identification and ranging of mass-spectral peaks significantly influence the results of all subsequent analyses. Previous round robin experiments have demonstrated that subjective user bias in mass spectral analysis can greatly affect the results, limiting accuracy and precision [5]. Ranging and phase identification are often iterative processes, requiring adjustments and revisions to previous steps. CAMECA is collaborating with research groups worldwide to develop new tools for peak identification, ranging, and volume segmentation to create a faster and more reproducible workflow using the Atom Probe Suite™ 6.3.3 platform that includes spatial ranging and an interactive extensions platform that can incorporate third-party algorithms.

This workflow, summarized in Figure 3, includes automated ranging using a supervised machine learning method that recognizes peaks and determines their boundaries as shown in Figure 4. The next step involves leveraging natural isotopic abundance patterns to identify elemental and molecular peaks through model training [6]. Confidence scores are reported to allow manual review of peaks of uncertain identity. Finally, multivariate statistical analysis methods are used to identify unique spectral components throughout the volume, leading to volume-segmented ranging and compositional analysis in unique phases identified by these components [7,8]. In the last step, automated ranging can be re-applied to each of the independent identified phases which typically increases confidence in peak assignments due to fewer overlaps in the independent phases and less background noise.

The AP Suite 6.3.3 spatial ranging and extensions platform has allowed independent algorithm development to automatically range, identify peaks, and identify spectrally unique regions of the 3D data. Each of these steps takes just seconds and removes user bias from peak ranging and identification leading to at least more precision and likely

more accuracy in data analysis. The machine learning workflow will allow retraining based on new datasets and the training data will be available for transparency.

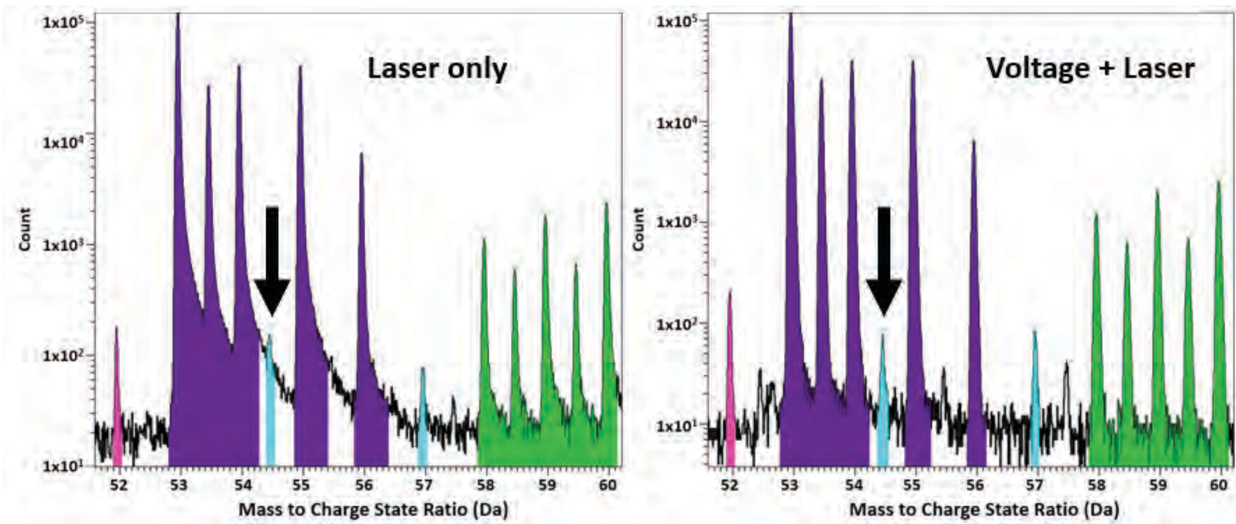

FIGURE 1. Comparison of the ZrO peaks with similar ion counts in (a) laser only mode and (b) simultaneous voltage pulse. Background levels and peak tails were reduced providing an increase in signal to noise of trace peaks.

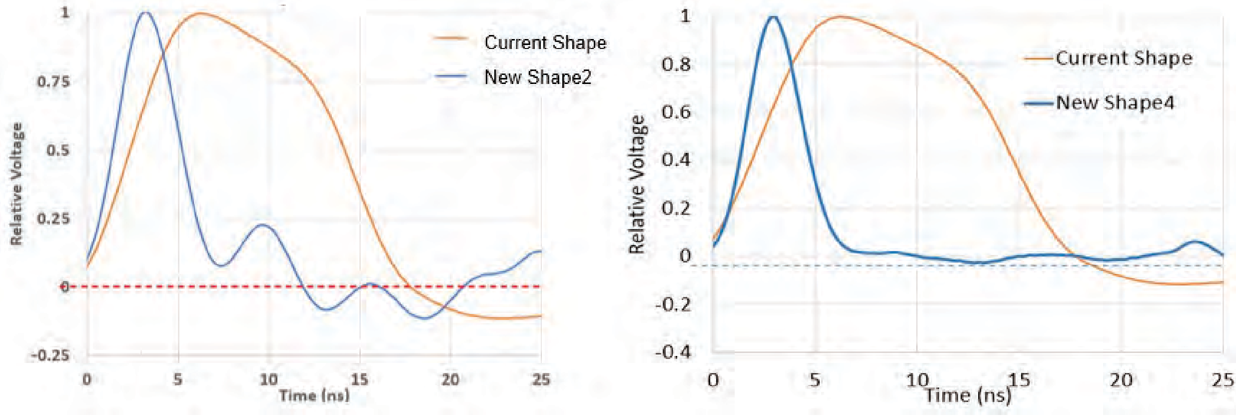

FIGURE 2. The current voltage pulse shape (orange) compared to two iterations of new pulse shapes (blue) as efforts were taken to narrow the pulse duration and minimize undesired post-pulse voltage variations.

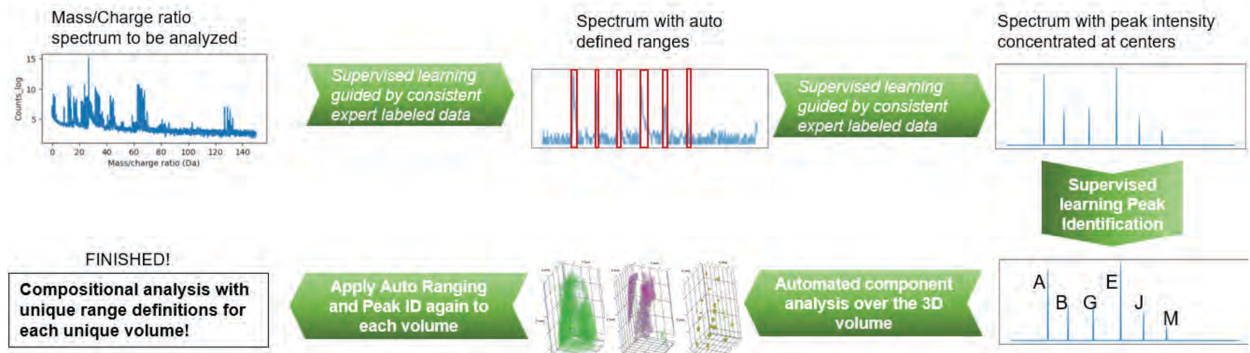

FIGURE 3. Automated workflow starting from the full mass spectrum, automated ranging and peak ID for the whole dataset. Automated spectral component analysis using MVSA followed by final ranging and peak identification for each identified volume for precise and rapid compositional analysis

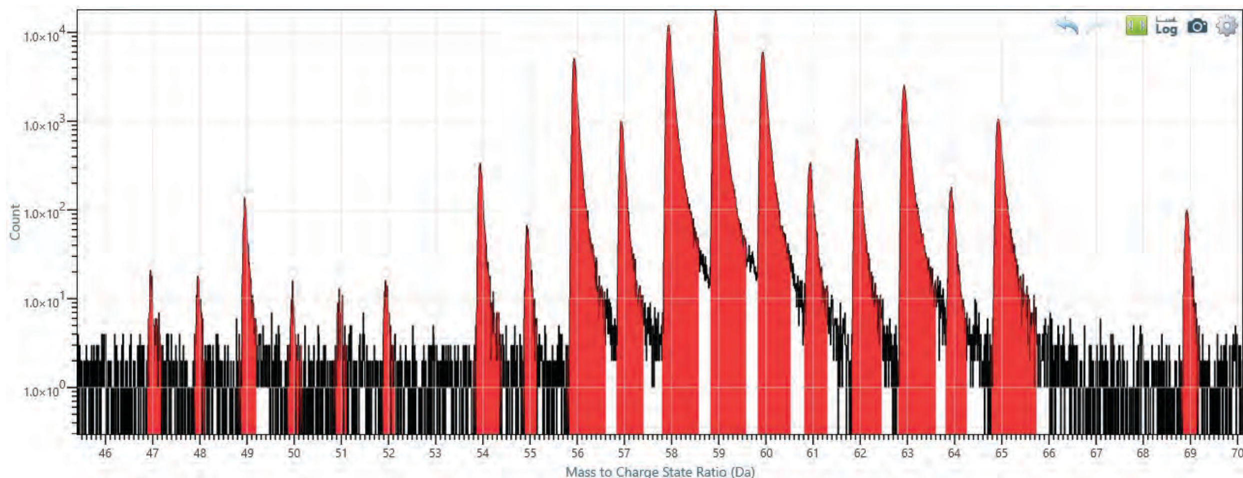

FIGURE 4. Automated peak ranging based on supervised machine learning from 'expert' ranged datasets.

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KEY WORDS

Atom probe, mass spectrum, data analysis, machine learning,

Advanced Packaging Process Control With Micro X-ray Fluorescence

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INTRODUCTION

High-bandwidth memory (HBM) drives multiple technology advancements and is a critical enabler for AI devices such as high-end GPUs, yet it is one of the most challenging modules to manufacture. Advanced packaging for HBM4 and future technology nodes require aggressive micro bump pitch scaling, down to below 10µm diameter to achieve higher interconnect density, enabling increased bandwidth, taller memory stacks, and improved power efficiency [2].

This scaling introduces significant complexity in fine-pitch solder deposition, underfill control, and warpage management, while demanding advanced inspection and metrology solutions to ensure reliability and yield at ultra-dense interconnect levels. One of the key metrology requirements for advanced packaging is high precision measurement of silver content in SnAg micro bumps and the thickness of critical metal layers such as nickel, copper, and gold.

Micro X-ray fluorescence (µXRF) has become an incumbent inline metrology technique due to its ability to measure individual bumps and small metal pads with high precision and acceptable throughput. However, the aggressive pitch shrink in next-generation packaging nodes necessitates metrology solutions capable of measuring smaller bumps and thinner metal layers without compromising accuracy or speed.

TECHNOLOGY

To enable the "single bump metrology" with µXRF, the equipment design (see Figure 1) must address several important challenges: Minimize the spot size to match the bumps size decrease while minimizing the X-ray flux outside of the bump. The vertical design is therefore implemented to minimize the spot projection and additionally minimize the sensitivity to height variation. The decrease in x-ray intensity due to decrease in material volume with the bump size and thickness reduction is addressed by careful excitation and analyte line selection. For example, for bump sizes above 15µm, high energy Ag Kα and Sn Kα lines are used to extract solder bump composition and solder height. A tungsten (W) X-ray source is utilized to ensure the high bremsstrahlung intensity that excites the above lines. However, one X-ray source isn't optimal for the whole range of packaging applications. To enable the best excitation conditions and, therefore, the best performance, a dual µXRF configuration is utilized: one µXRF channel with a W source for Sn and Ag and another one with a molybdenum (Mo) source, efficient for gold, copper and nickel excitation.

An array of Silicon Drift Detector (SDD) detectors and state-of-the-art Digital Pulse Processor (DPP) units are used with each source to enable high collection angle and efficient photon counting. Specially designed SDD detectors must are used to provide high quantum efficiency for high energies such as Ag and Sn Kα.

In addition, production monitoring on 300 mm wafers requires very accurate navigation. Micron level misalignment of the x-ray beam with respect to the bump or the pad results in significant degradation in dynamic precision as well as accuracy penalty. As an example, for a 3 µm mis-positioning of a 10 µm (FWHM) spot on a Ø15 µm bump the Poisson-related error from photon counting uncertainty is 0.3% relative standard deviation (RSD), but the predicted dynamic contribution to the error budget due to mis-positioning of the X-ray spot is 0.82%, thus dominating the error budget. Furthermore, the mis-positioning contributes 11% inaccuracy in thickness or composition measurement. Simulation shows that the navigation error must be < 0.5 µm to enable satisfactory process control.

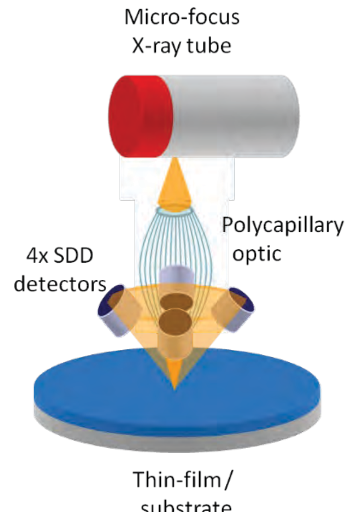

FIGURE 1: µXRF channel schematic for the advanced wafer level packaging process control

Analytical methods include peak deconvolution to remove background (example on the figure 2a case of the solder bump application) as well separate overlapped peaks, such as Cu Kα from Ni Kβ (figure 2b case of the metallization application).

Empirical regression is typically used to extract the bump composition and height. The use of the fundamental parameters algorithms (FP) has limited accuracy in the case due to the non-planar (and irregular) bumps' shape. An example of the regression equation is:

$$\%Ag = A_0 + A_1 \cdot \frac{I_{AgK\alpha}}{(I_{AgK\alpha} + I_{Sn\alpha})} + A_2 \cdot I_{SnK\alpha}$$

The last term accounts for the bump height variation. The FP approach is used for the metallization applications, because it handles the double and triple film stacks well.

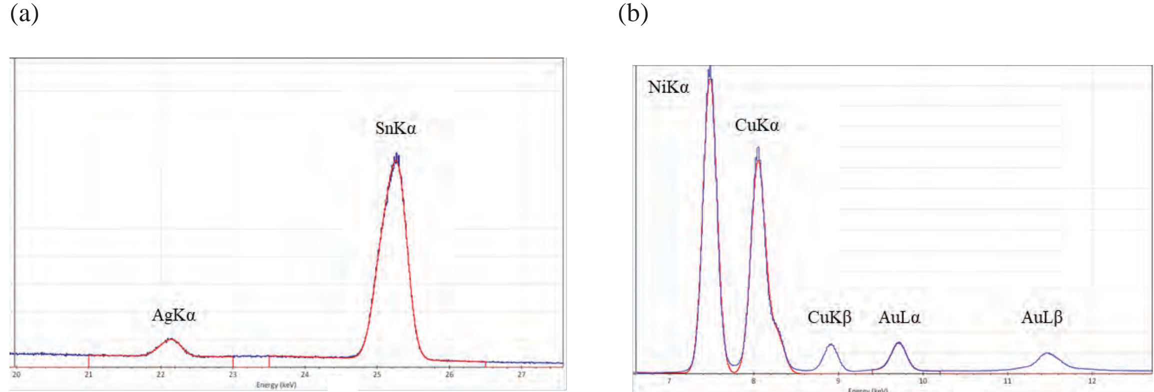

FIGURE 2: Representative X-ray spectra (blue) and fits (red). (a) Ag/Sn solder bump and (b) Cu/Ni/Au metallization

RESULTS AND DISCUSSION

Typical XRF spectra from the solder bump and Cu/Ni/Au metallization layers are shown in figure 2. The low intensity Ag Kα defines the equipment performance in terms of acquisition time, throughout and precision. The scaling of the bump size and the reduction of silver content further decrease the Ag Kα intensity. Combined with the

lower peak-to-background ratio, this is the major challenge in solder bumps metrology. Additional solutions are being considered for bumps below Ø10µm, such as usage of the low energy Ag Lα line, but this discussion is beyond the scope of this paper.

The metallization applications present another type of challenge due to the very high fluxes from the micron thick films. These fluxes can cause the system saturation requiring use of filter to control the flux and thus limiting the performance. Modern metrology tools, such as the Bruker Sirius-FW G2 address this issue with the latest high-performance DPP counting electronics.

The performance requirements, in terms of precision, are dictated by the needs of the process tolerances and are typically 3×RSD < 1% for %Ag and bump height (equivalent to the ±10% process tolerance) and even 3*RSD<0.5% for the metals such as Ni or Au (equivalent to the ±5% process tolerance). The performance requirement for longer-term stability is typically similar to dynamic repeatability and requires the use of automated drift correction algorithms to avoid frequent application re-calibration.

A throughput of at least 10-15 wafers per hour for typical fab sampling patterns is required to maintain the reasonable cost of ownership (CoO).

CONCLUSION

The key metrology challenges of the advanced wafer level packaging applications such as tight control of thickness and composition on ever shrinking solder bumps and back bumps are addressed by the specially designed µXRF metrology channels and tools. The industry roadmap for advanced packaging applications including HBM dictates in turn an aggressive roadmap for metrology equipment development to maintain the required performance in terms of process control and CoO. Technology inflections are expected which will require continued innovation for future process control development.

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ACKNOWLEGEMENTS

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KEYWORDS

Advanced Packaging, High Bandwidth Memory (HBM), Micro bumps, X-ray fluorescence (XRF)

Analytical X-Ray Solutions For Thin Film And Wafer Analysis

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INTRODUCTION

X-ray diffraction methods are a very important non-destructive tool in analysis of thin films and bulk crystals alike. The ability to very accurately measure lattice d-spacings in a variety of geometries provides structural information, not only about lattice parameters, phase identification and crystal orientations, but also about different metrics of crystal and film quality. For thin films, obtainable parameters include composition and relaxation, micro-strain, stress, mosaicity, lateral and vertical correlation lengths and crystallite size, microscopic tilts and twists, dislocation density, as well as layer thickness, roughness / diffuseness, and density. For bulk crystals, X-ray diffraction can be used to determine crystal quality via rocking curves, and crystal orientation, for example the offcut magnitude and direction.

In this work we present the capabilities of a few different laboratory diffractometers. We demonstrate several ways in which Reciprocal Space Mapping (RSM) can be performed, such as coplanar Ultrafast RSM using area detector or non-coplanar RSMs from fiber textured films. We compare several in-plane geometries on Empyrean and on X'Pert3 MRD (XL). We demonstrate the benefits of using a rotating slit in combination with an X-ray lens for consistent sample illumination at any Chi tilts, improving the quality of texture, non-coplanar RSM, and in-plane measurements.

Next, we focus on the ability to make the analysis of X-ray reflectivity less model-dependent, by using our patented free-form analysis method. This can be especially in research process in cases when the layer model is difficult to build - either because of oxidation, interlayer formation, density gradients, or any other processes that would need to be explicitly known in advance to be included in a model.

Finally, we present work on the rapid orientation determination of bulk crystals (wafers).

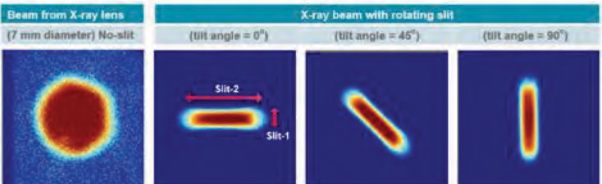

FIGURE 1. Effect of rotating slit on direct beam shape.

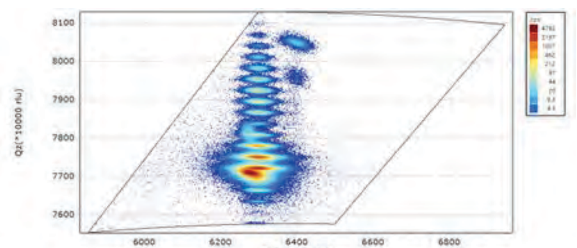

FIGURE 2. Fast RSM of GaN HEMT structure.

KEYWORDS

X-Ray Diffraction, X-Ray Reflectivity, Reciprocal Space Maps, High Resolution

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A Modular, Open-Source In Situ Ellipsometer for ALD: Low-Cost Instrumentation and a Complete Educational Build Guide

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INTRODUCTION

In situ spectroscopic ellipsometry performs optical measurements on a sample while a process such as thin film deposition is underway. It is widely used for real time monitoring of atomic layer deposition (ALD) because it provides reliable, non destructive measurements of film thickness and optical constants. A rotating compensator ellipsometer (RCE) modulates the polarization of light by rotating a quarter wave plate, allowing the extraction of ellipsometric parameters ψ and Δ from intensity harmonics.

Commercial RCE instruments cost tens of thousands of dollars and are not easily adapted to custom vacuum chambers. Our long term objective is to document and disseminate an open source, step by step protocol for building an in situ ellipsometer at a fraction of that cost. To this end we compiled a detailed parts list with supplier links (see Ellipsometer Parts List.xlsx) and will release CAD models and microcontroller code. The affordability of the design stems from using off the shelf optical components, a low cost hollow shaft stepper motor, and additive manufactured adapters.

DESIGN OF THE ROTATING COMPENSATOR ELLIPSOMETER

Our goal was to build a compact, single-wavelength RCE that could be attached to an ALD chamber and operate inside a vacuum. The optical train follows the conventional PSCRA configuration—polarizer, sample, compensator and rotating analyzer—to preserve both amplitude and phase information of the reflected beam. The intensity transmitted by such an instrument has the form

$$I = I_0(2 + S_1 - 2S_3 \sin\ 2C + S_1 \cos\ 4C + S_2 \sin\ 4C),$$

where I_0 is a scaling constant, S_1, S_2, S_3 are Stokes parameters of the reflected beam and $C(t) = \omega_c t$ is the compensator angle. This relationship is equivalent to Eq. 4.32 in Fujiwara's text [1] and shows that harmonics of $2\omega_c$ and $4\omega_c$ encode the ellipsometric angles ψ and Δ.

We modeled the intensity at the detector using the Jones-matrix formalism. Assuming the polarizer is fixed at 45° and the analyzer at 0°, and using a quarter-wave plate ($\delta = 90°$), the intensity contains harmonics at the fundamental, second and fourth multiples of the compensator frequency. This allows ψ and Δ to be extracted from Fourier coefficients. For our test structures we considered amorphous SiO_2 and Al_2O_3 films with refractive indices described by a Cauchy model, $n(\lambda) = A + B/\lambda^2$, using parameters A and B measured for each sample.

CUSTOM MOTOR MOUNT AND OPTICAL ASSEMBLY

To integrate the rotating compensator into the vacuum chamber we developed a hollow-shaft stepper motor mount using 3D-printed components. One piece couples the motor to standard 30 mm cage-rod optics; another couples the motor shaft to the quarter-wave plate (Figure 1a). The completed assembly, including polarizer, motor-driven compensator, sample chamber, analyzer and detector arms, is shown in Figure 1b. A microcontroller drives the stepper motor at ≈1400 rpm and acquires photodiode voltage while maintaining vacuum compatibility.

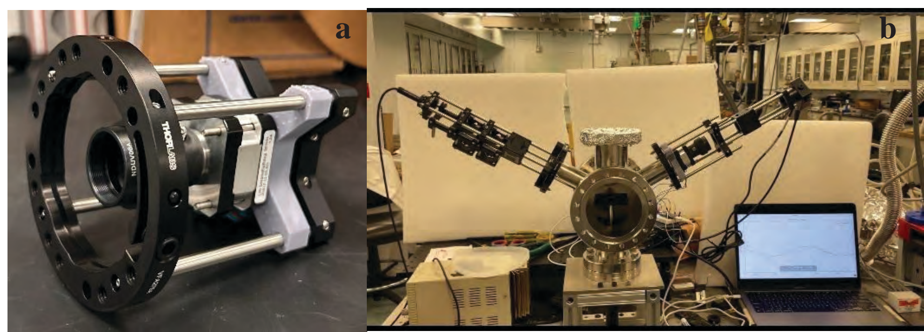

FIGURE 1. Hollow shaft motor mount set up (a). A photograph of the installed ellipsometer on an ALD chamber (b).

Standard cage-rod mounts do not share the same bolt pattern as the hollow-shaft motor; our custom adapter provides the necessary offset and mounting holes. Because the adapters contain fine threads, they were printed on a high-resolution resin printer (Elegoo Saturn 2 with water-washable resin). Although the parts could be machined in a shop, additive manufacturing allowed us to produce accurate threads rapidly under tight deadlines. A Mean Well NDR-240-48 power supply (48 V, 240 W) powers both the motor driver and control electronics.

The instrument was tested in a single-thickness configuration using a 520 nm laser source. Data acquisition and fitting were performed using a Python script. Measured voltages were fitted to the model using non-linear least squares.

THICKNESS MEASUREMENTS

Table 1 summarizes the results obtained for two calibration samples. Sample A consisted of a 35.34 nm thermal SiO_2 film with Cauchy parameters $A = 1.447$and $B = 4.06 \times 10^{-3}$ μm^2; Sample B was a 59.37 nm Al_2O_3 film with $A = 1.627$and $B = 6.67 \times 10^{-3}$ μm^2 (see Figure 4, e6dc7854-828b-4af2-907e-fa12cb847c63.png). The fitted parameters from our RCE show excellent agreement with the nominal thicknesses. For SiO_2 we obtained $d_{fit} =$ 35.45 nmwith $R^2 = 0.982$; for Al_2O_3 we obtained $d_{fit} = 59.79$ nm with $R^2 = 0.995$. The fitted ellipsometric angles were $\psi_{SiO_2} \approx 22.6°$ and $\Delta_{SiO_2} \approx 137.8°$, and $\psi_{Al_2O_3} \approx 28.5°$ and $\Delta_{Al_2O_3} \approx 114.0°$. These values are consistent with the expected optical response for films of similar thickness deposited on silicon substrates.

TABLE 1. Results of thickness measurements using the single wavelength rotating compensator ellipsometer. Nominal thicknesses and Cauchy parameters were provided by sample suppliers; fitted values were obtained by least squares fitting the measured voltage data.

Material	Nominal Thickness (nm)	Cauchy Parameters (A, B)	Fitted Thickness (nm)	Fit Quality (R^2)
SiO_2	35.34	A = 1.447, B = 0.00406 µm²	**35.45**	0.9817
Al_2O_3	59.37	A = 1.627, B = 0.00667 µm²	**59.79**	0.995

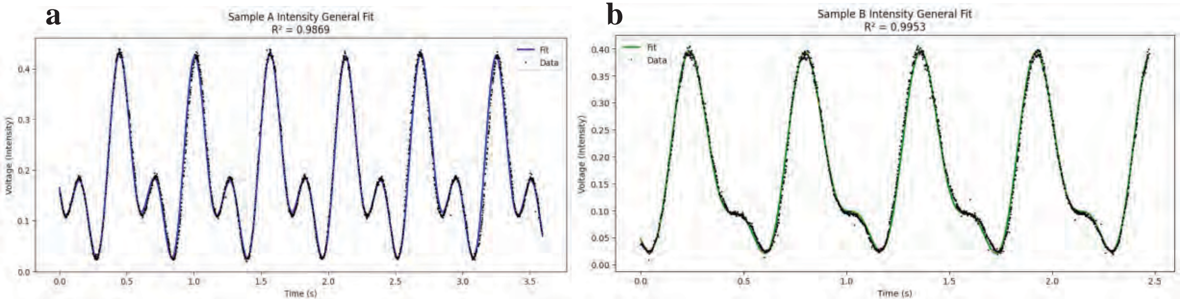

FIGURE 2. Plots of experimental and fitted voltage intensity values for SiO_2 (a) and Al_2O_3 (b).

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KEYWORDS

Spectroscopic ellipsometry; rotating compensator; atomic layer deposition; hollow shaft motor; 3D printing; thin film thickness.

DeepCore-X: Enabling Non-Destructive, High-Throughput Characterization of Buried Interfaces in Semiconductor Devices

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INTRODUCTION

Buried interfaces in multilayer semiconductor devices—such as MOSFETs, solar cells, and advanced memory architectures—play a pivotal role in determining device performance, reliability, and longevity. Traditional surface-sensitive techniques like X-ray photoelectron spectroscopy (XPS) are limited in their ability to probe these interfaces without destructive sample preparation. Hard X-ray photoelectron spectroscopy (HAXPES), with its increased information depth, has emerged as a powerful solution for non-destructive analysis of buried layers.

ENABLING DEEP HAXPES TECHNOLOGY

We present DeepCore-X, a next-generation laboratory instrument that integrates soft and hard X-ray photoelectron spectroscopy (XPS & HAXPES) in a single solution, delivering synchrotron-like performance for semiconductor research directly in the lab. At the heart of DeepCore-X is the Excillum Ga Kα MetalJet source (9.25 keV), offering a 3.5× intensity boost with 1000 W continuous operation. Together with a monochromator we achieve a 50 µm spot size, enabling deep, high-resolution probing of buried interfaces up to 50 nm without sputtering (1).

Coupled with the EW4000 hemispherical analyzer—featuring 60° angular acceptance, 200 mm radius, and image-corrected wide-angle detection—DeepCore-X achieves high-throughput, high-fidelity measurements across complex device stacks. The system supports automated sample handling, multi-point acquisition, and operando bias measurements, making it ideal for evaluating band bending (2), trap states, and chemical shifts in real-world device environments.

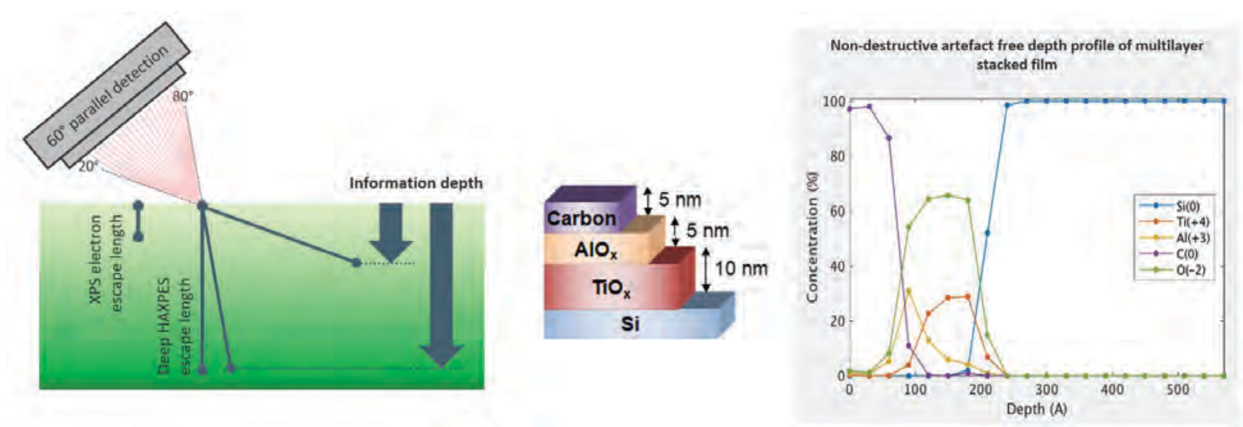

FIGURE 1. Non-destructive depth profile obtained from angular-resolved Deep HAXPES measurements at 9.25 keV, showing elemental concentrations as a function of depth. The results align well with the expected composition of the sample grown. Sample by NTT-AT. Data courtesy: Dr S. Toyoda, Scienta Omicron

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Key Applications in Semiconductor Research

- Non-destructive depth profiling: Angular-resolved HAXPES provides accurate layer thickness and composition without sample damage.
- Multilayer MOSFET gate stacks: Deep HAXPES reveals chemical states of buried oxides (e.g., In_2O_3, ZrO_2), inaccessible to conventional XPS.
- Operando bias studies: Enables direct observation of band structure variation under applied voltage, critical for understanding charge distribution and interface behavior.
- Thin film and passivation layer analysis: Detects deeply buried layers and interfaces, supporting advanced materials development.

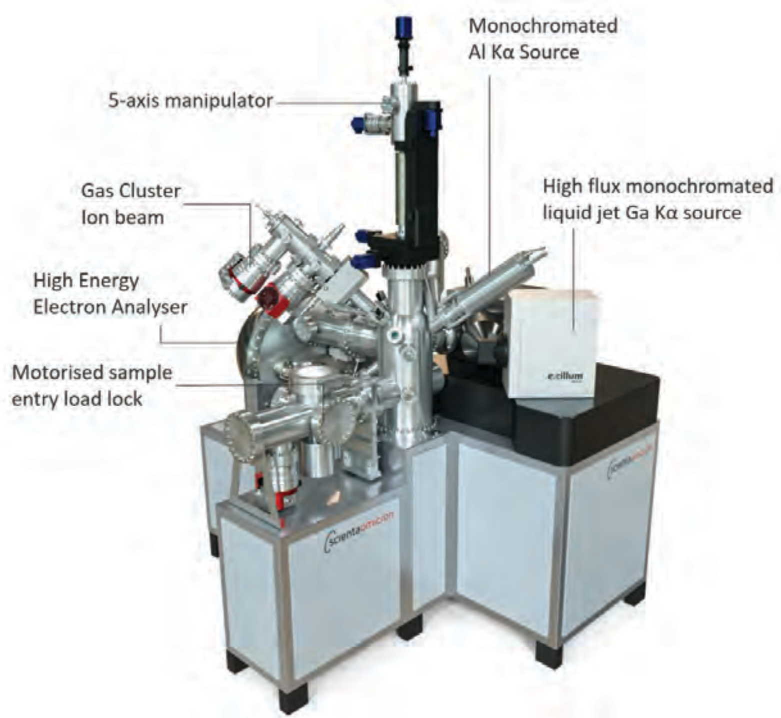

FIGURE 2. DeepCore-X redefines laboratory-based HAXPES by combining deep probing capability, automated high-throughput workflows, and operando measurement support. Its modular design and robust performance make it an indispensable tool for semiconductor interface research, bridging the gap between surface analysis and full device stack characterization – without the need for synchrotron access.

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KEYWORDS

HAXPES, XPS, thin films, buried interfaces, defects, non-destructive characterization

Improving Efficiency of Predictive Models Using Mixed Machine Learning Techniques on OCD Spectra

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INTRODUCTION

Spectroscopic Ellipsometry based Optical Critical Dimension (OCD) measurement technique is widely used during fabrication of nanoscale transistors. While OCD is primarily used to measure a handful of critical dimensions (CD) of the transistors at a given segment of its fabrication, it holds significantly more information on the CDs and material characteristics of the entire transistor stack that can be utilized for predictive modeling using machine learning approaches. Here, we demonstrate prediction of a CD parameter measured after a manufacturing process step using the information contained in the OCD spectra measured prior to that process step. Such predictive models capture the incoming variation to the CD metric of interest and allow for the process step to tighten that variation. A pure Rotating Coupled Wave Analysis (RCWA) based OCD model is untenable in such predictive model building owing to the lack of detailed information available regarding the transistor stack at the pre-process step. While a pure spectral machine learning (ML) approach may be successful in yielding a stable predictive model, it requires extensive training to become stable and has very high likelihood of breaking with smallest changes in the stack. In this work, we demonstrate the efficiency of a mixed RCWA based OCD model and ML technique for building such post-process CD prediction model using the pre-process spectra. This mixed ML technique requires significantly less resources to train, demonstrates matched or better performance than pure spectral ML models, are much cheaper to recalibrate upon changes of processes, and therefore, are more conducive for a high-volume manufacturing environment.

RESULTS AND DISCUSSION

In GAA technologies, thickness of Si nanowire channels (TSi) is one of the key transistor CD parameters to have fine control over. Typically, TSi is measured using OCD after the sacrificial SiGe is etched out completely in a process step referred to Nanowire Release (NWRLS). As the GAA transistor superlattice goes through several segments of processing, the thickness of the Si channels, as deposited in the superlattice, undergoes changes due to Ge diffusion and other impacts. Consequently, much of the TSi variation post NWRLS can be predicted even before the sacrificial SiGe is removed. In this work, the OCD spectra was measured prior to the NWRLS step to build a predictive model for TSi measured after the NWRLS step. Like majority of the OCD applications, this exercise was confined to a pre-defined process flow.

For building a TSi (measured post NWRLS) prediction model from the pre-NWRLS spectra, two distinct methods were tested: a) pure spectral ML based technique and b) mixed RCWA based OCD model and ML based technique. In the pure spectral ML based technique, 5 most sensitive Mueller Matrix (MM) spectral channels were used. The principal components extracted from these MM channels are composites of all the MM elements. Different models were tested with number of principal components ranging from 25 to 55. The ML training attained a steady state

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when trained with at least 39 principal components and that constituted the final model. The training of the ML model used spectra and TSi data post NWRLS from all the lots in a given timeframe and predicted the results for all the lots beyond that time window. It used spectra from all the lots and wafers from the training timeframe and trained on the spectra from 11 dies per wafer, to build a prediction of TSi for the lots measured in subsequent times. The goodness of the model was assessed by the steadiness of the RMSE in TSi prediction every week subsequently. The final spectral ML model used 50 such lots to train and reached a steady state RMSE for TSi prediction of ~0.07 for every week subsequently for 10 weeks.

On the other hand, the mixed RCWA based OCD model and ML modeling approach used much less resources. It started with a RCWA based OCD model including a stack of Ge diffusion layer alongside the TSi. This technique used the same MM channels as the pure spectral ML approach and arrived at a good global fit for the RCWA based OCD component of the model. Thereafter, the model employed ML on the combination of the measured spectra and the RCWA OCD model output, to build a good predictor for TSi measured post NWRLS. Owing to confined ranges of variation of the key parameters enabled by the RCWA OCD model, this mixed ML approach converges with much less resources and in this case, it needed only 19 lots worth of spectra and reference to stabilize, in contrast to the 50 lot resources needed for the pure spectral ML method. Furthermore, the RMSE of the predicted TSi at NWRLS stabilized faster to an approximately same number of ~0.07, for the next 10 weeks post training. Consequently, this mixed ML approach is a more sustainable and cheaper solution for the high-volume manufacturing environment.

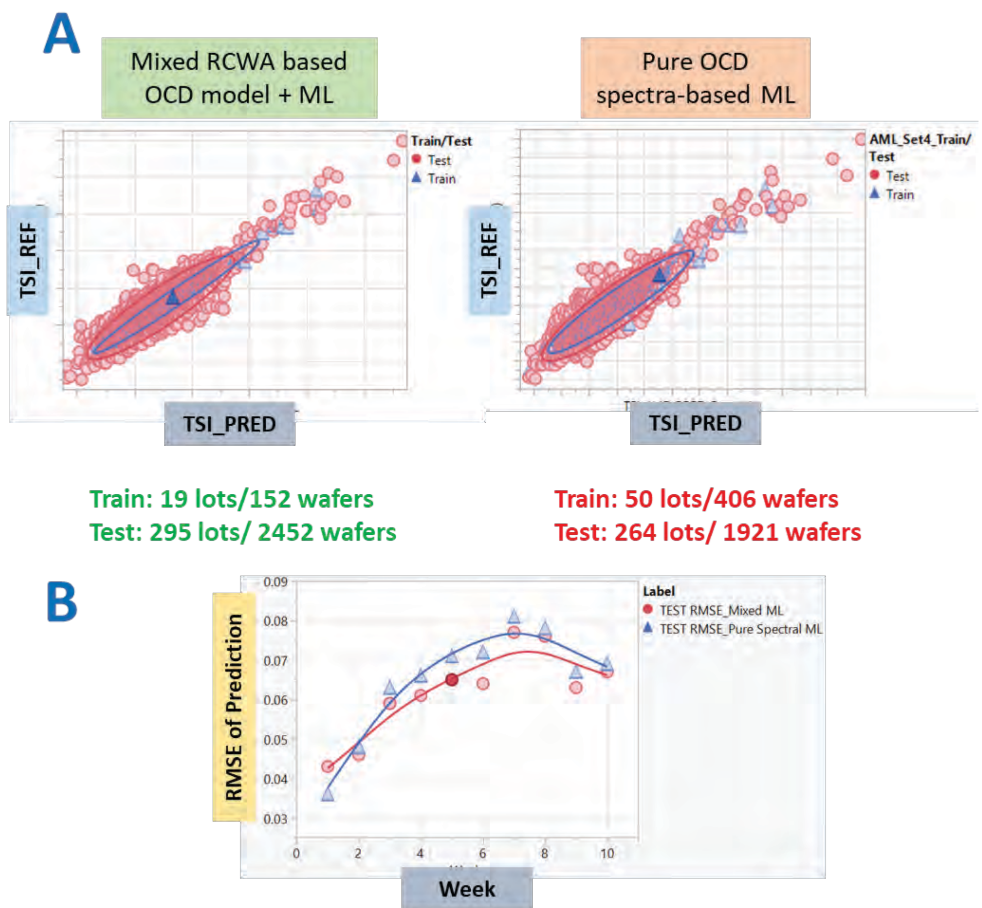

FIGURE 1. (A) Comparison of TSi measured after NWRLS etch step using OCD (y-axes) with TSi predicted from OCD spectra collected before the NWRLS etch step (x-axes). (Left) Mixed RCWA based OCD model and ML approach that uses only 19 lots worth of spectra and reference to train and (Right) Pure spectral ML approach that uses 50 lot worth of spectra and reference for comparable and stable results. (B) RMSE of TSi predicted using the two algorithms each week upon employing these models. Both the models stabilize at a RMSE of ~0.07 but the mixed ML approach stabilizes slightly faster.

KEYWORDS

Predictive Modeling, OCD, Machine Learning, Nanowire Thickness, GAA Transistors

Multi-wavelength atom probe tomography

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Atom probe tomography (APT) is a sensitive analytical tool capable of providing 3D atomic reconstructions with isotopically resolved elemental and sub-nm spatial resolution [1-3]. In the field of semiconductor manufacturing, APT is used for failure analysis, process development, and competitive engineering. The highly complex, multi-element heterogenous structures of modern electronic devices require APT tools capable of quantitative analysis of samples containing layers with different optical, thermal, and electrical properties.

Current state-of-the-art commercial APT instruments use a deep ultraviolet (DUV) light source with a wavelength of 257 nm (4.8 eV photon energy) to trigger the process of field ion evaporation from the samples under study. Historical progression of commercial APT instruments has shown that using shorter wavelength light sources results in improvements in sample survivability, especially for heterogenous samples, which is crucial for the study of semiconductor devices.

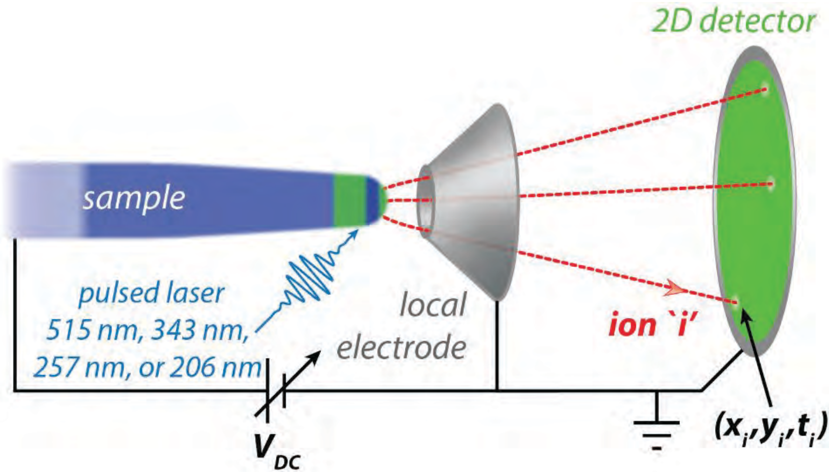

FIGURE 1. Schematic representation of multiple-wavelength laser-pulsed atom probe tomography.

In support of the semiconductor manufacturing industry, our group proposed and was tasked with the development of an APT instrument that employs a variety of wavelength sources. At NIST we are designing a beamline capable of delivering several different wavelengths (515 nm, 343 nm, 257 nm, and 206 nm) to the APT sample with similar beam parameters. This new multiple wavelength APT instrument will enable a careful study of the benefits and potential

drawbacks of each triggering wavelength, with special emphasis on sample survivability, background signal, and mass resolving power.

Our mission is to explore the APT wavelength parameter space using different triggering light sources to identify the ideal wavelength, or combination of wavelengths, best suited to improve the study of complex heterogenous semiconductor devices with APT.

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KEYWORDS

Atom Probe Tomography, Semiconductors

The Role of Ion Species in FIB-Induced Curtaining Artifacts

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INTRODUCTION

Focused ion beams (FIBs) are useful instruments for a multitude of nanomaterials characterization and manipulation activities. They are commonly used to prepare cross-sectional faces that expose sub-surface sample features for subsequent imaging and analysis. Critically, the cross-sectional face must not contain FIB-induced artifacts that would obscure the features of interest. FIB-induced artifacts can include chemical or structural modification of the surface [1] and physical distortions such as rippling [2,3] and uneven erosion of the cross-section face, often referred to colloquially as "curtaining" artifacts [4–6]. When sufficiently periodic, the surface undulations into and out of the cross-sectional plane appear reminiscent of hung window coverings. These artifacts can affect the operator's ability to obtain reliable metrology information from the nanoscale devices of interest. Conventional strategies to mitigate or otherwise prevent the formation of curtaining artifacts include using protective capping layers [7], reducing the beam current [8], and orienting the FIB incidence angle at a bias relative to interfaces within the target [4], The first two strategies serve to minimize the influence of beam tails on surface erosion in advance of the core of the beam. A protective cap provides a nominally homogenous slab of material that acts like a high-pass beam filter, while reducing the beam current reduces the size of the beam tails. In both cases, minimizing the influence of the beam tails reduces erosion of the sample surface ahead of the cross-sectional face, resulting in a more even milled surface. The third strategy avoids interfacial channeling and self-shadowing effects. Collectively, these strategies can be effective but come at the cost of increased process complexity and reduced throughput.

For numerous historical reasons, Ga^+ ions produced by a liquid metal ion source are the most prevalent ion species in commercial application. Recent advancements in source technology have enabled the introduction of various gas-phase source feedstocks, substantially increasing the pool of ion species available to include gases like argon, xenon, oxygen, or nitrogen [9,10]. Experimentation with non-Ga^+ ion species has opened a host of new applications, as well as allowing more convenient investigation into the fundamental mechanisms that govern FIB-sample interactions [11,12].

Here we share our observations of how the ion species identity can affect cross-section surface quality. Specifically, we observe that the argon ion species is fundamentally less prone to producing curtaining artifacts than either gallium or xenon ion species. We share experimental evidence that these differences are due to the identity of the ion species. We propose that the size of the ion interaction volume also plays a fundamental role in the creation and propagation of FIB-induced curtaining artifacts. Specifically, a larger interaction volume reduces the sensitivity to spatially-confined material differences and promotes rounding and softening of sharp corners. This quality reduces both the likelihood of curtaining artifact formation as well as the severity of curtaining artifacts that do appear.

RESULTS

Figure 1 shows a montage of scanning electron micrographs of diagonal slice and view mills [13] acquired from a commercially obtained 3D NAND sample and created using various ion species at various milling beam currents. The mills were created using a consistent 30 µm x 7 µm x 30 µm cleaning cross-section (CCS) pattern with the microscope stage at 0º stage tilt (FIB at 52º incidence relative to initial sample surface), a -10º rotational offset relative to the NAND slits, and +6.2º FIB scan rotation. We performed the mills without any protective cap on the sample surface. The blanked beam current and pattern time are noted in each panel of the montage. The top row of images were collected from surfaces milled with 30 keV xenon ions and various beam currents arranged in decreasing order from left to right. The middle row similarly shows images collected from surfaces milled with 30 keV gallium ions, and the bottom row shows images collected from surfaces milled with 30 keV argon ions. All the

images show the presence of pronounced curtaining artifacts. For all three ion species, the curtaining artifacts become less severe as the beam current is reduced (moving left to right), consistent with previous observations that reducing beam tails reduces the prevalence and severity of curtaining artifacts. However, the surfaces milled using 30 keV Xe^+ and 30 keV Ga^+ continue to exhibit prominent curtaining artifacts at the smallest beam currents included in the montage (4.66 nA and 2.6 nA, respectively), while there are almost no curtains visible in the surface milled using 30 keV Ar^+ ions at 9.65 nA beam current. Vitale and Sugar [14] documented relative differences in beam size between 30 keV Xe^+ and Ga^+ FIBs. The beam sizes of 30 keV Ar^+ focused ion beams are more like those of 30 keV Xe^+ and less like those of Ga^+ beams, yet they produce a surface with remarkably fewer and less severe curtaining artifacts. This observation suggests that factors related to the ion species (in addition to the beam size) affect the presence and severity of curtaining artifacts.

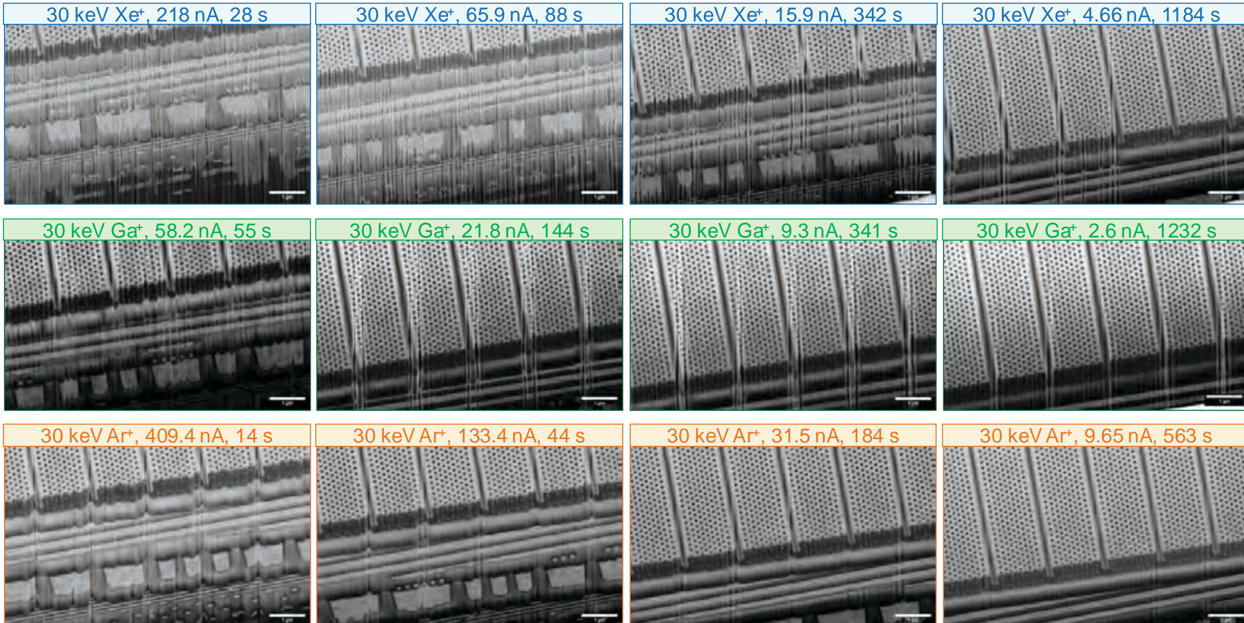

Figure 1. Montage of scanning electron micrographs from diagonal cross-section surfaces acquired using secondary electron imaging with a 2 keV primary beam energy and 0.2 nA nominal primary beam current. The beam energy, ion species, blanked beam current, and mill time are noted in the header for each panel in the montage.

Figure 2 shows the results of an experiment designed to test whether the ion interaction volume size is potentially correlated with curtaining severity. We collected cross-sectional surface contours as a function of ion dose for several different ion energy and species combinations from a silicon sample with lithographically defined sharp edges, arranged from smallest interaction volume (5 keV Xe^+) to largest interaction volume (30 keV Xe^+). The etched features were ridges approximately 3 µm wide and 0.5 µm tall with nominally vertical sidewalls. There is a clear correlation between the top edge radius of curvature that develops due to ion irradiation and the size of the interaction volume. A small interaction volume (5 keV Xe^+ in silicon) mostly preserves the sharp corner present in the initial surface topography, while a larger interaction volume (30 keV Ar^+) leads to a softer, more rounded corner. The increased tendency to erode sharp corners as the interaction volume size increases occurs because more of the collision cascade is exposed to a surface from which sputtering can occur. The qualitative appearance of the curtaining artifacts in Figure 1 is consistent with the implication of this experiment: Milling with 30 keV Xe^+ ions leads to sharper, more severe curtaining artifacts, while milling with 30 keV Ar^+ ions leads to softer, less severe curtaining artifacts and ultimately a smoother cutface.

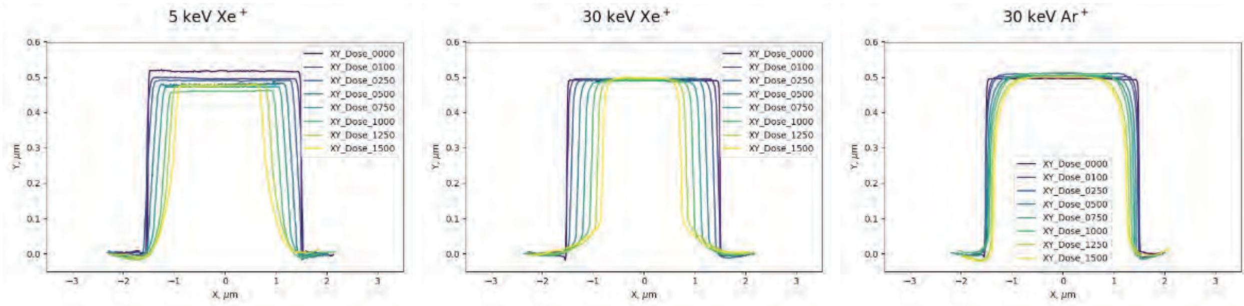

Figure 2. Cross-sectional surface contours of sharped-edged features lithographically etched in silicon irradiated by the indicated ion species, beam energy, and dose (in pC/μm^2) at normal incidence.

CONCLUSIONS

Collectively, these observations suggest that, in addition to the known mechanisms of beam tails, channeling, and differential sputtering, the size of the ion interaction volume also influences the presence and severity of FIB-induced curtaining artifacts during cross-sectioning. When available, cross-sectioning with 30 keV Ar^+ instead of 30 keV Xe^+ or 30 keV Ga^+ may enable higher throughput production of cross-sectional surfaces suitable for reliable metrology by reducing the need for complicated curtaining mitigation strategies.

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KEYWORDS

Focused Ion Beam, Cross-Section, Metrology, Curtaining, Sample Interactions, Interaction Volume

Advanced automation of both acquisition and analytical processing in routine surface chemical analysis measurements with XPS.

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Demand for surface chemical analysis across a broad swath of materials systems has seen strong growth, and the advancements in the automation of modern instrumentation provide broader access to more robust analyses over larger sample sets with advanced approaches.

The ability to measure and analyse surface chemistry and determine interfacial properties is critical to the development of compound materials systems, their interconnection, and their packaging. These surface properties become exceedingly relevant across the entire nanomaterials dimension, since, by definition, the entire volume of a nanostructure can lie within what was traditionally considered the surface region of a material, so that the bulk materials properties are no longer dominant and the surface properties dominate as the prevalent factors governing the functionality of the end material.

The increased demand for surface analysis has pushed the development of automation for hardware operation, as well as in the software processing of the data, which improves workflow efficiency and analytical consistency. The modern multi-technique XPS system incorporates automated sample handling with automated analysis by XPS, UPS, depth profiling and others, including higher energy Ag-Lα generated, quantitative HAXPES, for increased depth analysis and clarification of chemical state. Automated data handling systems can mitigate analyst bias, reduce errors, and enhance the comparability of results across different laboratories.

Automation allows for combinatorial screening of mixed materials systems, with both automated hardware operation and software tracking of the data and sample relationships. Grouped processing of data from coordinated samples then allows for improved visualization of the results. This approach will be demonstrated for discreet samples, as well as the interpolation across large inhomogeneous distributions (Figure 1).

Beyond automation of the collection and coordination of the data and relationships, modern computers allow for the automated processing of data and analysis of results. Data Dependent Analysis (DDA) allows a broader range of operators with less experience to confidently collect the correct high resolution chemical state data, selecting the appropriate core level and acquisition window. In a similar manner, batch analysis of similar samples for comparative purposes is automated with modern computers in the Known Sample Workflow (KSW), with the data collected and then automatically corrected for any charging effects and then automatically applying previously developed models and iterating the fitting routines, then producing tabular data in the report for direct comparison. Examples will show the utility of the Known Sample Workflow in comparative analysis for electronic materials development.

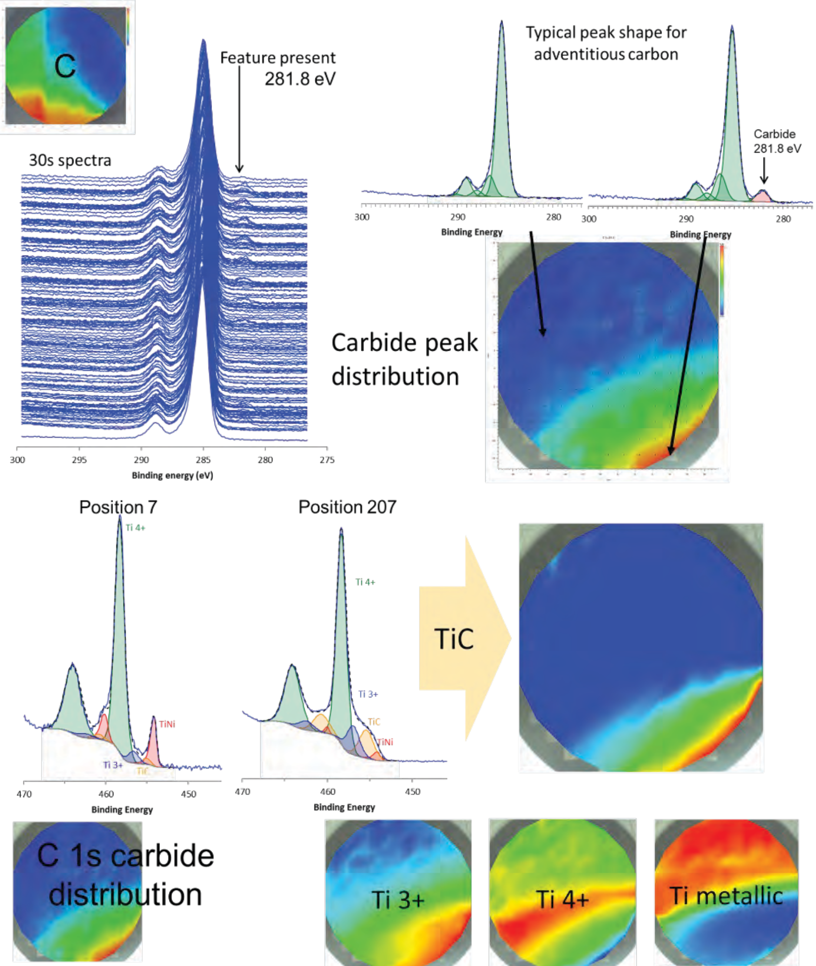

Figure 1. Group analysis shows distribution of titanium and carbon chemistries on the surface of the deposited film, identifying regions of varying Ti chemical states, including a region with TiC chemistry.

KEYWORDS

XPS, Surface Analysis, Automation

Quantum Enhanced Josephson Junction Field-Effect Transistors for Low-Energy Power-Efficient Microelectronics Applications

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Overview

The need of data centers for cloud and network computing has dramatically increased power consumption. In 2014, data centers in the U.S. consumed an estimated 70 billion kWh, representing about 1.8% of total U.S. electricity consumption [“United States Data Center Energy Usage Report," published in June 2016 and supported by the Federal Energy Management Program of the U.S. Department of Energy]. Worldwide, the International Energy Agency estimates that currently about 1% of all global electricity is used by data centers. It is expected that by 2030 the electricity use of information and communications technology may exceed 20% of all global electricity.

Superconducting computing is a promising approach for low-energy, power-efficient microelectronics applications [1]. Moreover, using superconducting interconnects can further reduce power consumption. Josephson junction field-effect transistors (JJFET, Fig. 1a) [2] have emerged as a promising candidate for superconducting computing. JJFETs are particularly useful for low power consumption applications as they are operated with, in the superconducting regime, zero voltage drop across its source and drain. Feasibility of using JJFETs for logic operations has been explored [3,4]. Moreover, high noise margin has been demonstrated for the logic inputs [5].

For JJFETs to perform logic operations, the gain-factor (α_R) value must be larger than 1. Here $\alpha_R = dI_c/d(V_g–V_t) \times \pi\Delta/I_c$, Δ is the superconducting gap, V_g the gate bias voltage, V_t the threshold voltage, I_c the critical supercurrent. In conventional JJFETs [6], V_g-V_t ~ 0.1V. For α_R greater than 1, this requests a superconducting transition temperature of ~ 400K, far exceeding recorded critical temperatures. As such, it is impossible to use conventional JJFETs for logic operations.

Device and Results

Here, we propose a novel type of JJFET based on quantum phase transition, such as the excitonic insulator (EI) transition in a type-II InAs/GaSb heterostructure [7], for low-energy, power-efficient logic applications. The nature of the collective phenomenon in the EI quantum phase transition can provide a sharp transition (i.e., V_g-V_t very small, ~ 10mV) of the supercurrent states (as shown in Figs. 1b and 1c, respectively) which should enable α_R greater than 1 with an easy-to-achieve superconducting transition temperature. In this presentation, we will present some preliminary results demonstrating that indeed the gain factor in these quantum enhanced JJFETs can be greatly enhanced [8], thus making them a promising candidate for logic applications [3].

Fig. 2a shows a JJFET made of a zero-gap InAs/GaSb heterostructure with tantalum (Ta) as the source and drain electrodes. The superconducting critical current in the JJFET is zero when V_g-$V_t \leq 0.23$V, but sharply jumps to a finite value at V_g-$V_t = 0.24$V and then increases slowly as V_g-V_t continues to increase (Fig. 2b). The gain factor is calculated to be ~ 0.06 [8]. Though still less than 1, it is already more than 50 times larger than that recently reported in a conventional JJFET made of InAs quantum wells [6]. With further optimizations, we believe a gain factor greater than 1 can be achieved.

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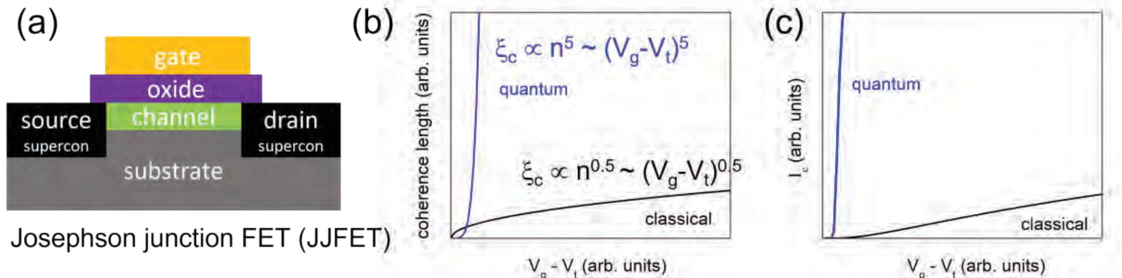

Fig. 1: (a) Schematic of a Josephson junction field-effect transistor (JJFET). The source and drain electrodes are made of superconducting material tantalum. (b) Schematic gate bias dependence of coherence length in a conventional classical JJFET and in a quantum enhanced JJFET. (c) Gate bias dependence of superconducting critical current calculated for classical and quantum JJFETs.

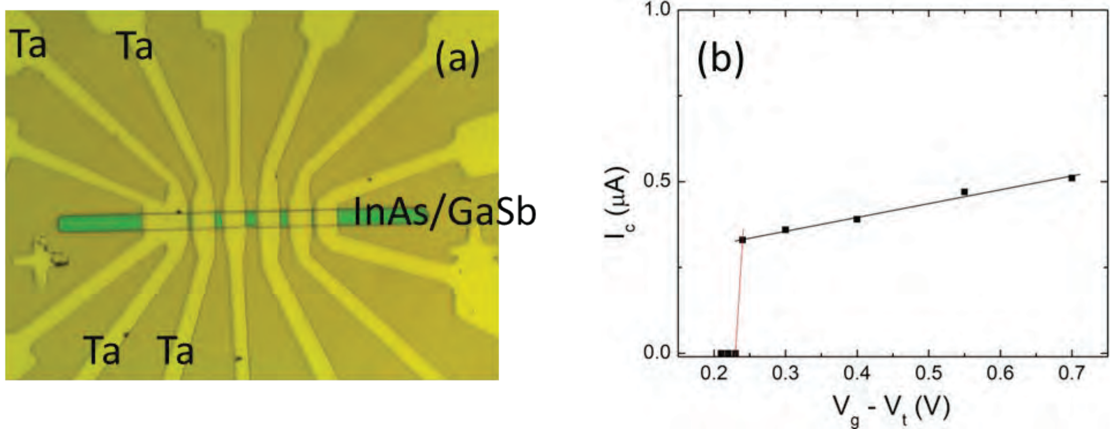

Fig. 2: (a) Optical image of a JJEFT device. The green-colored bar represents the InAs/GaSb heterostructures. Superconducting Ta electrodes are marked for the Josephson junction studied. (b) Critical current I_c versus V_g-V_t. Lines are linear fits. The slope of the red line is $dI_c/dV_g = 33$ μA/V.

Topics – Nanoelectronics Materials and Devices; Hybrid Structures; Channel Engineering

Key words: low-power, energy-efficient microelectronics; superconducting computing, quantum, Josephson junction, field-effect transistor

Using Computational Suppression of Diffraction Artifacts to Enhance OV Metrology Precision

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INTRODUCTION

In the semiconductor industry, overlay (OV) is a critical step which measures the lateral alignment of different wafer layers in a multilayer stack. This is a metrology process and is important in large scale production to tune the fabrication process and flag the problematic wafers early. As device dimensions shrink to nanometer scale, it is imperative to measure the overlay error with sub-nm precision. Dark-field digital holographic microscopy (DHM) has emerged as a promising technique to address the challenges of OV metrology[1]. This is a diffraction-based overlay (DBO) technique where the intensity difference between +1st and -1st diffraction orders corresponding to two biased overlapping gratings, scales linearly with the overlay error[2]. Additionally, DHM captures the complex optical field (amplitude and phase) as a hologram using a reference beam and there by enabling a flexible computational filtering in the pupil plane.

Currently, diffraction-based overlay (DBO) metrology relies on high-precision intensity measurements. While this approach performs well for targets with dimensions around 16×16 µm², it faces increasing limitations as target sizes shrink below 10×10 µm². At these smaller scales, finite grating effects become more pronounced. Specifically, the sharp edges of the grating broaden the zeroth-order diffraction peak, causing signal leakage into the first-order peak, which is the primary signal used for overlay measurement. This unwanted interference introduces errors in intensity readings and significantly compromises overlay accuracy.

We present a computational method to suppress these spurious signals. By modeling the error and subtracting it from the main signal, we effectively isolate the desired diffraction peak without compromising resolution. This approach enables improved precision in overlay measurements, particularly for smaller metrology targets, and paves the way for more robust DBO metrology in advanced semiconductor nodes.

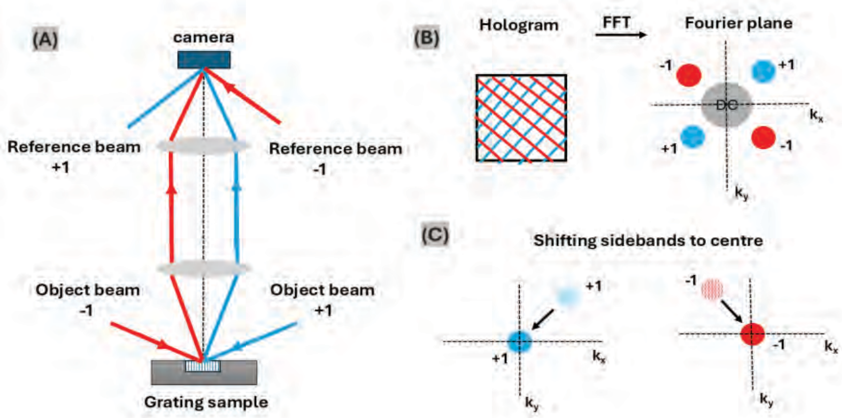

FIGURE 1. Illustrating off-axis holographic recording and processing concept. **A.** Schematic of the dark-field off-axis digital holography microscopy. **B.** Recorded digital hologram with two overlapping interference patterns of the +1st and -1st diffraction orders. Performing a 2D-FFT propagates the hologram back to the pupil plane. **C.** Selecting the sidebands and translating them to the center of the pupil plane.

Posters

ZEROTH ORDER LEAKAGE

In our dark field DHM set up, a digital hologram recorded by the camera helps in reconstructing the object field. As shown in Fig. 1, we computationally propagate from the image plane to the pupil plane and obtain an angular spectrum with a base band, i.e., autocorrelation signal and four sidebands. The baseband does not contain any information about the phase of the object whereas the sidebands encode both the amplitude and phase. Due to the off-axis angle configuration of the reference beams, the sidebands are fully separated from the baseband. One of the sidebands is translated to the center of the pupil plane. Finally, via an inverse Fourier transform, the object field of either the +1st and −1st is retrieved. The intensity corresponding to the object fields of +1 and -1 are directly proportional to the overlay error. Hence, for accurate measurement, a bigger RoI (Region of Interest) of the grating is used. However, images of smaller targets show bright edges as artifacts owing to the finite grating size (Fig. 2). The sharp edges of a finite grating results in the broadening of the zeroth order signal (Fig. 2) in the spatial frequency domain. This broadening is inversely proportional to the grating size and is severe as the target size decreases. A well-known solution to suppress spurious signals is to use an apodization filter[3]. Such filters reduce Gibbs ringing effects but it will be at the expense of resolution. Additionally, there is also reflectivity difference between the top layer and the grating itself which contributes to the signal imperfections. One of the simplest solutions for measuring accurate intensity is to choose a smaller RoI which ignores the edges of an image. But, with a smaller grating of size $< 10 \times 10\ \mu m^2$, the RoI might have to be the entire grating as more photons are available for the measurement. Hence, it is better to suppress the zeroth order signal to improve imaging at smaller dimensions.

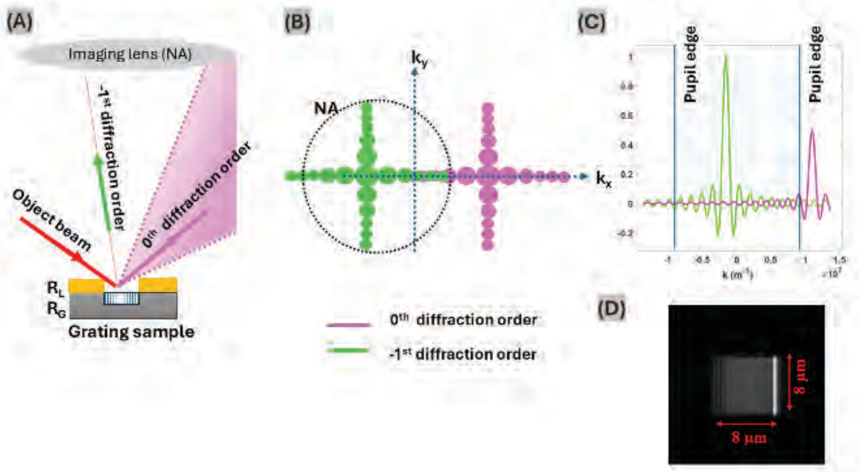

FIGURE 2. (A) Illustration of zeroth diffraction order leakage concept in dark-field configuration with an oblique object beam. (B) 2D pupil plane (C) 1D cross section of the pupil plane. Here, pink is the zeroth diffraction order and green is the -1st order. (D) An example of experimentally captured image of a grating of size $10 \times 10\ \mu m^2$; bright edge is clearly visible.

MODEL-BASED SUPPRESSION OF ZEROTH-ORDER

We usually have prior knowledge about basic parameters of the overlay metrology targets. Variables such as size and pitch of the grating, duty cycle of the grating lines, and grating material are accurately known and this helps us to construct a model based on the physics of diffraction through the grating. As we have discussed in the previous figure, even though we rely on 1st diffraction order for our overlay measurements, the zeroth order leakage into the pupil plane introduces artifacts in the final intensity and this can be modelled as a combination of 2D sinc functions. The square gratings used here are equated to the summation of two sinc functions corresponding to zeroth and 1st order of diffraction. Both the orders here have a certain phase difference which is directly related to the depth of the grating, material properties of the grating lines and the background wafer (owing to difference in transmission or reflectance). This becomes an optimization problem where we try to fit the pupil plane with our model and the initial guesses are also based on the knowledge of the sample and its image plane. The fitted model presents us with the contribution from zeroth and first orders and hence one can subtract the unwanted signal, here the zero order to

finally retrieve the corrected image plane[4]. The suppression of artifact from the images can be used for accurate measurement of OV error.

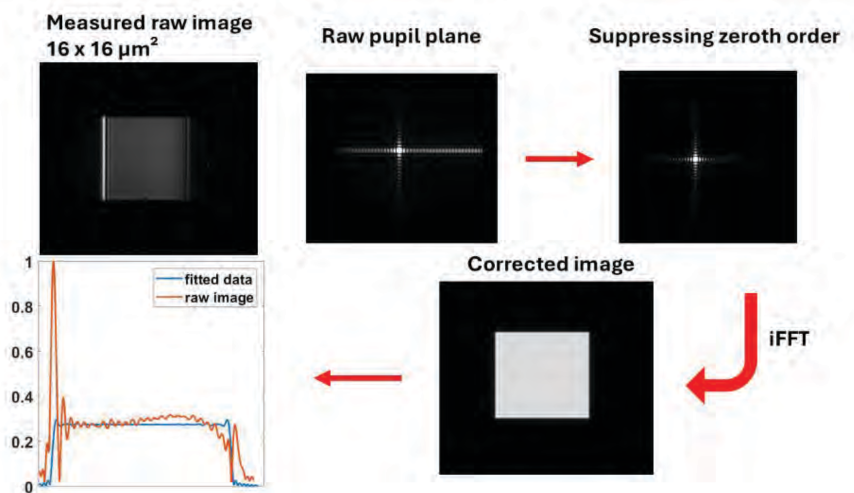

FIGURE 3. The measured raw image of a grating 16x16 µm² is shown here with a bright edge. The pupil plane of this image reveals the extent of zeroth order leakage. After suppressing the artifact using the sinc function model optimisation, the corrected pupil plane is retreived by inverse Fourier transform. A comparison of intensities of the raw image and corrected image is shown which reveals the suppression of bright edge.

CONCLUSION

We present here the coupling of DHM and computational techniques, where we retrieve the full complex field and are able to modify the signals of interest through model-based optimization technique. This can be a way to increase the RoI of the grating image for better intensity measurement, leading to higher precision in metrology. We demonstrate here the suppression of zeroth order resulting in eliminating the bright edges in the image plane. This modelling and suppression technique will further be strengthened by using a more complex model which directly correlates grating properties to the phase used in the optimization step. This will allow us to investigate much smaller (~1 x 1 µm²) metrology targets.

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KEYWORDS

Semiconductor metrology, digital holographic microscopy, computational imaging, diffraction artifacts

Multiscale Strain Characterization using Moiré Sampling in Aberrations Corrected Scanning Transmission Electron Microscopy

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INTRODUCTION

Aberration-corrected Scanning Transmission Electron Microscopy (STEM) is a key method in modern materials and device characterization, offering direct imaging of atomic arrangements and interfaces [1]. Its high spatial resolution has been crucial for understanding strain and defect formation in advanced semiconductor architectures, including, SiGe stressors, and oxide heterostructures used in quantum and neuromorphic devices. However, the imaging field-of-view (FOV) of high-resolution STEM remains restricted by the Whittaker–Kotelnikov–Shannon–Nyquist sampling theorem [2]. The sampling grid spacing must remain smaller than half the probe size, which limits conventional high resolution STEM imaging to approximately 100–150 nm in FOV.

For semiconductor metrology or failure analysis, this limitation prevents direct visualization of multiple device-scale strain fields and long-range lattice distortions. Collecting stitched atomic-resolution datasets over micron-scale regions is time-consuming, electron-dose intensive and involved additional post processing tasks. Thus, bridging the length-scale gap between atomic-resolution microscopy and micron scale analysis is an essential goal for future nanoelectronics characterization.

In this work, we demonstrate that Moiré sampling in STEM can overcome these limitations by enabling undersampled acquisition of periodic crystalline signals. The technique allows the extraction of structural and strain information beyond conventional Nyquist constraints, expanding the effective FOV by an order of magnitude while maintaining atomic-scale sensitivity.

MOIRÉ SAMPLING IN STEM

Moiré sampling relies on the coherent interference between a crystalline lattice and a sampling grid. When the sampling spacing is intentionally mismatched with the crystal periodicity, the resulting aliasing produces a Moiré pattern (hologram) that embeds the high-frequency lattice information into a lower-frequency envelope ((see Fig. 1b-c)). Provided that the original structure is periodic and bandwidth-limited, this Moiré hologram can be mathematically inverted to recover the oversampled lattice information [3] or directly analyzed to map strain and orientation fields [4].

In STEM, this concept transforms conventional oversampling schemes into deliberate structured undersampling strategies. Since the position of the electron probe is controlled during the image acquisition, the sampling grid can be designed to generate Moiré patterns with well-defined spatial frequency distributions. Once the sampling parameters (such as scan step size and scan rotation) are set, the Moiré pattern acts as a magnified projection of the crystal lattice, making long-range deformations and periodic modulations accessible without atomic-resolution oversampled STEM images over the entire region. This approach extends the capabilities of aberration-corrected STEM imaging towards large FOVs up to several microns [5].

APPLICATIONS TO SEMICONDUCTORS

To illustrate the potential of this method, we apply Moiré sampling in STEM to semiconductor materials and device relevant to nanoelectronics. Because the Moiré fringes encode the underlying crystalline lattice, quantitative analysis of their modulation allows the strain field to be mapped across the entire field of view. By adapting the Geometrical Phase Analysis (GPA) methodology with a Moiré correction, the two-dimensional strain tensor can be directly extracted using well-established algorithms [6]. Two representative examples are presented in this study:

- InP/InAsP/InP epitaxial thin films, analogous to the SiGe/Si system, where Moiré sampling enables monitoring of growth quality and relaxation behavior over multiple length scales (Fig. 1d-e)).
- AlGaN/GaN heterostructures engineered as nanorods for deep-UV light-emitting diodes, where the approach captures the deformation field across multiple adjacent devices within a single acquisition (Fig. 1f-g)).

Beyond the extension of the field of view, several additional advantages emerge from the Moiré sampling approach. First, the Moiré fringes are intrinsically more sensitive to small lattice deformations when recorded over larger fields of view. The loss of spatial resolution in the strain maps caused by large sampling is compensated by a significant increase in phase sensitivity [7]. Second, the Moiré fringes highlight abrupt variations in periodicity near interfaces, dislocations, or other structural defects, enabling their identification and tracking over extended regions (Fig. 1g)). Finally, Moiré sampling is a continuous phenomenon that can be tuned across different magnifications, allowing the method to adapt naturally to the morphology and scale of the material or device under investigation.

CONCLUSIONS

Moiré sampling in aberration-corrected STEM represents a promising route toward multiscale strain characterization in semiconductor and quantum materials. By deliberately undersampling crystalline lattices, it enables large-area imaging and low-dose strain mapping without compromising lattice information. The method bridges the gap between atomic-resolution microscopy and device-level metrology, offering a valuable complement to conventional techniques such as X-ray nanodiffraction or 4D-STEM. Continued developments in hardware (off-axis aberrations correctors), sampling strategy, and reconstruction methods will further consolidate Moiré sampling as a powerful methodology for the next generation of nanoelectronic devices.

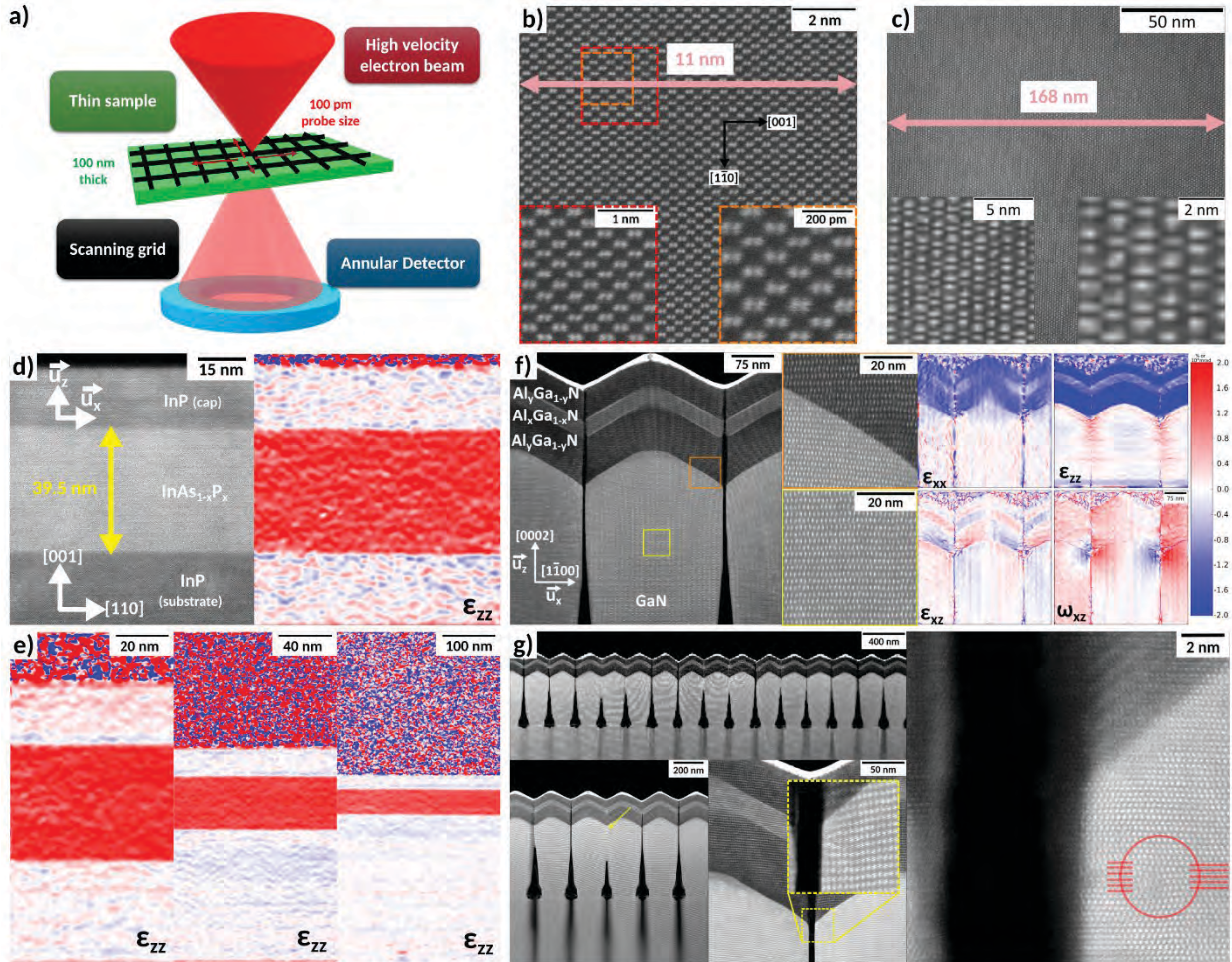

FIGURE 1. Overview of STEM Moiré imaging for strain mapping on semiconductor materials and devices. a) Schematic of the STEM imaging setup. b) Oversampled STEM image acquired on silicon. c) Undersampling STEM image acquired on silicon revealing a Moiré pattern. d) STEM image of an InP/InAsP/InP stack and the associated uniaxial relative deformation along the growth direction Ezz using Geometrical Phase Analysis. e) Ezz strain maps from the same sample as in d) using STEM Moiré imaging. f) STEM Moiré image of an AlGaN/GaN LED device and the corresponding strain maps. g) STEM Moiré images of the AlGaN/GaN LED devices over different field of view, revealing an edge dislocation at low magnification.

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KEYWORDS

Scanning Transmission Electron Microscopy; Moiré Sampling; Strain Mapping; Semiconductor Devices; Undersampling

X-ray Scattering Metrology Solutions for Semiconductor Materials: A Comprehensive Overview

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INTRODUCTION

Semiconductor device performance is fundamentally governed by structural parameters such as microstructure, phase composition, layer thickness, and defects. Precise control of these features is essential for enabling advanced semiconductor materials engineering, process optimization, and device reliability [1, 2]. X-ray scattering metrology constitutes a non-destructive, high-resolution technique for characterizing structural attributes across a broad spectrum of material systems, including highly crystalline and amorphous films, and spanning sample scales from full 150 mm silicon carbide (SiC) substrates to nanometer-thick thin film layers.

This work presents the application of a comprehensive suite of X-ray scattering techniques for structural and quality assessment of semiconductor materials. These techniques include high-resolution X-ray diffraction (HRXRD), reciprocal space mapping (RSM), grazing incidence XRD (GI-XRD), wide-angle XRD (WA-XRD), in-plane and asymmetric XRD, omega and phi scans, and X-ray reflectivity (XRR). HRXRD and RSM are utilized to determine epitaxial film thickness, composition, and defectivity. GI-XRD enables analysis of randomly oriented grains in polycrystalline films, while WA-XRD and in-plane XRD resolve out-of-plane and in-plane crystallographic structures and orientations, respectively. Asymmetric XRD provides complementary directional insights, and omega/phi scans are employed to assess crystal orientation and quality, particularly in monocrystalline materials. XRR facilitates quantification of film thickness, density, and interface roughness through electron density contrast.

Collectively, these methods enable rapid, high-precision characterization of complex film stacks and heterostructures, supporting accelerated process development and improved engineering control over material properties. The metrology solutions discussed in this study address high-value problems across multiple Applied Materials business units, with selected examples demonstrating broader applicability throughout diverse semiconductor platforms.

RESULTS AND DISCUSSION

This study presents six case studies in which Applied Materials process engineers applied a targeted methodology to address high-value problems across diverse semiconductor applications. Each case demonstrates how scenario-specific techniques, particularly advanced X-ray scattering methods, enabled precise material characterization and process optimization.

The first case focuses on metal carbide hard masks used in dynamic random-access memory (DRAM) capacitor applications [3]. These masks require amorphous or nanocrystalline films to ensure uniform etching performance. While scanning electron microscopy (SEM) provides limited quantitative insight, GI-XRD enables detailed grain size analysis. As shown in Figure 1, a 20 nm cubic WC film transitions to an amorphous phase under deposition conditions A, B, and C. These conditions differ slightly in composition, with higher tungsten content correlating with smaller grain sizes. In addition to crystalline structure, diffraction intensity scales with atomic number via the scattering factor; therefore, higher tungsten content results in stronger diffraction peaks, as observed in Figure 1. Grain size can be calculated using the Scherrer equation [4], which is correlated with the full width at half maximum (FWHM) of the diffraction peaks. Peaks broader than 5° indicate an amorphous structure with grain sizes below 20 Å. This is the case for deposition condition C. This study underscores the value of compositional tuning and advanced diffraction techniques in achieving the desired phase and microstructure for etch-critical DRAM hard mask applications.

The second case investigates hexagonal boron nitride (hBN) as a material for enhancing heat dissipation in next-generation chips with back-side power delivery. Precise control of film crystallinity is critical, and a combination of

WA, in-plane, and GI-XRD techniques was employed to obtain comprehensive structural insights. Efficient thermal conduction occurs perpendicular to the ⟨001⟩ orientation due to strong B–N covalent bonding. The data indicate that vertically textured nanocrystalline hBN with larger grain sizes achieves optimal out-of-plane thermal conductivity. Figure 2 presents XRD data for a 170 nm hBN film ($\kappa \approx 18$ W/m·K), along with schematics illustrating its structure and preferred heat flow direction. These findings highlight the importance of crystallographic orientation and grain size engineering in optimizing thermal performance of hBN films for advanced chip architectures.

In the third case, our team addressed the need for high-quality hexagonal gallium nitride (GaN) in micro light-emitting diode (MicroLED) display applications. Achieving monocrystalline GaN is critical for device performance, particularly in minimizing defect-related light leakage and enhancing pixel uniformity. To evaluate crystal quality during process development, symmetric and asymmetric XRD techniques were employed, along with omega and phi scans. Figure 3 presents XRD data for a 1 μm GaN / 700 nm aluminum nitride (AlN) / Si stack, featuring GaN phi scans, rocking curve FWHM values for the (002) (~34.6°) and (102) (~48.1°) reflections, and calculated threading dislocation densities (TDDs) for both screw and edge type TDDs. These results demonstrate the effectiveness of advanced XRD techniques in quantifying crystalline quality and dislocation density, characteristics that critically influence the engineering of GaN layers in high-resolution MicroLED displays

The fourth case focuses on precise off-cut determination for 4H-SiC substrates, a critical parameter for evaluating epitaxial layer and substrate quality, as well as ensuring accurate device processing. Channeling implantation depends heavily on this parameter to achieve precise implant profiles. To assess wafer orientation, WAXRD and omega scans were performed using the 004 reflection (~35.6°). Omega scans were collected at φ = 0°, 90°, 180°, and 270°, producing a sinusoidal fit from which both the off-cut angle and direction were extracted. Figure 4 presents the omega scan data, peak-φ correlation, and the fitted off-cut result summarized in the inset table. This method enables reliable extraction of off-cut parameters, which are essential for optimizing channeling implantation and achieving high-quality device fabrication on 4H-SiC substrates.

The fifth case supports the integration of sequential complementary field-effect transistors (CFETs), which vertically stack p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) devices. Our team developed a fast, non-destructive metrology approach for characterizing Si/SiGe superlattices (SLs) used in layer transfer processes [5]. Conventional techniques such as transmission electron microscopy (TEM) are destructive and time-consuming, making them unsuitable for high-throughput monitoring. We demonstrated that X-ray scattering methods, including HRXRD, RSM, and XRR, effectively detect interfacial roughness and structural changes induced by hydrogen implantation, a critical step in the silicon cut process. This process has been proposed to reduce layer transfer costs by enabling reuse of the donor wafer substrate. While hydrogen implantation does not significantly alter layer thickness or density, it nearly doubles interfacial roughness, as shown in Figure 5, which may impact channel integrity. These findings establish X-ray-based metrology as a scalable, non-destructive alternative to TEM for inline monitoring of transfer layer quality in advanced logic device fabrication.

In the final case, we investigated XRR method to enhance self-assembled monolayer (SAM) selectivity on chemical vapor deposition (CVD) molybdenum (Mo) surfaces through post-pre-clean treatments for back-end-of-line (BEOL) logic applications. SAMs play a critical role in area-selective deposition by suppressing unwanted tantalum nitride (TaN) growth, and selectivity gain is defined by the reduction in TaN thickness on treated versus untreated Mo surfaces. XRR revealed treatment-induced changes in Mo density profiles, which correlated with improved SAM performance. Figure 6 and Table 1 present data from eight Mo films, linking higher Mo density to improved TaN selectivity. Among the treatments tested, Treatment 4 most effectively densified Mo and maximized selectivity gain. These findings demonstrate that surface densification via tailored pre-clean treatments can significantly improve SAM-based selectivity, offering a promising route for precise material engineering in advanced BEOL integration.

SUMMARY

This study demonstrates the strategic application of advanced X-ray scattering techniques to address critical process challenges across a wide spectrum of semiconductor technologies. Through six distinct case studies, we illustrate how scenario-specific metrology approaches enabled precise structural characterization and informed process optimization. In DRAM capacitor fabrication, GI-XRD revealed the relationship between tungsten content and grain size in metal carbide hard masks, guiding phase control for etch performance. For thermal management in next-generation chips, WA-XRD, in-plane XRD, and GI-XRD provided insights into hBN crystallinity and orientation, directly correlating with enhanced out-of-plane thermal conductivity. In MicroLED display development, symmetric and asymmetric XRD, along with omega and phi scans, quantified GaN crystalline quality and threading

dislocation densities, supporting defect mitigation strategies. Off-cut determination for 4H-SiC substrates was achieved through WAXRD and omega scans, enabling accurate channeling implantation and improved device processing. For CFET integration, HRXRD, RSM, and XRR offered a non-destructive alternative to TEM, detecting hydrogen-induced interfacial roughness in Si/SiGe superlattices and supporting inline monitoring of transfer layer quality. Finally, XRR was used to evaluate Mo surface densification via pre-clean treatments, revealing a strong correlation between Mo film density and SAM selectivity, which is essential for area-selective deposition in BEOL logic applications.

Together, these findings underscore the versatility, precision, and scalability of X-ray scattering metrology in modern semiconductor process engineering. As device architectures continue to evolve, the continued advancement of scattering-based techniques will be pivotal in enabling reliable, high-performance manufacturing across emerging platforms.

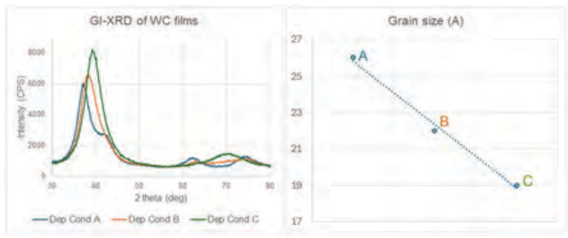

FIGURE 1. GI-XRD 2θ scan at 0.9° incident angle with calculated grain sizes for deposition conditions A, B, and C (~20 nm thickness).

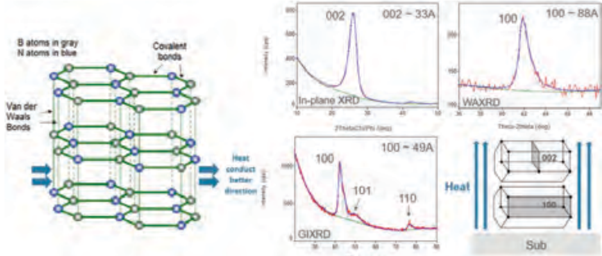

FIGURE 2. In-plane, WA, and GI-XRD scans of a 170 nm hBN film (κ ≈ 18 W/m·K), with schematics illustrating layered structure and preferred heat dissipation direction

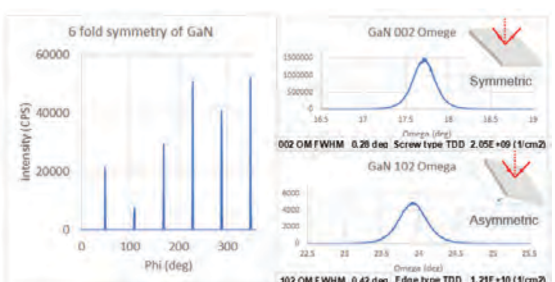

FIGURE 3. XRD φ, symmetric, and asymmetric ω scans of a 1 µm GaN / 700 nm AlN / Si stack, showing monocrystalline features, rocking curve FWHM, and calculated screw and edge type TDDs

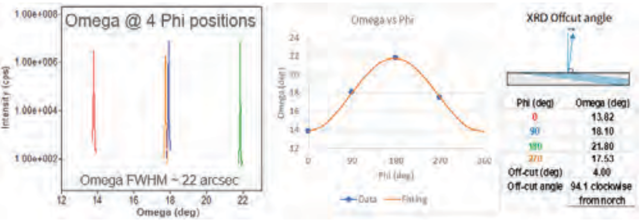

FIGURE 4. Omega scans at four phi positions, omega peak position–phi correlation, and off-cut schematic with fitted results (inset table) for a 150 mm SiC substrate

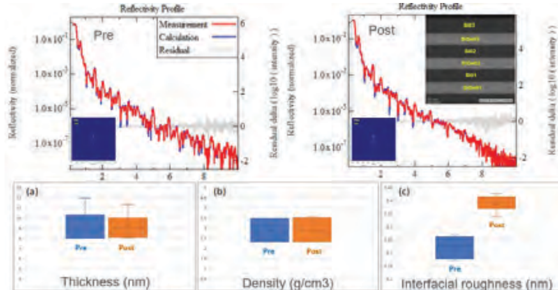

FIGURE 5. XRR fits for Si/SiGe transfer layers pre-/post-H_2 implantation. Insets show asymmetric (224) RSMs confirming no SL relaxation and a TEM image of the SL in the post XRR data. Comparison includes (a) thickness, (b) density, and (c) interfacial roughness for both conditions.

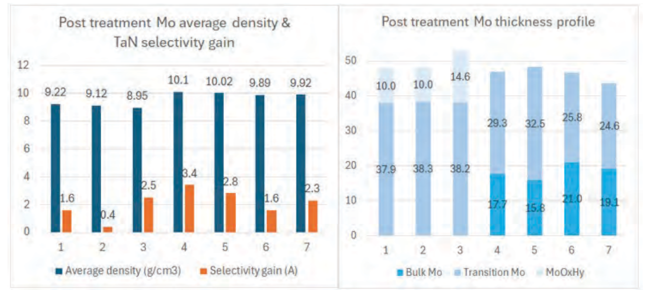

FIGURE 6. XRR analysis of eight Mo films on a 50 Å Mo / 50 Å W / 1kÅ SiO_2 / Si stack, showing Mo density and TaN selectivity gain (left). Treatment 4 yields the highest densification and selectivity gain. Post-treatment Mo thickness profiles include surface MoOxHy, transition Mo, and bulk Mo (right).

Posters

TABLE 1. Structural and selectivity characteristics of Mo films before and after treatment: layer-specific density, thickness, average density, and TaN selectivity gain

Treatment	MoOxHy		Transition Mo		Bulk Mo		Average density	Selectivity gain
	ρ (g/cm3)	THK (Å)	ρ (g/cm3))	THK (Å)	ρ (g/cm3)	THK (Å)	ρ (g/cm3))	THK (Å)
NA	1.82	16.8	9.55	30.6	9.60	8.9	9.56	N/A
1	2.75	10.0	9.22	37.9	N/A	N/A	9.22	1.6
2	3.11	10.0	9.12	38.3	N/A	N/A	9.12	0.4
3	1.78	14.6	8.95	38.2	N/A	N/A	8.95	2.5
4	N/A	N/A	10.00	29.3	10.28	17.7	10.10	***3.4***
5	N/A	N/A	9.90	32.5	10.28	15.8	10.02	2.8
6	N/A	N/A	9.66	25.8	10.16	21.0	9.89	1.6
7	N/A	N/A	9.78	24.6	10.10	19.1	9.92	2.3

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KEYWORDS

X-ray scattering, X-ray diffraction (XRD), X-ray reflectivity (XRR), semiconductor materials, metrology solution

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Nanoscale Measurement of Semiconductor Interface Electric-Fields

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INTRODUCTION

The ability to accurately predict and control interface behavior in semiconductor devices is increasingly important as device size continues to decrease and complexity continues to increase. To enable accurate predictions, nanoscale measurements of interface structure, chemistry, strain and electric field are needed. The high brightness and spatial resolution of modern scanning transmission electron microscopes (STEMs) have facilitated many of these measurements, but atomic scale measurement of electric field remains challenging.

METHODS

We are investigating measurement of electric field by two S/TEM based techniques: electron holography (EH) and differential phase contrast (DPC). Both techniques allow determination of the in-plane electric field distribution in a specimen through detection of the phase shift of the electron beam as it is transmitted through the sample. In EH, the phase shift is determined by splitting the electron beam into two parts, one of which is transmitted through the sample and the other through vacuum, then interfering the beams to obtain an image of the sample-induced phase shift, as illustrated in Fig. 1 a).[1] In DPC, field-induced shifts in the transmitted, convergent electron beam are measured as a function of position in the specimen with segmented or pixelated electron detectors, Fig. 1 b).[2,3] Using these methods we have measured electric-field distributions across a variety of semiconductor interfaces including a homoepitaxial GaAs p-i-n junction. We compare the results with predicted electric-field distributions modeled with a commercially available self-consistent Schrödinger-Poisson-Current solver using nominal sample dimensions and doping concentrations.

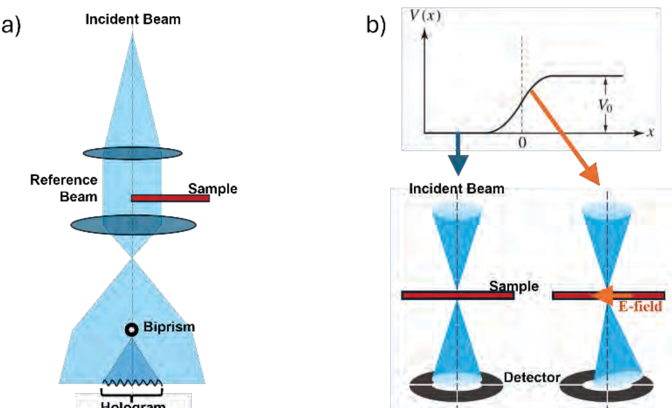

FIGURE 1. Two S/TEM based methods to measure electric fields. In both the field in the sample deflects the transmitted beam. This deflection can be retrieved from a) interference fringes formed by adding the deflected and reference beams together (EH), or b) direct measurement of the transmitted beam deflection (DPC).

RESULTS AND DISCUSSION

Electric-field distributions measured across the GaAs p-i-n homojunction by EH and DPC in a 406 nm thick S/TEM lamella are shown in Fig. 2, along with predicted distributions modeled for two sample thicknesses. Measurements were also made of lamella with thicknesses of 72 nm, 109 nm, 173 nm, 204 nm and 315 nm (not shown).

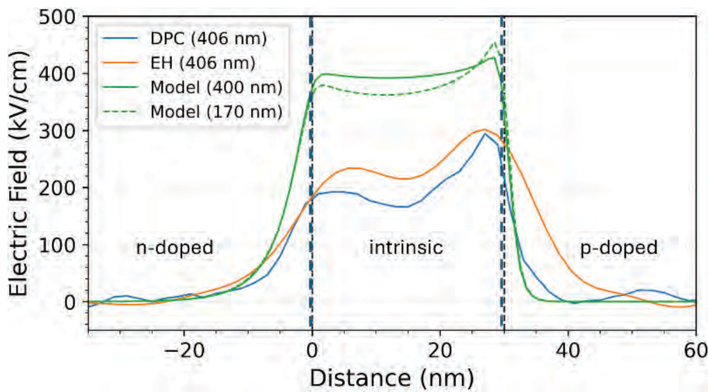

FIGURE 2. Electric field distributions measured and modeled for a GaAs p-i-n homojunction. The nominal width of the intrinsic region was 30 nm, and the nominal doping levels of the n- and p- layers were $5x10^{18}$ and $1x10^{20}$ /cm^3 respectively.

As can be seen in the figure, EH and DPC produced qualitatively similar measurements of the electrical field within the sample, however, the field magnitudes were considerably smaller than that predicted by modeling. Some of this difference can be attributed to surface damage caused by the ion-beam preparation of the S/TEM lamella. Consistent with this, measurements of the thinnest samples (72 and 109 nm) yielded even lower electric fields, as a larger fraction of the sample thickness was damaged and inactive.

Another factor potentially contributing to the difference in field magnitude is uncertainty in the lamella thickness measurement. For both experimental techniques, accurate measurement of the sample thickness is as important as the measurement of the phase shift in determining the magnitude of the electric field, and overestimation of sample thickness can substantially reduce the measured electric field. Related to this, it is interesting that the shape of the measured field at the doping interfaces is more similar to that modeled for a thinner lamella (170 nm), where surface pinning has a larger effect, than to that predicted for the 400 nm thick lamella, suggesting the thicknesses of the lamella contributing to the electron beam phase shift may be significantly thinner than the measured thickness.

The EH measurements were generally more reproducible than DPC measurements for different thickness samples. However, the electric fields determined from EH data were broadened due to the gaussian filtering used to reduce noise from the biprism fringes. This broadening is particularly evident in regions where the field changes quickly (e.g at the junction interfaces).

More details of the influence of these and other parameters on the measurements of the GaAs homojunction and other samples will be discussed.

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KEYWORDS

electric field, interfaces, nanoscale, transmission electron microscopy, modeling

OBF-STEM: Enhancing Critical Dimension Measurements of Low-Contrast Beam Sensitive Semiconductor Structures

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INTRODUCTION

The continuous downscaling of semiconductor devices demands highly reliable metrology methods capable of resolving features at the nanometer scale. Transmission Electron Microscopy (TEM) and Scanning Transmission Electron Microscopy (STEM) have become indispensable tools in this field, providing direct and quantitative structural information with sub-nanometer precision. In both logic and memory devices, thin dielectric layers such as silicon oxynitride (SiON) and silicon dioxide (SiO_2) remain fundamental materials for device performance and reliability. They serve as gate dielectrics, tunneling barriers, and interfacial layers, playing crucial roles in controlling carrier transport, minimizing leakage current, and maintaining charge retention. As device dimensions continue to scale and the equivalent oxide thickness approaches the sub-nanometer regime, the structural integrity and uniformity of these layers become increasingly critical. However, their amorphas nature, ultrathin thickness, and low atomic number composition result in inherently low contrast in electron microscopy, making accurate visualization and critical dimension measurement particularly challenging.

METHODOLOGY AND IMAGING APPROACH

To address these challenges, we explored the use of STEM-OBF (Optimum Bright Field)[1)] imaging for quantitative metrology of low-contrast dielectric structures. STEM-OBF reconstructs image contrast from segmented detector signals using a phase–sensitive algorithm to achieve the highest signal-to-noise ratio. The experiments were conducted using a JEM- ACE200F (JEOL Ltd.) equipped with SAAF detector, operated at 200 kV. HAADF and BF images were acquired with convergence semi angle 25 mrad, probe current 58 pA, which (approximately 1.3×10^4 electrons/$Å^2$), and collection semi angle 0-12 mrad (BF) and 46-147 mrad (HAADF). The OBF image was observed with convergence semi angle 6.9 mrad, and probe current 15 pA, and collection semi angle 1.6-3.5 mrad (approximately 2.5×10^2 electron/$Å^2$). The electron dose for OBF is 50 times lower than HAADF and BF imaging in this experiment. The cross section thin film was prepared by JIB-PS500i (JEOL Ltd.).

Results and discussion

The STEM-OBF technique demonstrate clear advantages for the observation and analysis of beam-sensitive SiON layers. STEM-OBF method provide high-contrast images even under low-dose conditions, enabling stable and reproducible visualization of SiON layers without significant beam induced degaradation[2)]. The resulting images exhibited a markedly higher contrast than conventional HAADF and BF image, allowing more reliable evaluation of dielectric layer thickness. Furthermore, a low-pass filtering process was applied to the OBF images to effectively

suppress high-frequency components originating from the amorphous structure within the SiON film.This post processing step improved edge uniformity and measurement repeatability, leading to more consistent CD determination across multiple sites. Fig. 2. shows the CD measurement result of HAADF and lowpass filtered OBF image are almost same. Our result shows the OBF CD measurement results has same CD results with higher contrast than HAADF image. Overall, the combination of low dose OBF imaging and adaptive frequency filtering provide reliable, non-destructive metrology of fragile dielectric films in advanced logic and memory devices.

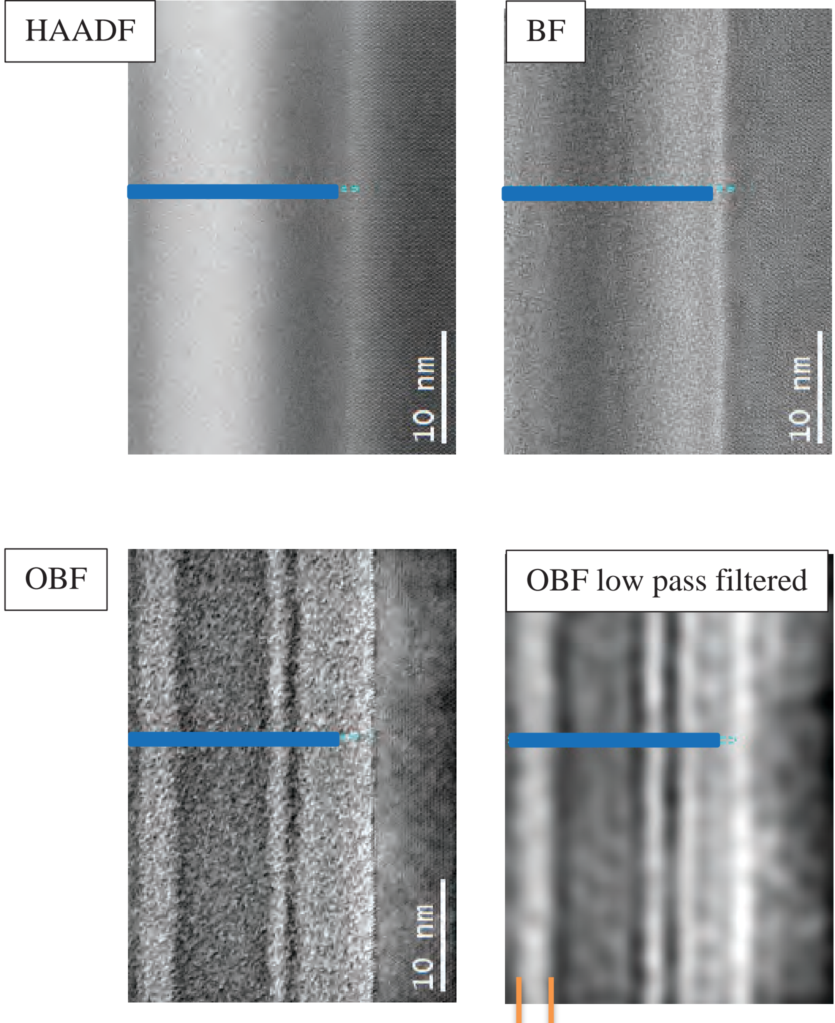
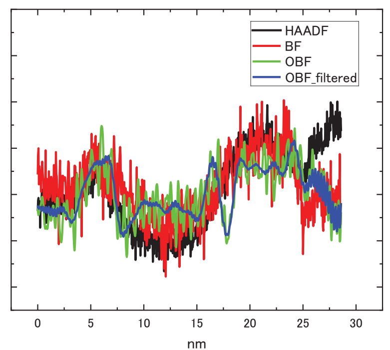


Fig. 1 STEM image of HAADF, BF, OBF and low pass filetered OBF
(orange line shows SiO_2 layer, Blue line means the line profile position)



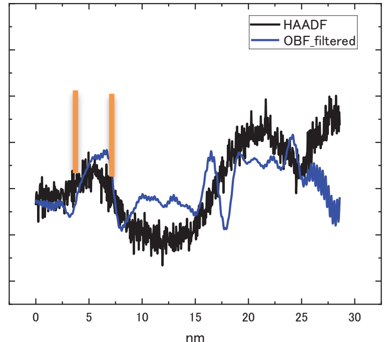


Fig. 2. line profile extracted from each image with jsut10 pixel (HAADF image was multiplied -2.5 times, and BF image was multiplied twice for comparing the thickness of the film, orange line shows also SiO_2 layer)

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KEYWORDS

SiON, low contrast, STEM-OBF, low dose

Advanced Synchrotron X-ray Characterization for Overcoming Manufacturing and Performance Challenges in the Semiconductor Industry

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Semiconductors play a crucial role in modern society, with applications spanning multiple industries, including computing, communications, consumer electronics, automotive, healthcare, energy, and artificial intelligence. However, the advancement of semiconductor technologies is often hindered by performance and manufacturing limitations, such as material constraints, thermal management, interconnect delays, power limitations, and design complexity. Alternative methods for advanced characterization of semiconductor materials can help address these bottlenecks. Synchrotron X-ray facilities like the Stanford Synchrotron Radiation Lightsource (SSRL) offer multi-scale structural characterization, ranging from Ångstrom to millimeter length scales and from tens of picoseconds to multi-hour time scales. The diverse range of X-ray techniques and capabilities available at SSRL presents a unique opportunity to engage the semiconductor industry and tackle key challenges that limit materials and device research, development, integration, and manufacturing. This poster will highlight current progress and future prospects for advanced characterization throughout the semiconductor lifecycle. Synchrotrons have previously facilitated ultra-sensitive structural, electronic, and chemical analyses, enabling the study of synthesis and film growth, defects (such as dislocations), elemental composition, bonding, and interfaces with high spatial resolution, which is vital for next-generation devices. Techniques like X-ray absorption spectroscopy (XAS) uncover electronic states, photoelectron spectroscopy (PES) maps band structures at surfaces, and X-ray diffraction (XRD) visualizes crystal defects, often during processing to understand real-time behavior. Current priorities at SSRL include the development of high-throughput, robot-automated data acquisition and analysis for autonomous structural characterization; the use of in situ and operando methods for real-time monitoring of structure and performance; and multi-modal characterization. Additional discussion topics will include new access models, the potential for dedicated beamlines, and advancements in metrology.

Keywords
Synchrotron X-ray, Advanced Characterization, Semiconductors

Quantification of P-doped Si in Advanced and confined Semiconductor Structures Using TOF-SIMS, Orbitrap™-SIMS, and Self-Focusing SIMS

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INTRODUCTION

Accurate quantification of P in doped SiP is a key prerequisite for advanced CMOS architectures, where device geometries progress from blanket films to densely patterned structures, resulting in gate all around (GAA) devices, and complementary field effect transistors (CFET) test vehicles. Classical Secondary Ion Mass Spectrometry (SIMS) approaches, such as magnetic sector (MS) and Quadrupole (Quad) SIMS provide robust P quantification in blanket layers of sufficiently high P-dopant levels in Si, while Time-of-Flight (TOF) SIMS already suffers from severe mass interferences of P with Si-hydride species falsifying quantification results even on blanket samples. Ultimately all these techniques fail to correctly quantify P in Si, when confronted with feature-scale coverage loss, severe 3D topography, and complex material stacks characteristic of CFET processing due to a severe loss of sensitivity. These complex structures present patterned SiP material in a surrounding SiO_x matrix in small pad dimensions, which provides three main challenges to classical SIMS techniques: the presence of another Si source, e.g. SiO_x does not allow to use the most pronounced Si matrix signals, such as Si and Si_2 for quantification, also the presence of dielectric complicates charge compensation for some of these techniques and finally the small pad size required better focus than e.g. MS-SIMS can usually provide and reduces the sensitivity. In this work Orbitrap™-SIMS combined with the self-focusing SIMS (SF-SIMS) principle is presented as a robust and reliable pathway toward reliable P dopant quantification in SiP confined structures surrounded by Si containing matrix. Building on established methodologies for P analysis in SiGe and addressing the intrinsic mass-resolution challenges posed by overlap with Si-hydride species, the high mass-resolving power and high sensitivity of the Orbitrap™ is demonstrated to provide a robust and reliable dopant quantification.

SELF FOCUSING – SIMS CONCEPT

A full description of the SF-SIMS approach is provided in detail elsewhere.[1] In the context of phosphorus quantification in confined SiP regions embedded within surrounding silicon-containing materials such as SiO_x, the same fundamental principles apply (see Figure 1a). In essence, the formation of a secondary ion cluster (for example, SiP or Si_2P) may proceed through either the direct emission mechanism or the atomic combination mechanism.[2] In the direct emission pathway, the detected cluster originates from pre-existing chemical bonds within the SiP region. In the combination mechanism, one could imagine that Si and P species emitted from spatially separated regions—such as SiP and the surrounding SiO_x—might combine above the surface. However, SF-SIMS relies on the fact that cluster formation requires an extremely tight temporal, spatial, and energetic overlap of the emitted species.[3]
Because of this strict requirement, approximately 90% of the atoms contributing to a given cluster originate as first- or second-nearest neighbors at the surface, within <0.5 nm of one another.[3] This means that a cluster such as SiP can only form if both Si and P atoms are emitted from the same local SiP region. If the Si signal originates from the surrounding SiO_x while the P signal originates from the confined SiP volume, the spatial separation prevents their combination into a cluster during emission. Consequently, cluster formation pathways leading to mixed contributions

from distinct regions are effectively excluded. This eliminates the risk of spurious cluster signals that would otherwise obscure the true P concentration within the SiP volume.
Quantification in this context depends on the use of matrix signals that are specific to the analyzed SiP volume. In conventional SIMS, monomeric and dimeric silicon species (Si and Si_2) are often employed as matrix signals; however, their intensity rapidly diminishes beyond Si_2, rendering larger clusters undetectable. Moreover, these signals are generated in both SiP and the surrounding SiO_x, and thus they do not provide specificity for the SiP phase. In contrast, Orbitrap™-SIMS exhibits a lower detection threshold of approximately m/z 50, allowing monomeric and dimeric silicon signals to be excluded. Under these conditions, higher-order silicon clusters such as Si_3, Si_4, and Si_5 are observed with sufficient intensity, and crucially, they are not produced in the SiO_x matrix (see Figure 1b). This renders them unique to the SiP volume and suitable for use as matrix signals. By employing the ratio of P-based clusters such as SiP or Si_2P to these higher-order Si_x ($x \geq 3$) clusters, reliable quantification of the phosphorus dopant concentration within confined SiP regions can be achieved.

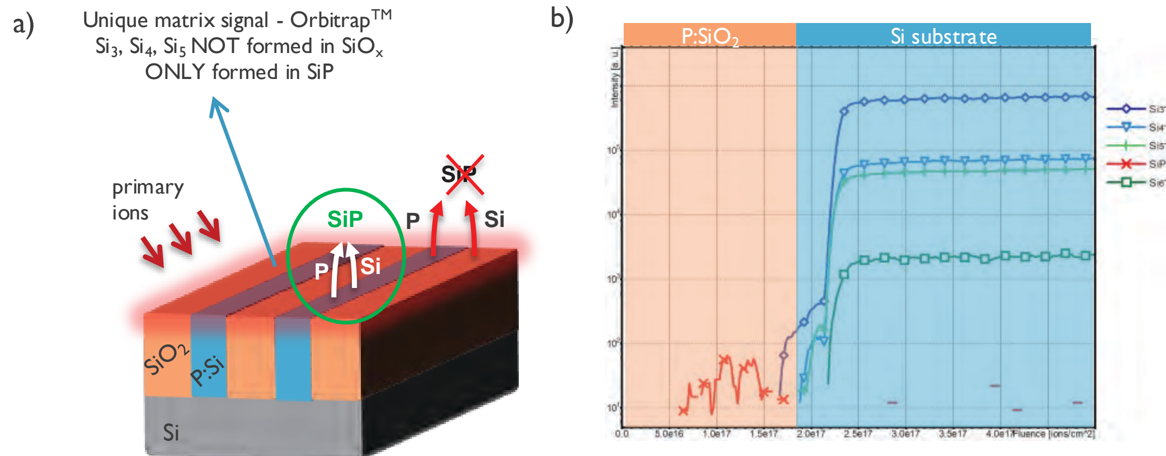

Figure 1 a) Schematic representation of the Self-Focusing SIMS concept for the example of confined SiP lines in a SiO_2 matrix and b) Orbitrap™-SIMS depth profile on a P doped SiO_2 standard on Si substrate.

RESULTS AND DISCUSSION

As a result, SF-SIMS enables reliable compositional analysis in nanoscale, confined SiP regions despite the presence of adjacent Si-rich oxides. Figure 2 shows an example of a pad on a device structure containing active areas with P-doped Si surrounded by SiO_x. The active areas (shown in green in Figure 2 b) are way below the lateral resolution of SIMS techniques therefore a statistical analysis over the whole pad are is required, including active and non-active areas. For the precise P quantification in the active areas only Orbitrap™-SIMS can be applied for the above mentioned reason of small pad size and charging due to dielectric.
By applying the method across many nominally identical features patterned over a large area, SF-SIMS yields statistically robust average composition values derived from comparatively large analyzed volumes. The high count rates produced by this ensemble averaging lead to excellent signal-to-noise characteristics. This statistical advantage is a key strength of SF-SIMS for quantitative process control, especially when compared to high-resolution techniques such as Atom Probe Tomography (APT) or Transmission Electron Microscopy – Energy dispersive X-ray Spectroscopy (TEM-EDX), which probe only single structures and may be impacted by local anomalies such as partially filled, misshaped, or defective features, in addition to limited sensitivity imposed by their much smaller analysis volumes.

The result of the analysis is shown in a quantified depth profile obtained with Orbitrap™-SIMS (see Figure 2c). The P is quantified using the ratio of SiP^- to Si_3^- and the known RSF (Relative Sensitivity Factor) value derived from the NIST® SRM® 2133 certified reference material.[4] The P doping level in the SiP is determined to be around 1e21 at/cm^3.

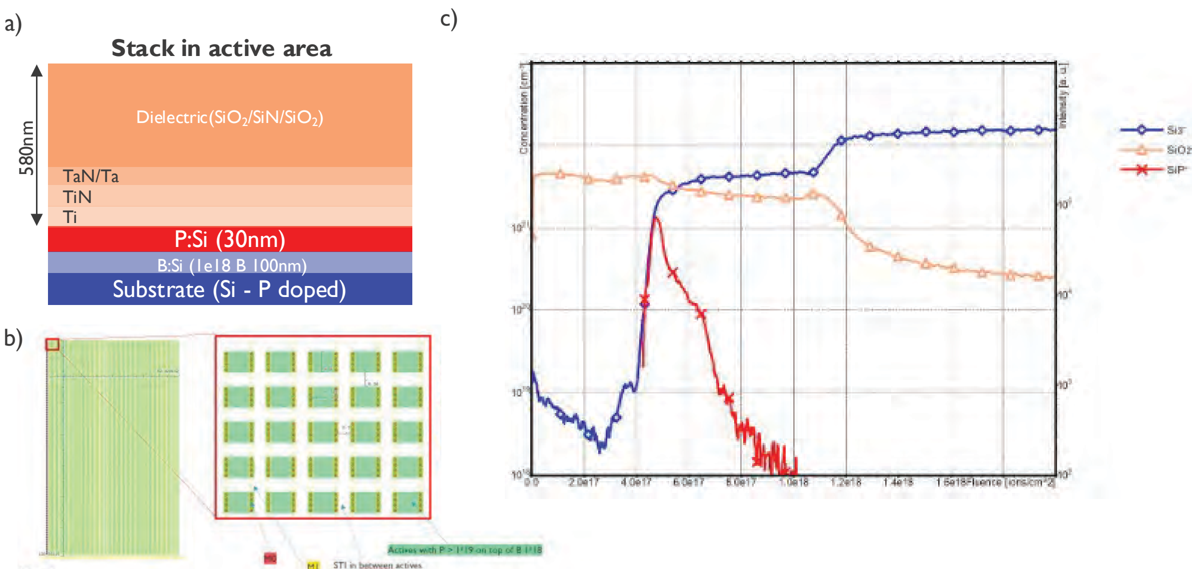

Figure 2 a) Material stack in b) the active areas (green squares), surrounded by SiOx (light orange) of the total analyzed field of view of 40x40 µm² within the pad. c) Depth profile acquired with a 2keV Cs beam in the Orbitrap™-SIMS.

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KEYWORDS

Phosphorous (P) quantification, Silicon phosphide (SiP), Orbitrap™-SIMS, Self-Focusing SIMS, Dopant depth profiling, High mass resolving power

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Surface Enhanced Particle Sizing (SEPS) and Surface Enhanced Raman Speciation (SERS) for on-wafer contamination identification and characterization

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INTRODUCTION

As semiconductor device geometries continue to shrink, traditional contamination control methods face significant challenges. The IRDS Yield Enhancement Roadmap[1] calls out issues due to insufficient metrology for control of particles and critical organics in Ultrapure Water (UPW) and other liquid chemicals. Sub-10 nm particles can present retention difficulties for conventional filtration systems, while particle precursors—dissolved molecular compounds that form particles when dried on wafer surfaces—remain largely unmanaged by current filtration media due to their molecular nature. Further, this type of contamination is invisible to traditional optical particle counting techniques. Novel measurement methods are necessary to address this challenge. This abstract examines novel on-wafer measurement and characterization techniques, called Surface-Enhanced Particle Sizing (SEPS) and Surface-Enhanced Raman Speciation (SERS), for the detection and characterization of contamination in UPW and other liquid chemicals.

SEQUENTIAL SPIN COATING (SSC): TRANSITION FROM LIQUID TO WAFER METROLOGY[2]

The transition from liquid to on-wafer metrology is done with Sequential Spin Coating (SSC). Individual drops of liquid are spin-dried onto a wafer surface as illustrated in Figure 1(a). The rotation speed of the wafer, number of drops, interval between drops and final drying time are automatically set and controlled depending on the liquid. SSC concentrates contamination from the liquid onto the wafer surface, shown in Figure 1(b) as a linear increase in particle concentration with drop count for a 2.4E6 particle/ml solution of Ludox TM50 silicon dioxide (SiO_2) particles in UPW. We have used SSC with UPW, dilute Sulfuric Acid (H_2SO_4), Isopropyl Alcohol (IPA), Hydrogen Peroxide (H_2O_2) and Tetramethylammonium hydroxide (TMAH).

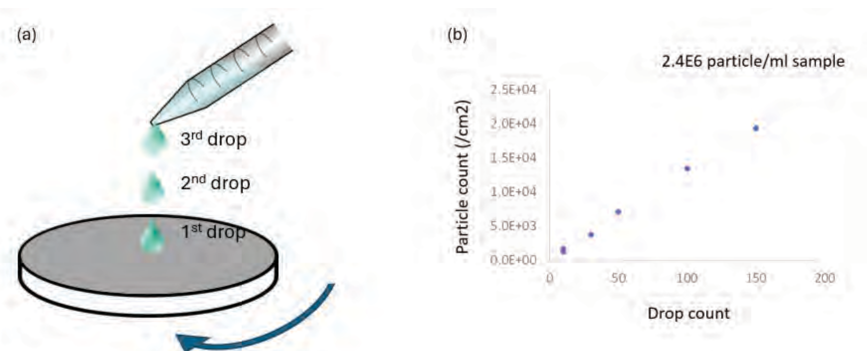

FIGURE 1. (a) Illustration of the SSC technique to concentrate contamination from liquid onto a wafer. (b) Correlation of particle count to drop count for Ludox TM 50 silicon oxide particle in UPW.[2]

SURFACE ENHANCED PARTICLE SIZING (SEPS) AND SURFACE ENHANCED RAMAN SPECIATION (SERS)

The process for Surface Enhance Particle Sizing (SEPS) and Surface Enhanced Raman Speciation (SERS) is shown in Figure 2(a). Starting with an unpatterned wafer with contamination (particles) on the surface, a unique coating is added to the wafer whereas the growth and morphology of a metal film leads to the formation of "optical antenna" on every contamination (particle) site. When resonated by a light source, the optical antenna create localized surface plasmons, enhancing the Rayleigh and Raman optical scattering, resulting in orders of magnitude signal-to-noise improvement as shown for SEPS in Figure 2(b-c). The combination of SEPS and SERS provides particle size, location on wafer, morphology, and molecular fingerprint.

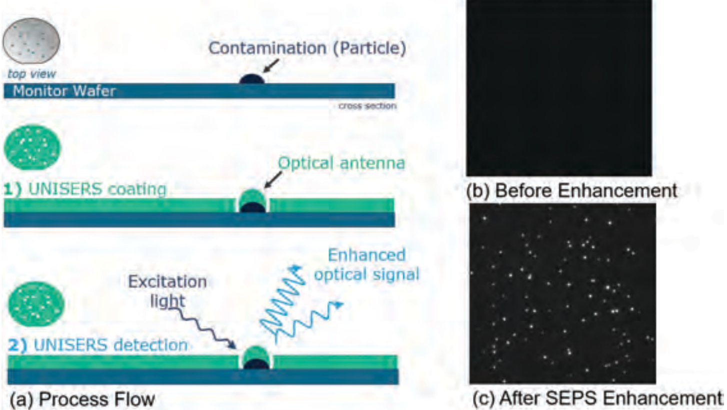

FIGURE 2. (a)Two-step SEPS and SERS process flow. Example darkfield microscope images (b) before enhancement and (c) after SEPS enhancement.

SEPS on Silicon Dioxide (SiO_2) in UPW[3]

To characterize SEPS performance, three different sizes of SiO_2 particles were suspended in UPW and spin-dried on an unpatterned silicon wafer using SSC. The three particles used in this experiment are Ludox SM with a nominal size of 8nm, Ludox HS with a nominal size of 15nm and Ludox TM with a nominal size of 30nm. The wafer was then coated and imaged using the SEPS process described in the previous section. Particle count vs size is shown in Figure 3. The expected Gausian shaped size distributions are detected for HS and TM. SM is at the edge of the current SEPS detection limit and only half of the normal gaussian size distribution can be detected. More work will be done in the future to push the SEPS technique to detect smaller sized particles.

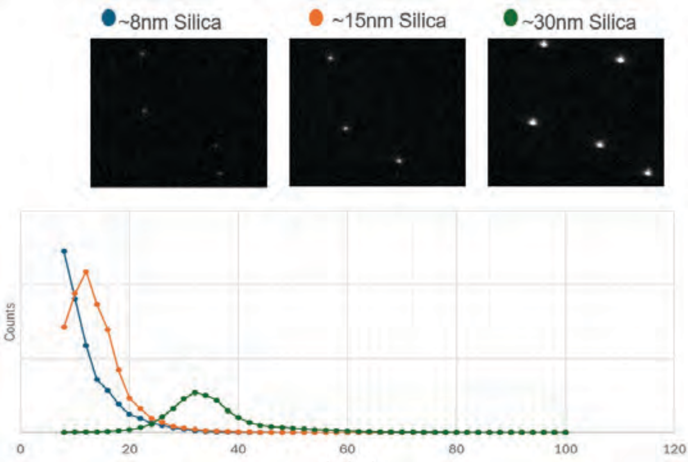

FIGURE 3. SEPS of Ludox SM, TM and HS silicon dioxide (SiO_2) particles on an unpatterned silicon test wafer.[3]

Posters

SERS on UPW with Sulfonated Polystyrene Resin Leachates[4]

Sulfonated polystyrene is a resin material used for trapping ions during the UPW purification process. Ion exchange resins can also release unwanted leachates or particle precursors into the UPW. In this experiment there are two liquid samples, UPW control (As Received) and UPW with the ion exchange resin leachates (UPW Residue). Each liquid sample was drip-dried onto its own clean silicon wafer. SERS was collected on particles sized 50nm and larger from both wafers. The As Received sample does not have any significant spectral peaks. The UPW Residue sample has spectral peaks indicating SO_4, C_6-Ring, SO_3, and SO bonds indicative of styrene and sulfonate.

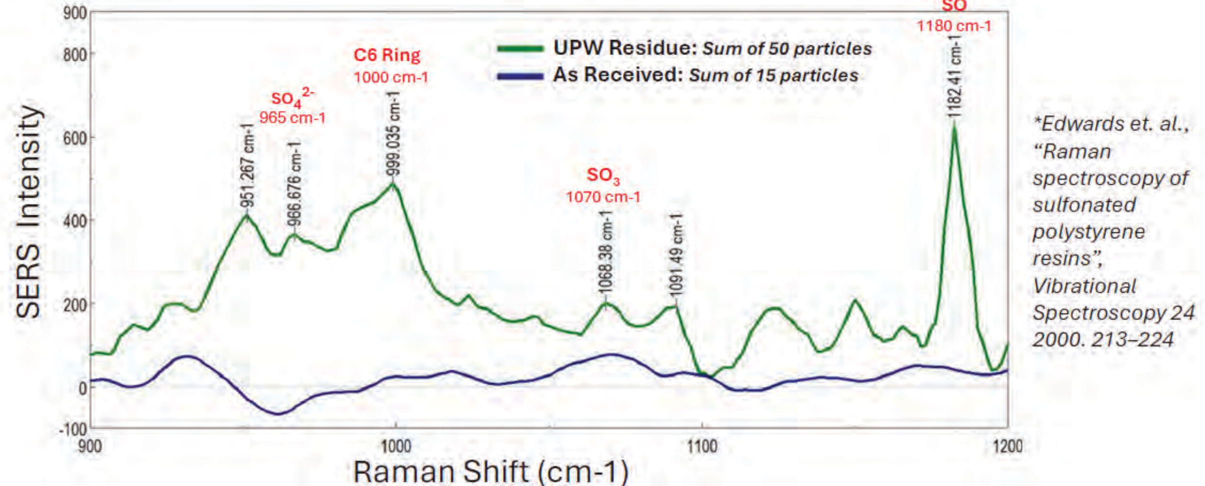

FIGURE 4. SERS intensity vs Raman Shift (cm^{-1}) for the "as received" control sample and the UPW residue sample.[4]

CONCLUSION

In this abstract we have introduced the novel measurement method of SSC combined with SEPS and SERS for on-wafer detection and characterization of liquid defectivity. We have shown examples of SEPS and SERS experimental data and provided a path towards closing the metrology gap for the detection and characterization particles and particle precursors in UPW and other liquid chemicals.

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KEYWORDS

Novel Measurement Methods, SEPS, SERS, Raman, Liquid Defectivity, Particle Precursor

Towards Direct Measurement Of Chemical Noise In EUV Resists: Dose Dependent IR-AFM Measurements

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INTRODUCTION

With the move to high-NA EUV lithography, resist performance is becoming a critical and potentially performance limiting aspect in the lithography process. The performance of resist may be critical as regards the final dimensions and quality (roughness) of the written patterns. Diffusion processes during the development phase may not only cause loss of sharpness but may also act to reduce roughness. Additionally, there are concerns that at the small scales that are becoming accessible with high-NA EUV, chemical stochasticity may start to cause noise and, finally, roughness in the written patterns. Secondly, understanding resist performance is also crucial to ensure that the resist is well activated, to produce a defect free pattern at the lowest possible dose, to both reduce energy use and optimize throughput of the lithography process.

Traditionally, it has been difficult to obtain insight into the exact mechanisms at play within a photoresist layer from exposure to development. The relevant chemistry has been studied in bulk material using optical spectroscopic methods (1), but it has been difficult to access resist chemistry and properties at relevant length scales for lithography and within the thin layers used by high-NA EUV workflows. Recently, some techniques have emerged which enable a window on processes in the resist, namely soft x-ray (2), PEEM (3) and IR-AFM (4, 5). All techniques hint at chemical heterogeneity at nm length scales and a need to understand and control the process of photoresist development in the context of nm-scale patterns. It appears that the interplay between chemical heterogeneity and diffusion throughout the development process may be key to optimize resists further to achieve finer line pitches with less defectivity. All these techniques are, however, still low in technology readiness level and are primarily research lab techniques. Here, we will present our results on reproducible dose-focus matrix measurements using IR-AFM of a EUV resist. We will show how different chemical species within the resist are activated upon exposure depending on dose. We will pay special attention to reproducibility of these measurements and what may be needed to implement such dose-focus matrix measurements as a calibration tool in a fab environment, paving the way for IR-AFM to become accepted as a valuable metrology tool in the production line.

SYSTEM AND METHODS

To perform IR-AFM on the samples, we used a commercial Vista One system by Molecular Vista equipped with a Block Engineering QCL mid-IR laser in its standard PiFM operating mode (7) with NCH-PtIr PiFM cantilevers. However, special care was taken to ensure the tips were clean and not subject to wear or degradation. We also made sure settings resulted in comparable signals and contrast levels between different experimental runs, samples and tips.

The topography images are processed using line-by-line z drift corrections and the remaining xy-stage-related slope is corrected using a two-point background line subtraction using Matlab. No image processing is done on the PiFM images. IR-spectra and their locations are extracted using SurfaceWorks. A gaussian smooth filter has been applied to the spectra. Resist samples were exposed according to industry standards at various exposure doses on an EUV NXE scanner.

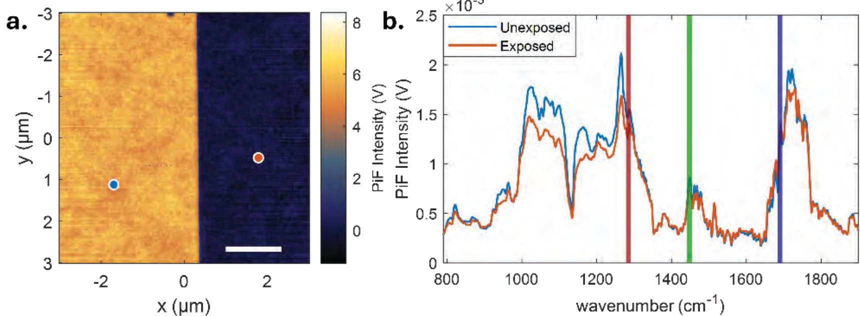

FIGURE 1. **a.** Topography image and **b.** IR spectra of resist near the edge of a flood exposure region. The exposure caused a significant change in film thickness even without development, leading to a clear edge in the topography image. Spectra on both the exposed and unexposed areas reveal chemical differences that can be related to the PAG as well as the polymer backbone.

RESULTS

Measurements were performed in an area containing a flood exposure, without fine scale patterns. We focused on areas at the edge between EUV-exposed and unexposed areas. Figure 1.a shows a representative image on a sample with a dose of 24.4 mJ/cm^2. We observe that the exposed film has shrunken and there is a step height of roughly 5.4 nm between the exposed and unexposed resist. We acquired IR spectra on both exposed and unexposed areas shown in figure 1.b., which present features related to the resist chemistry. The interpretation of any differences between the spectra is however hampered by the observation that the overall intensity of the spectra changes for subsequent iterations. We speculate that this is because of heating of the area under the tip and subsequent tip contamination. This supports the importance of carefully optimizing IR-AFM measurements and spectrum acquisition on soft materials like resists.

It turned out that PiFM imaging at selected wavenumbers gives more robust information, likely due to a limited acquisition time at every tip location, limiting heating and contamination effects. The wavenumbers chosen for imaging are marked by the colored vertical lines in figure 1.b. The red line corresponds to the specific SO_3^- group of the photo-acid generator at 1285 cm^{-1}, the green line corresponds to the CH2 of the protection group at 1448 cm^{-1} and the blue line corresponds to the C=O bond of the carboxylic acid after exposure at 1690 cm^{-1}. In Figure 2, we show a set of PiFM images at the three wavenumbers for two samples with different doses. Figure 2.a-c shows PiFM images for a dose of 24.4 mJ/cm^2 while Figure 2.d-f shows PiFM images for a dose of 17.5 mJ/cm^2. Figure 2.a and 2.d show increased signal, on average, on the exposed area, as expected for the SO_3^- group of the PAG. Figure 2.c. and 2.f show a similar pattern, consistent with the C=O bond being formed after exposure. We note that, while we can get an averaged signal on the exposed area higher than the averaged signal on the unexposed area for the 1285 cm^{-1} wavenumber, the signal difference is small enough to not show the cross pattern present in the other PiFM images. The topography acquired simultaneously to the Figure 2.d. does show the cross. The PiFM images related to the protection group in Figure 2.b and 2.e consistently shows a higher intensity of the PiF signal on the unexposed area rather than in the exposed area.

In order to quantify the differences of the PiFM intensity we calculated the average signal level in both the exposed and unexposed regions. Then, we defined the asymmetry $\alpha = \frac{A_{Unexposed} - A_{exposed}}{A_{Unexposed} + A_{exposed}}$. The result of this analysis is shown in Figure 2.g. For the C=O bond of the carboxylic acid, we see a clear evolution of the asymmetry with dosage, where it becomes more negative as the dose increases. The same can be said about the asymmetry for the SO_3^- group of the photo-acid generator but in a weaker way. For the CH2 of the protection group, we can see that no well-defined increasing or decreasing trend can be observed within the measurement uncertainty.

We note that the spread of the asymmetry points for the same dose is significant, and we should note that these variations can be attributed to tip apex alterations. This data has been acquired using a single cantilever of which the tip ultimately aged, because of interactions between the tip and the sample. The consequence is that the tip apex changed in its shape but also in its chemical composition because of contamination. This shows that, in order to push

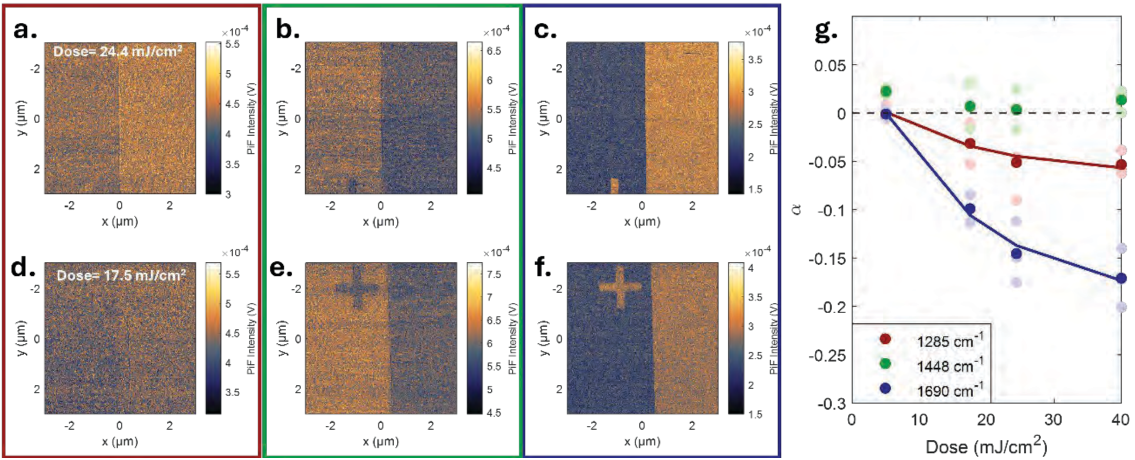

FIGURE 2. a-c. PiFM images on a sample with a dose of 24.4 realized at the wavenumbers 1285 cm^{-1}, 1448 cm^{-1} and 1690 cm^{-1}. **d-e.** Same but on sample with a dose of 17.5. [Parameters: Drive amplitude: 0.8 nm, Setpoint: 75%, size: 6 µm by 6 µm, Laser power: 5%] **g.** Plot of the extracted asymmetry of the PiF intensity between unexposed and exposed area for the three probed wavenumbers. The hard colored dots correspond to the average of the lightly colored dots. An exponential fit of the averaged data is also plotted for 1285 cm^{-1} and 1690 cm^{-1} using the same decay rate parameter.

the reliability of the IR-AFM metrology forwards, there is a need to focus on the tip-sample interactions and characterization of the tip apex during experiments such as this one.

By using IR-AFM and more specifically PiFM imaging, we have shown that we can extract information about specific chemical groups on a resist sample with EUV-exposed and unexposed areas. Additionally, we can observe a dose dependance of this chemical information and rationalize it. This is another example that demonstrates that IR-AFM is a powerful metrology for resist characterization despite a number of sample dependent challenges that need further development and optimization of the IR-AFM metrology.

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KEYWORDS

Resist chemistry, EUV exposure, IR-AFM

High-resolution Scanning Thermal Microscopy for Nanoscale Temperature Mapping of Operating Microelectronic Devices

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INTRODUCTION

Effective thermal management is essential for optimizing the performance and reliability of micro- and nano-electronic devices. Localized heat generation and nanoscale hot spots can strongly influence charge transport, power dissipation, and long-term stability of miniaturized functional electronic devices[1-3]. Quantitative temperature mapping at the nanometer scale is therefore critical for understanding and engineering thermal phenomena in operating devices. However, conventional approaches such as Raman thermometry, infrared and near-field optical thermometry or standard scanning thermal microscopy often suffer from diffraction limited resolution, artifacts caused by poorly defined tip–sample thermal contacts, and parasitic heat paths[4].

Picowatt-resolution Scanning Thermal Microscopy for Quantitative Temperature Mapping

In this work, we present a high-resolution scanning thermal microscopy platform that enables nanoscale temperature mapping of operating electronic devices. The system employs a custom single-feedback SThM probe operating solely on the thermal signal from the thermistor on the tip to continuously balance the probe temperature against that of the sample, eliminating the need for auxiliary topographic or electrical feedback loops which could potentially induce irregular thermal contacts particularly across abrupt topographical variations such as steps, bumps, or edges. We demonstrate that this technique can quantitatively map surface phonon temperature fields of operating nanoelectronic devices with sub-10 nm spatial and <100 mK temperature resolution. The method is highly robust even in complex device geometries and accurately captures true local temperature distributions without distortion from abnormal probe–sample contact and surface contamination. Representative results reveal well-defined nanoscale thermal gradients and dissipation hot spots that would typically require extensive post-processing to correct for contact thermal resistance in conventional SThM.

This high resolution SThM offers a flexible platform for probing energy transport phenomena at the nanoscale. Through quantitative, high-resolution mapping of surface phonon temperatures under steady-state conditions, this technique opens new possibilities in exploring non-equilibrium heat dissipation, hot-carrier dynamics, and phonon–electron coupling in a broad range of functional materials and quantum systems. Its ability to perform reliable thermal

mapping on complex topographies without crosstalk from electrical or topographic feedback makes it uniquely suited for investigating emerging electronic and thermal materials, where thermal transport often exhibits unconventional signatures. In particular, this approach can provide direct insight into edge-state heat flow in anisotropic phonon transport and energy dissipation pathways in semiconductor devices. It can also provide real time phonon imaging on nonlocal heat conduction and phonon propagation in nanoelectronic devices, where classical diffusive models are invalid. Its application potential spans from high-power nanoelectronics and plasmonic devices to quantum thermodynamic systems and low-dimensional materials, offering a universal platform for improving the understanding of nanoscale heat and energy transport.

Results

The optical microscope image of our customized-fabricated probe is summarized in Fig. 1a, with the phonon temperature mapping schematics shown in Fig. 2b. The customized fabricated SThM probe features a patterned NbN line with high TCR integrated on top of a dielectric cantilever (SiO2) which provides low thermal conductivity (10-W/K) to increase the temperature resolution of the probe[5]. The tip of the probe is patterned through standard lithography methods and further milled by focused ion beam with a final tip radius ~80nm to increase the spatial resolution. The probe is manipulated by a 3-axis high precision piezo during our modified null point mapping scheme. During each point, the current (temperature) of the NbN line will be dynamically adjusted to identify the current value where there is zero heat flux between probe and tip (corresponding to equal probe and sample temperatures). This self-balancing feedback ensures that the measured signal directly represents the local surface temperature without requiring calibration against an external reference. A vertical compensation drift is simultaneously applied to the z piezo actuator to preserve a constant and minimal thermal contact resistance on the order of a few nW/K between the tip and the sample. This can ensure the probe achieves sub-10 nm spatial resolution while maintaining high thermal sensitivity, allowing reconstruction of nanoscale temperature gradients and dissipation features even across complex device geometries.

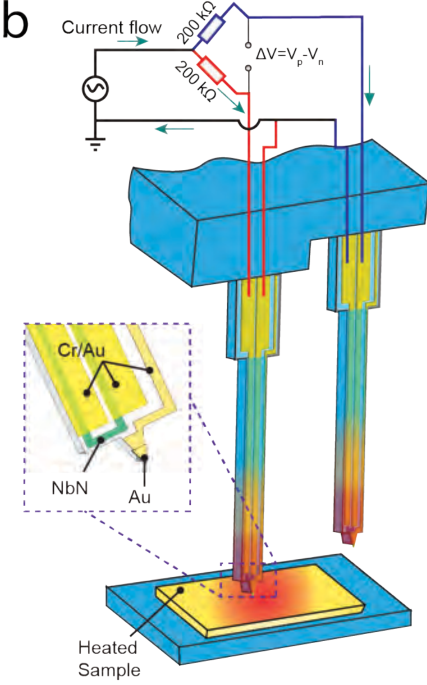

FIGURE 1. Optical microscope image and schematics of the custom-fabricated high-resolution scanning thermal microscope.

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KEYWORDS

Scanning Thermal Microscopy (SThM), Nanoscale Thermometry, Nanoscale Hot Spots, Operating electronic devices, Artifact-Free Thermal Imaging

Posters

A Conformal PEALD-SiN_x Coating for Suppressing Mesa-Induced Leakage in GaN Vertical SBDs

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INTRODUCTION

Gallium Nitride (GaN) vertical power devices are pivotal for next-generation high-voltage applications. A critical challenge in their fabrication, particularly for devices utilizing deep mesa etch termination (DEMT) for field management, is the severe surface damage and trench-like defects induced by aggressive etching processes.[1] These defects become dominant leakage paths, severely degrading breakdown voltage and preventing the realization of ideal avalanche breakdown. Conventional dielectric deposition methods like plasma-enhanced chemical vapor deposition (PECVD) struggle to conformally cover these high-aspect-ratio features, leading to interfacial voids and inadequate passivation. [2]This work presents a microfabrication strategy to overcome this limitation by employing plasma-enhanced atomic layer deposition (PEALD) for conformal silicon nitride (SiN_x) passivation. We clearly demonstrate that PEALD-deposited SiN_x provides excellent passivation of defects in DEMT structures by effectively mitigating etching-induced sidewall defects, offering superior interface quality with minimal oxygen contamination, and enabling conformal coverage of high-aspect-ratio features, thereby substantially enhancing the voltage-blocking capability of GaN vertical devices.(Kim et al. 2025)

RESULTS AND DISCUSSION

I. Preparation and Analysis of High-Quality SiN_x via PEALD

We demonstrate the growth of high-quality SiN_x films via an optimized PEALD process using a Si_2Cl_6 precursor under ultra-high vacuum. The process, stabilized at 450°C and 150 W plasma power, yields films with exceptional uniformity (<±1% thickness variation on a 6-inch wafer), low surface roughness (RMS ~0.3 nm), and near-zero oxygen contamination.

The efficacy of this PEALD-SiN_x film was investigated in GaN vertical Schottky barrier diodes (SBDs) with a 6 μm deep mesa. Cross-sectional HRTEM and EDS analysis confirmed that the PEALD-SiN_x provides a conformal, void-free interface, effectively filling etching-induced trenches and mitigating the underlying damaged GaN layer. In stark contrast, PECVD-SiN_x passivation resulted in a defective interface with significant Si diffusion and incomplete coverage. (Fig. c-f)

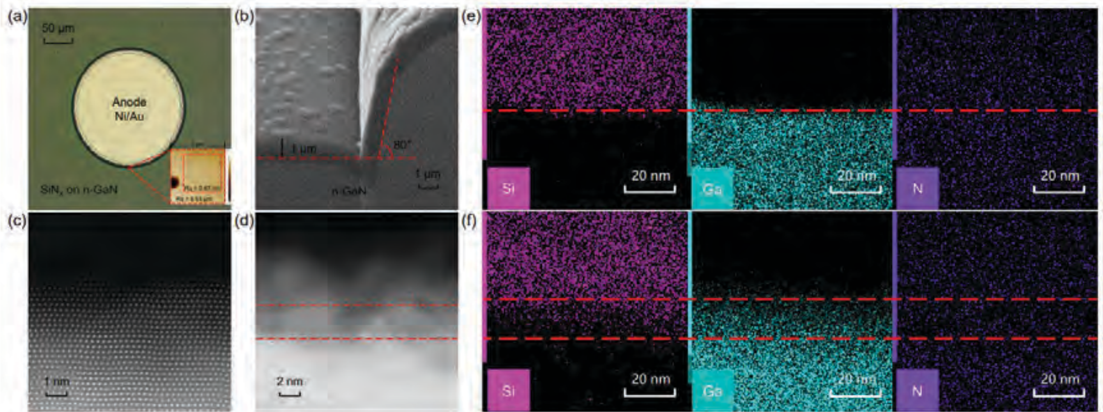

FIGURE 1. (a) Top view image of SBD and AFM image of etched surface after depositing SiNx with a scanning area of 5 μm × 5 μm. (b) Cross-sectional SEM image of the sidewall of DEMT. (c)~(d) Cross-sectional HRTEM image of the interface between SiNx passivation deposited by PEALD or not. (e)~(f) EDS mapping of the interface of SiNx/GaN.

II. Analysis of DC Characteristics of GaN Vertical SBDs

Electrical characterization revealed a transformative improvement in device performance. Fig. 2(a) and (b) show that SBDs passivated with PECVD-SiN_x alone suffered from severe voltage-dependent leakage, reaching nearly 1 mA at just 80 V without breakdown. Conversely, PEALD-passivated devices exhibited a stable, ultra-low leakage current (~10^{-11} A) until a sharp avalanche breakdown at approximately 400 V, a five-fold increase in breakdown voltage and a 10^4-10^5 reduction in leakage. Inter-anode leakage measurements further confirmed that PEALD passivation completely suppressed the sidewall conduction path, restoring bulk-limited conduction.

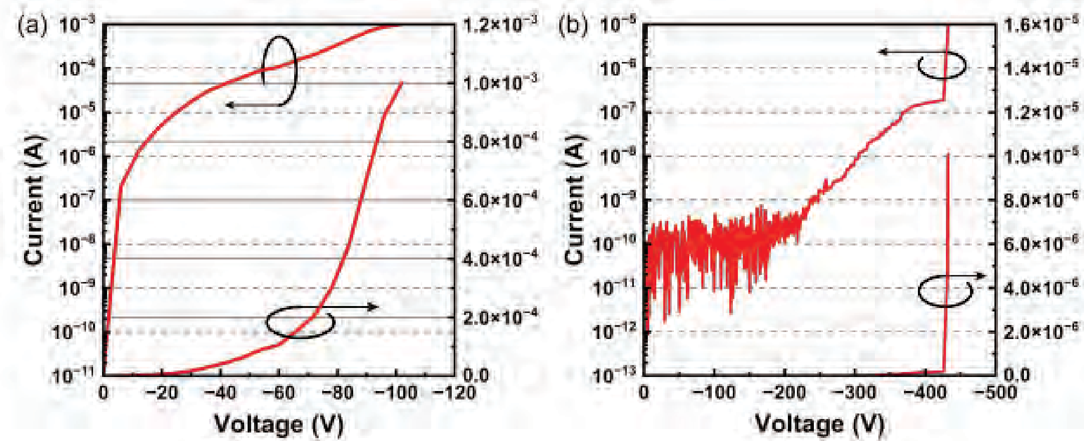

FIGURE 2. (a) Reverse breakdown characteristics of GaN vertical SBD (b) with PEALD-SiN_x passivation or without PEALD-SiN_x passivation in linear and semi-logarithmic scales.

CONCLUSION

In conclusion, this study establishes PEALD-SiN_x as an essential micro-fabrication technology for enabling high-voltage GaN vertical devices. Its superior conformality and interface quality directly address the core challenge of etching-induced damage, unlocking the full voltage-blocking potential of DEMT structures and paving the way for robust, high-performance GaN power electronics.

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KEYWORDS

PEALD, Atomic Layer Deposition, SiN_x, Microfabrication, Vertical Mesa Passivation, Interface Damage, Conformal Coating.

Laser scanning optical photothermal infrared (O-PTIR) microscopy for localization and identification of contaminants with sub-micron spatial resolution and breakthrough chemical imaging speed

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INTRODUCTION

Contamination analysis of modern microelectronics is key to improve manufacturing process. However, it also poses a great challenge due to the chemical complexities and especially when the contaminant size becomes too small. Vibrational spectrum, unique to each compound, could be used to identify chemicals by searching against large spectral database. Recent publications have established the Optical PhotoThermal InfraRed (O-PTIR) technique as a novel, effective solution for contamination feature sizes smaller than 10 µm [1-3].

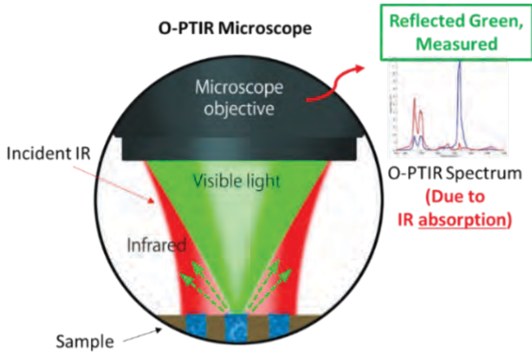

FIGURE 1. Operation principle of O-PTIR and the formation of O-PTIR spectra

The O-PTIR technique enables collection of FTIR transmission-like infrared spectra with Raman-like spatial resolution. This technique employs a “pump-probe” excitation-detection mechanism, where the pump is a pulsed infrared laser illuminating the specimen surface; simultaneously, the probe is a constant wave visible laser in the same space to sense localized photothermal effect from infrared absorption. The use of a visible laser in O-PTIR technique improves the spatial resolution to the size of probe laser’s diffraction spot. Typically, the probe laser is 532 nm, thus leading to a theoretical spatial resolution around 500 nm which is independent of the IR wavelength [1]. The visible probe laser can also serve as a Raman excitation laser for Raman spectra acquisition. The dual use of probe laser makes it possible to collect simultaneous IR and Raman from the same spot without imaging registration. Meanwhile, the setup offers the advantage of non-contact and removes the possibility of sample cross-contamination. Figure 2 shows the laser scanning O-PTIR system for detection of contaminants on a non-IR transparent substrate. The system can be adapted for contaminants on IR-transparent substrate by separating IR and visible laser optical paths as published for another application case [4]. In both cases, the IR and probe laser are synchronized, and their focal planes overlap with each other.

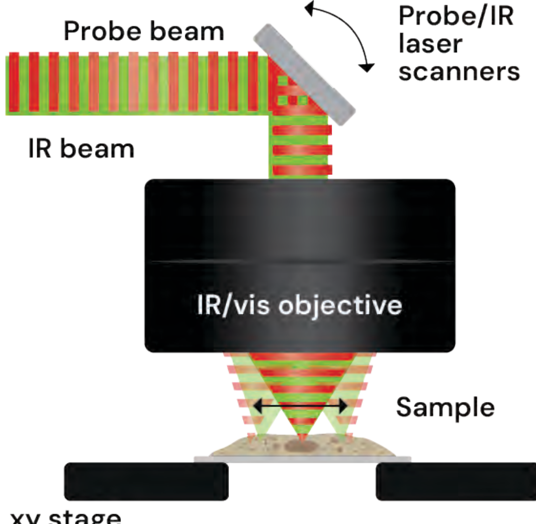

FIGURE 2. Laser scanning O-PTIR microscope setup for contaminates that are not on an IR-transparent substrate

The new laser scanning O-PTIR system uses synchronized fast IR and probe lasers to achieve imaging speeds that are more than 10-fold faster than the previous stage-scanning O-PTIR system. The laser scanning principle improves the imaging speed significantly, reducing hyperspectral imaging time from hours to minutes, and single wavenumber imaging from minutes to seconds. This increased imaging speed makes rapid contaminant detection practical and will improve the quality control in modern microelectronics manufacturing.

MAPPING CONTAMINANTS ON A SURFACE

O-PTIR offers the identification of features smaller than 10 µm. It can be combined with fluorescence imaging for fluorescence-guided IR spectra collection, thus improving the time efficiency [5]. The laser scanning O-PTIR system offers even a higher speed for imaging contaminants within a region of interest (ROI). When O-PTIR spectrum is collected from a point and identified as contaminant, the distribution or coverage of identified contaminant can be of interest. By tuning the infrared laser to the specific wavenumber unique to the contaminant and then reading out the photothermal effect at each step, the system allows mapping the distribution of contaminants on a surface. Figure 3 is an example of mapping the contaminant. For such a experiment (100 µm-by-100 µm, 200 nm step size), it takes 24 seconds to finish a single wavenumber image on a laser scanning O-PTIR system while it takes about 10 minutes on a stage-scanning O-PTIR system. The imaging speed of laser scanning O-PTIR system is almost 30-fold faster in this case.

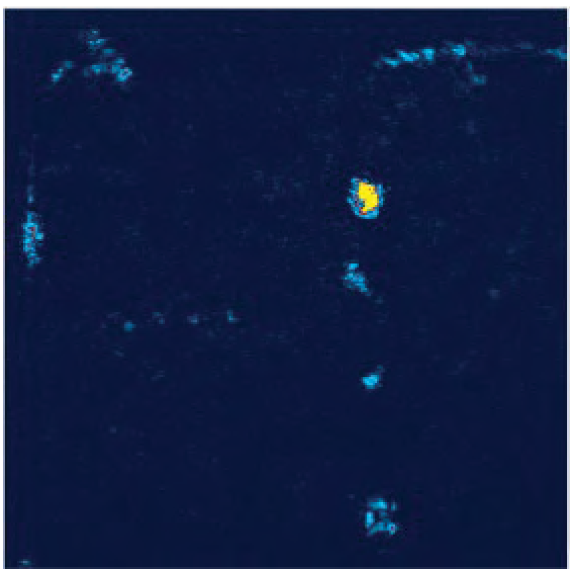

FIGURE 3. Imaging contaminants on a sample surface. The ROI size is 100 µm by 100 µm; Step size for imaging is 200 nm; Pixel dwell time is 80 µs; IR wavenumber for imaging is 1750 cm^{-1}. This image reveals that there are multiple contaminant locations in the field of view that absorbs IR @1750 cm^{-1}.

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KEYWORDS

Infrared, O-PTIR, sub-micron, laser scanning, contamination.

Multi-technique Analysis of Semiconductor Materials

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INTRODUCTION

Advances in semiconductor device performance and reliability increasingly depend on comprehensive material and chemical analysis. This work presents an integrated approach to semiconductor material analysis, leveraging a suite of advanced analytical techniques, including X-ray Photoelectron Spectroscopy (XPS), Angle-Resolved XPS (ARXPS), Hard X-ray Photoelectron Spectroscopy (HAXPES), Ultraviolet Photoemission Spectroscopy (UPS), and Reflection Electron Energy Loss Spectroscopy (REELS), to probe composition, chemical state, electronic attribute, interface property, and energy band diagram. We demonstrate how combining diverse datasets yields information or insights that are not readily available with individual analytical techniques. This information is desirable for driving innovation in device characterization and process optimization.

XPS, ARXPS, AND HAXPES: COMPOSITION, COVERAGE, AND SILICIDE

As semiconductor devices continue to scale down, the compositional depth profile of a thin film or film stack becomes increasingly important. For example, silicon oxynitride (SiO_xN_y) used in both NAND and DRAM cells exhibits low leakage currents and interface defect densities as well as improved electrical stress properties compared to SiO_x and SiN_x. The compositional depth profile of SiO_xN_y largely dictates these properties. As such, accurate and precise compositional depth profiling of thin films or film stacks, such as SiO_xN_y, is highly desirable for understanding, modeling and predicting device physics and performance. Although SiO_xN_y of <2 atomic % N can be profiled using Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS), XPS is better suited for analyzing SiO_xN_y of ≥2 atomic % N. For SiO_xN_y of <80Å thick, ARXPS analysis aided with data modeling is resorted to extracting its compositional depth profile (Figure 1c), which has better accuracy than XPS sputter depth profile with a monatomic Ar^+ beam (Figure 1a) that suffers a preferential sputter of N over Si and improved depth resolution compared to XPS sputter depth profile after adjusting for preferential sputter effect (Figure 1b).

For shrinking semiconductor devices, it is critical to deposit ultra-thin and good quality films such that the film reaches full (100%) coverage at the lowest thickness possible. Moreover, area-selective deposition (ASD) is gaining momentum for fabricating small features that cannot be achieved with traditional photolithography, particularly for 3D structures. An accurate metrology of determining film coverage is thus highly sought. The ion intensity ratio of overlayer to substrate with ToF-SIMS was used for gauging the film coverage. However, the ion yield tends to vary with matrix or coverage such that the resultant “S-shaped” curve often does not reflect the actual coverage. ARXPS aided with data modeling is adopted to quantify film coverage through accounting for different inelastic mean free paths of photoelectrons originating from film and substrate (Figure 2a). Figure 2b displays film coverage vs. thickness obtained by ARXPS + data modeling, showing 100% coverage of the thinnest film can be attained with film-1, while a thicker film is needed with film-2 or film-3 and an even thicker film-0 is needed to achieve 100% coverage on high-k. Figure 2c shows film-1 has the lowest deposition rate among the four types of films. The deposition rate is calculated from the film thickness divided by the number of atomic layer deposition cycles. These observations are not unexpected as a slower deposition typically renders better film coverage.

Owing to the finite escape depth of photoelectrons excited by Al Kα X-ray photons, XPS sampling depth is limited to ≤ 10nm. As such, when analyzing a sample with surface segregation or surface contamination, as-measured elemental concentrations often do not represent the bulk. The challenge is addressed by HAXPES that offers a much greater sampling depth than XPS. Figure 3a shows atomic % Ta by HAXPES vs. the expected value for five tantalum carbide (TaC_x) films in comparison with those from XPS surface scans and sputter depth profiles of the same samples. The HAXPES result agrees well with the expected value while the XPS surface scan appreciably underestimates the Ta content, and XPS sputter depth profiling drastically overestimates the Ta content. The observed overestimate of the C content by the XPS surface scan may be attributed to adventitious carbon contamination and the presence of native TaO_x at the sample surface, while the overestimate of the Ta content by XPS sputter depth profiling is most likely attributed to a preferential sputter of C over Ta. Figure 3b displays atomic % Si by HAXPES vs. Rutherford Backscattering Spectrometry (RBS) data for two boron silicide (BSi_x) films in comparison with atomic % Si obtained

from XPS sputter depth profiles of the same samples. The HAXPES result agrees well with the RBS data while XPS sputter depth profiling appears to significantly underestimate the Si content.

Metal to Si contact used in semiconductor devices tends to exhibit a Schottky barrier although ohmic contact is needed for attaining good conductivity. A thin layer of silicide ($TiSi_x$) or TiSiN at the metal/Si interface is conducive to forming ohmic contact. Although XPS is suited for discerning the bonding state of Si by evaluating the binding energy (BE) of Si2p, the BE of Si2p for silicide is identical to that of elemental Si (Figure 4a), making XPS incapable of differentiating silicide from elemental Si. We developed a HAXPES method of discerning silicide or TiSiN. Figure 4b displays the modified Auger parameter (α') of Si vs. depth obtained by HAXPES aided with Ar^+ sputtering for a N-deficient TiN/poly Si stack, clearly showing the presence of ~1nm $TiSi_x$ layer at the TiN/poly Si interface. The α' of Si is defined as Si KLL kinetic energy (KE) plus Si2p BE. The working principle of this method is based on fundamental physics, i.e., α' of Si varies with polarizability and energy of final state ion in the Si KLL transition with elemental Si and silicide exhibiting distinct polarizability and energy of final state ion in the Auger transition [1].

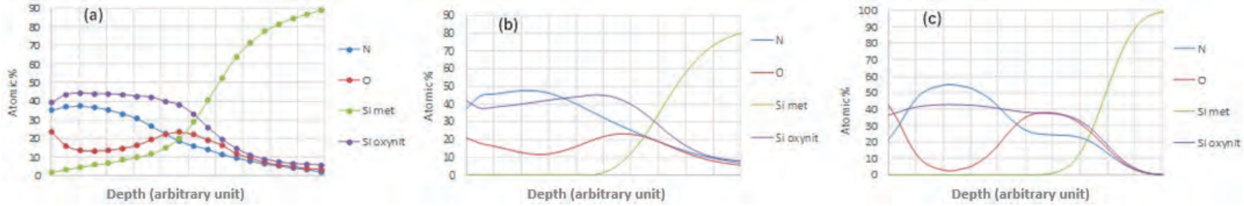

FIGURE 1. (a) XPS depth profile, (b) XPS depth profile after preferential sputter correction, and (c) ARXPS depth profile. Of note, the x-axis depth scale on the graphs in this abstract is deliberately omitted due to confidentiality.

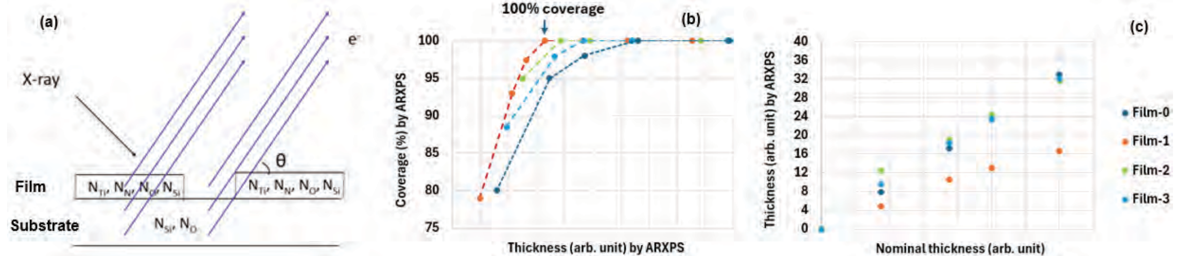

FIGURE 2. (a) ARXPS data contain information on both the thickness and coverage of overlayer, (b) coverage vs. thickness by ARXPS, and (c) thickness by ARXPS vs. nominal thickness for four types of film.

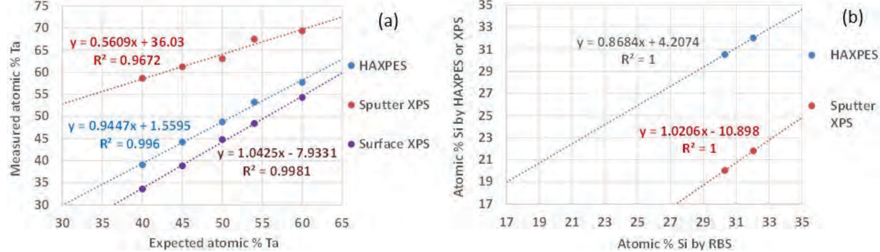

FIGURE 3. (a) Atomic % Ta determined by HAXPES, XPS surface scan and XPS sputter depth profiling vs. the expected value for five TaC_x films and (b) atomic % Si by HAXPES and XPS sputter depth profiling vs. RBS data for two BSi_x films.

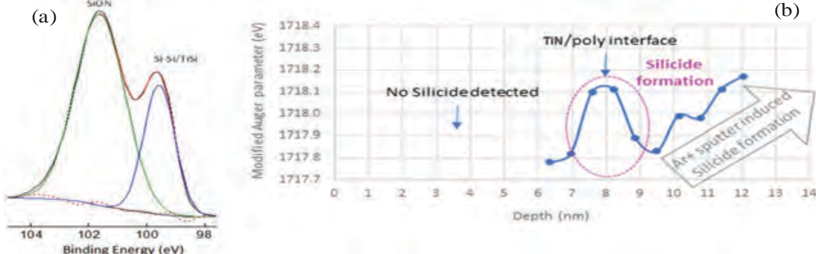

FIGURE 4. (a) XPS Si2p spectrum indicating the presence of SiON and Si-Si or silicide and (b) modified Auger parameter of Si vs. depth determined by HAXPES aided with Ar^+ sputtering reveals the presence of ~1nm silicide layer at the TiN/Si interface.

UPS, REELS, AND XPS: ELECTRONIC ATTRIBUTE AND ENERGY DIAGRAM

Metals, metal-like semiconductors, and dielectrics are ubiquitously used in the semiconductor industry. Besides conductivity, work function is another important quantity depicting the electronic characteristics of metals or metal-like semiconductors (Figures 5a and 5b). Conduction band minimum (CBM), valence band maximum (VBM), and band gap (E_g) are the electronic attributes of metal-like semiconductors (Figure 5b) or dielectrics (Figure 5c). E_g is defined as the energy difference between CBM and VBM. The work function is measured with UPS (Figure 6a), E_g is measured with REELS (Figure 6b), and VBM is measured with XPS (Figure 6c). Figure 5c depicts the energy diagram of a film stack comprised of dielectric, SiO_2 and undoped Si. The E_g and VBM of the three layers are determined with REELS and XPS, from which valance band offset (VBO) and conduction band offset (CBO) are derived. VBO and CBO represent electron and hole barrier heights. With the work function of undoped Si measured using UPS, the electron affinity of each layer is estimated. These quantities determine the energy band lineups related to the conduction mechanism at the material interface. VBO, CBO and electron affinity are tuned for device optimization through varying film deposition or treatment processes.

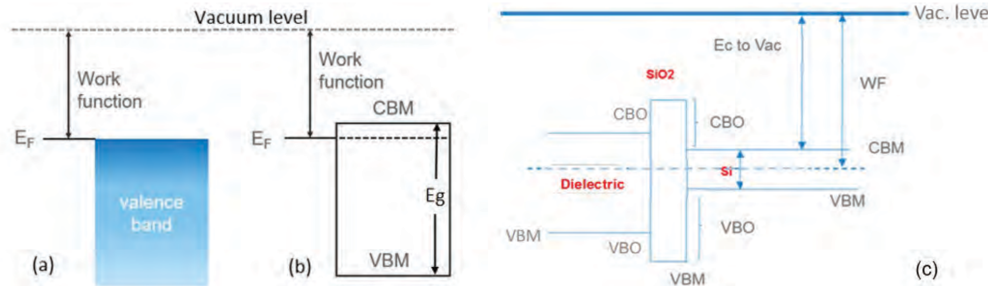

FIGURE 5. Energy diagram of (a) metal, (b) metal-like semiconductor, and (c) a film stack containing a dielectric, SiO_2 and undoped Si.

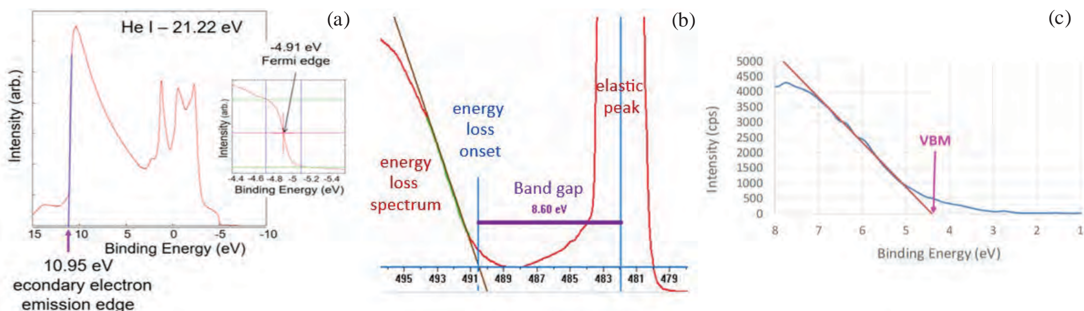

FIGURE 6. (a) Work function measurement with UPS, (b) E_g analysis with REELS, and (c) VBM measurement with XPS.

CONCLUSIONS

While XPS is capable of elemental identification and quantification, chemical state or bonding analysis, and VBM measurement, ARXPS is suited for determining the compositional depth profile of thin films and film coverage. HAXPES enables bulk composition and buried layer or interface analysis as well as silicide detection. REELS is used for E_g analysis and UPS for work function measurement. Combining XPS, REELS and UPS, electron or hole barrier height (CBO or VBO) and electron affinity are determined, thereby the energy band diagrams of film stacks are constructed for modeling and understanding the device physics and performance.

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KEYWORDS

Compositional depth profile, film coverage, bulk composition, silicide, electronic attribute, energy band diagram

X-ray Metrology and Inspection for Advanced CFET Logic and 3D-DRAM

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INTRODUCTION

The semiconductor industry's push to improve power, performance, area, and cost (PPAC), accelerated by AI's demand for compute and memory, increasingly relies on 3D-device architectures and vertical scaling. In logic, gate-all-around (GAA) is evolving toward complementary FETs (CFETs) that vertically stack n- and p-devices using Si/SiGe multilayers; in memory, emerging 3D-DRAM pushes Si/SiGe multilayers to extremes, potentially involving hundreds of layer pairs. Both technologies rely on engineered substrates with epitaxial Si/SiGe multilayers on a Si wafer as the first step in a complex and costly process flow. Per-layer composition (Ge fraction), thickness and interface sharpness are important parameters that set the window for downstream process steps such as critical etches. Many analysis techniques are needed to develop and control such 3D devices [1,2]. X-ray metrology and inspection provide a non-destructive route to accurate and precise control of multilayer structures. We will discuss how recent developments in X-ray techniques can qualify and monitor Si/SiGe multilayers for emerging CFET logic and 3D-DRAM technologies, enabling inline feedback that helps keep PPAC gains on track.

COMPLEMENTARY FIELD EFFECT TRANSISTOR (CFET) LOGIC

The fabrication of CFET devices starts with the deposition of an epitaxial Si/SiGe multilayer on a Si substrate. Individual layer composition and thickness vary by design through the multilayer and must be tightly controlled as they impact steps later in the process flow. A schematic of a CFET structure with an example cross-sectional STEM image is shown in Figure 1.

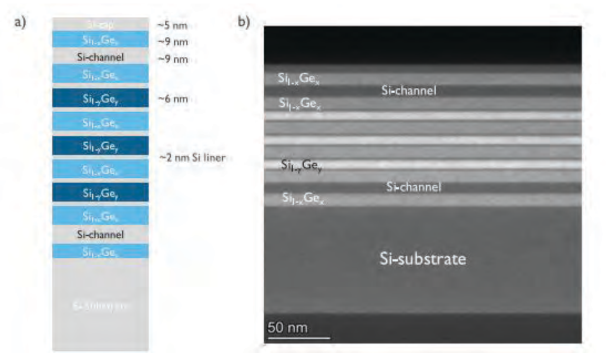

FIGURE 1. (a) Schematic cross-section and (b) cross-sectional STEM image from a Si/SiGe multilayer for CFET devices. Source: Loo et al [3]

Using a Bruker Sirius-XRD inline tool, we measured X-ray reflectivity (XRR) and high-resolution X-ray diffraction (HRXRD) from multiple CFET multilayers with different Ge compositions grown using CVD by imec

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[3]. XRR is most sensitive to individual layer thickness and interface roughness, while HRXRD is most sensitive to lattice parameters and thus SiGe composition. Figure 2 shows representative measured XRR and HRXRD scans with their best-fit simulations. Combining these measurements in a hybrid analysis reduces thickness/composition parameter correlations and improves repeatability.

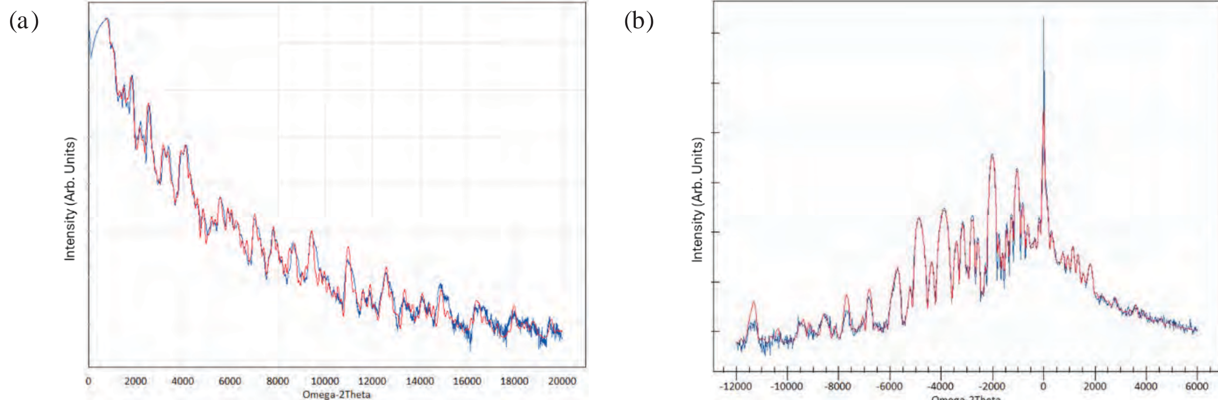

FIGURE 2. Representative data from an epitaxial Si/SiGe CFET multilayer on bulk Si (001): (a) X-ray reflectivity and (b) high-resolution X-ray diffraction ω–2θ scan around the Si (004) Bragg reflection. Measured data in blue; best-fit simulations in red.

From the hybrid analysis, we extract individual layer thickness and Ge composition with sufficient accuracy and repeatability for epitaxial process development and control. The same workflow applies to CFET stacks on bulk Si or SOI substrate, with additional HRXRD alignment as tilt between the thin active Si and the carrier wafer is present. The workflow also extends to backside power delivery integration schemes that incorporate SiGe layers in addition to those in the active device. Additionally, micro X-ray fluorescence (µXRF) can map cross-wafer variations in Ge dose on device wafers at different process steps, providing complementary, rapid screening of composition uniformity across the wafer [4,5].

3D-DRAM MEMORY

Many of the issues that make CFET metrology challenging also apply to 3D-DRAM, but the latter typically employs many more layers, increasing complexity of both growth and characterization. Recent developments enable 3D-DRAM multilayers with hundreds of layer pairs, but with more layers mean greater opportunity for layer-to-layer variation.

XRR only penetrates the upper few hundred nanometers of material and thus cannot access the deepest portions of multilayers several micrometers thick. HRXRD can penetrate the entire epitaxial Si/SiGe multilayer and is sensitive to its average layer properties and also small variations withing the multilayer. These variations can be quantified using a parametric model rather than fitting every layer individually. This approach can conveniently model the progressive thickness drifts reported during long deposition runs [6].

Thick 3D-DRAM stacks are prone to strain relaxation through dislocations and/or crystal lattice undulations that propagate through the stack and can degrade device performance. XRDI rapidly visualizes defects in single crystal materials and is sensitive to early-stage relaxation: linear defects often nucleate at wafer edge and advance toward the center as the Si/SiGe pair count grows. Figure 3 illustrates HRXRD and XRDI on a 120-pair Si/SiGe multilayer grown using CVD on a Si(001) wafer by imec [6]. In the HRXRD scan, variation in the thickness of layers in the multilayer is apparent from the multilayer's diffraction peaks progressive increase in width as the magnitude of the angle increases with respect to the Bragg peak from the Si substrate.

XRDI images, here measured using a Bruker Sensus-600F inline tool, can be analyzed to non-destructively quantify defect distribution within the wafer. In the example image, dark-gray edge regions indicate elevated defect density that diminishes toward the light-gray wafer center; higher-resolution images show a characteristic ⟨110⟩ cross-hatch pattern from strain relaxation in lattice mismatched heteroepitaxial material.

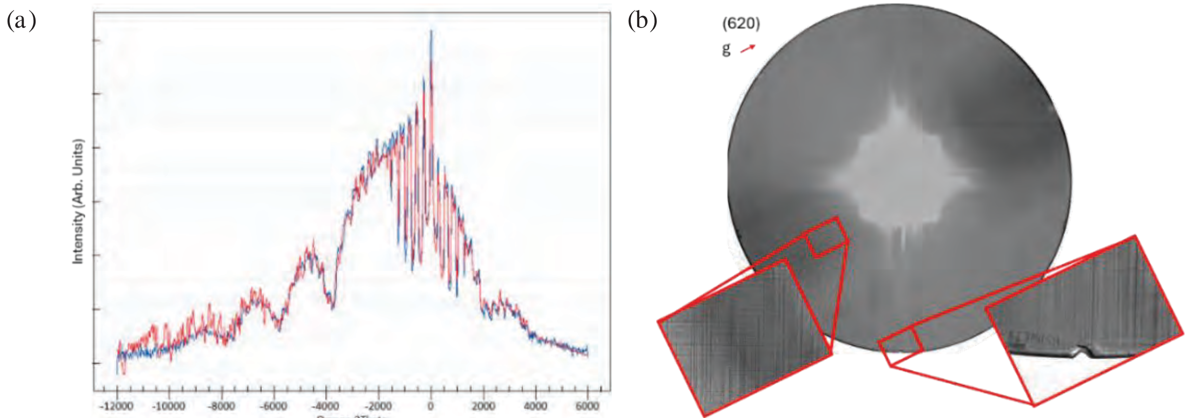

FIGURE 3. Measurements from a 120-pair Si/SiGe multilayer on Si(001) substrate. (a) Representative HRXRD ω-2θ scan around the (004) Bragg reflection at the center of the wafer where there are few dislocations. (b) Transmission XRD images using the asymmetric Si (620) Laue diffraction order of the whole wafer together with high-resolution zoom-ins showing a crosshatch pattern due to a high density of dislocations in the multilayer.

CONCLUSION

As device density continues to rise and structures grow more complex, characterization techniques must keep pace to resolve finer details and subtle variations. X-ray metrology provides non-destructive, quantitative analysis for emerging CFET logic and 3D-DRAM memory based on Si/SiGe multilayers. Used together for CFET multilayers, HRXRD and XRR determine per-layer composition and thickness, and their combined analysis reduces parameter correlations and improves repeatability. For 3D-DRAM, HRXRD provides valuable information on the layer composition/thickness and their variation through the multilayer. XRDI complements these measurements by providing quantitative imaging of the defect distribution across a wafer. Continued developments of X-ray metrology and inspection techniques will help enable future CFET logic and 3D-DRAM memory nodes, helping to sustain PPAC gains through precise, non-destructive, wafer-scale control of increasingly complex Si/SiGe multilayers.

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KEYWORDS

CFET logic, 3D-DRAM memory, SiGe/Si multilayers, X-ray diffraction, X-ray reflectivity, X-ray diffraction imaging

Advanced Packaging Process Control With Micro X-ray Fluorescence

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INTRODUCTION

High-bandwidth memory (HBM) drives multiple technology advancements and is a critical enabler for AI devices such as high-end GPUs, yet it is one of the most challenging modules to manufacture. Advanced packaging for HBM4 and future technology nodes require aggressive micro bump pitch scaling, down to below 10µm diameter to achieve higher interconnect density, enabling increased bandwidth, taller memory stacks, and improved power efficiency [1,2].

This scaling introduces significant complexity in fine-pitch solder deposition, underfill control, and warpage management, while demanding advanced inspection and metrology solutions to ensure reliability and yield at ultra-dense interconnect levels. One of the key metrology requirements for advanced packaging is high precision measurement of silver content in SnAg micro bumps and the thickness of critical metal layers such as nickel, copper, and gold [3].

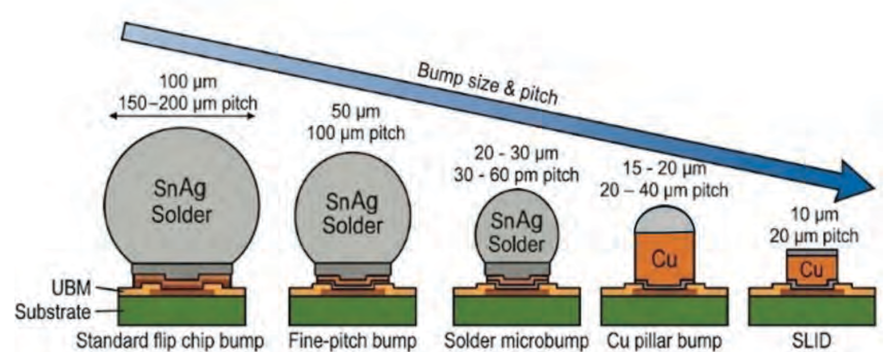

FIGURE 1: Evolution of bump technology, size and pitch (SLID = Solid-liquid interdiffusion bump).

Micro X-ray fluorescence (µXRF) has become an established inline metrology technique due to its ability to measure individual bumps and small metal pads with high precision and acceptable throughput. However, the aggressive pitch shrink in next-generation packaging nodes necessitates metrology solutions capable of measuring smaller bumps and thinner metal layers without compromising accuracy or speed.

TECHNOLOGY

To enable the "single bump metrology" with µXRF, the equipment design (figure 2) must address several important challenges:

Minimize the spot size to match the bumps size decrease while minimizing the X-ray flux outside of the bump. The vertical design is therefore implemented to minimize the spot projection and additionally minimize the sensitivity to height variation. The decrease in x-ray intensity due to reduced material volume with the bump size and thickness

reduction is addressed by careful excitation and analyte line selection. For example, for bump sizes ~15µm and larger, high energy Ag Kα and Sn Kα lines are used to extract solder bump composition and solder height. A tungsten (W) X-ray source is utilized to ensure the high bremsstrahlung intensity that excites the above lines. However, one X-ray source isn't optimal for the whole range of packaging applications. To enable the best excitation conditions and, therefore, the best performance, a dual µXRF configuration is utilized: one µXRF channel with a W source for Sn and Ag and another one with a molybdenum (Mo) source, efficient for gold, copper and nickel excitation.

An array of Silicon Drift Detector (SDD) detectors and state-of-the-art Digital Pulse Processor (DPP) units are used with each source to enable high collection angle and efficient photon counting. Specially designed SDD detectors must are used to provide high quantum efficiency for high energies such as Ag and Sn Kα.

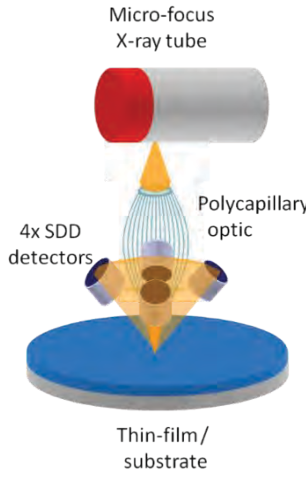

FIGURE 2: µXRF channel schematic for advanced wafer level packaging process control

In addition, production monitoring on 300 mm wafers requires very accurate navigation. Micron level misalignment of the x-ray beam with respect to the bump or the pad results in significant degradation in dynamic precision as well as accuracy penalty. As an example, for a 3 µm mis-positioning of a 10 µm (FWHM) spot on a Ø15 µm bump the Poisson-related error from photon counting uncertainty is 0.3% relative standard deviation (RSD), but the predicted dynamic contribution to the error budget due to mis-positioning of the X-ray spot is 0.82%, thus dominating the error budget. Furthermore, the mis-positioning contributes 11% inaccuracy in thickness or composition measurement. Simulation shows that the navigation error must be < 0.5 µm to enable satisfactory process control.

Analytical methods to extract the net fluorescence intensity for each element of interest include background removal (see figure 3a for the solder bump application) as well deconvolution of overlapping peaks, such as Cu Kα from Ni Kβ (see figure 3b for the metallization application).

Empirical regression is typically used to extract the bump composition and height. The use of the fundamental parameters algorithms (FP) is limited in the case due to the non-planar (and irregular) bumps' shape. An example of the regression equation is:

$$\%Ag = A_0 + A_1 \cdot \frac{I_{AgK\alpha}}{\left(I_{AgK\alpha} + I_{Sn\alpha}\right)} + A_2 \cdot I_{SnK\alpha}$$

where the last term accounts for the bump height variation and Aj are empirical calibration coefficients.

The thin-film FP approach [4] is used for the metallization applications and provides accurate and precise thickness metrology for the double and triple film stacks with few calibration samples needed.

RESULTS AND DISCUSSION

Typical XRF spectra from the solder bump and Cu/Ni/Au metallization layers are shown in figure 3. The low intensity Ag Kα defines the equipment performance in terms of acquisition time, throughout and precision. The

scaling of the bump size and the reduction of silver content further decrease the Ag Kα intensity. Combined with the lower peak-to-background ratio, this is the major challenge in solder bumps metrology. Additional channel implementations are being investigated for bumps below Ø10µm, such as using of the lower energy Ag Lα line, but this discussion is beyond the scope of the current work.

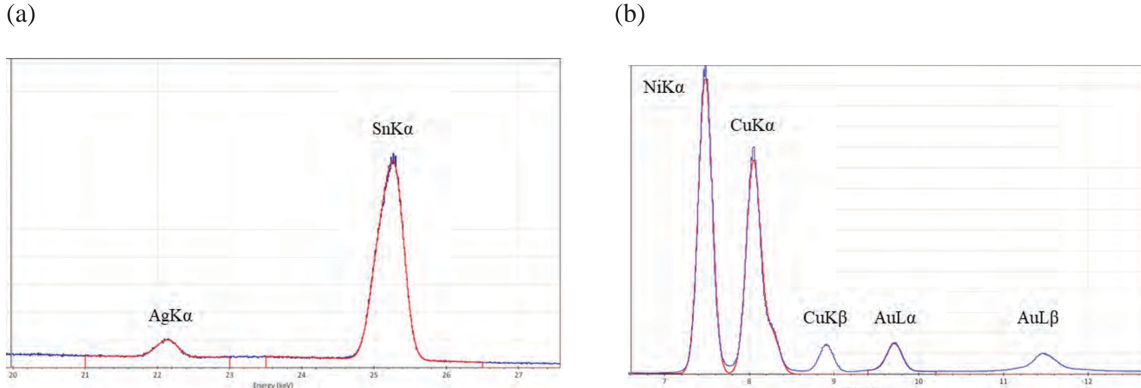

FIGURE 3: Representative measured X-ray spectra (blue) and fits (red). (a) Ag/Sn solder bump and (b) Cu/Ni/Au metallization

The metallization applications present another type of challenge due to the very high fluxes from the micron thick films. These fluxes can cause the system saturation requiring use of filter to control the flux and thus limiting the performance. Modern metrology tools, such as the Bruker Sirius-FW G2 address this issue with the latest high-performance DPP counting electronics.

The performance requirements, in terms of precision, are dictated by the needs of the process tolerances and are typically 3×RSD < 1% for %Ag and bump height (equivalent to the ±10% process tolerance) and even 3×RSD<0.5% for the metals such as Ni or Au (equivalent to the ±5% process tolerance). The performance requirement for longer-term stability is typically similar to dynamic repeatability and requires the use of automated drift correction algorithms to avoid frequent application re-calibration.

Finally, a throughput of at least 10-15 wafers per hour for typical fab sampling patterns is required to maintain the reasonable cost of ownership (CoO).

CONCLUSION

The key metrology challenges of the advanced wafer level packaging applications such as tight control of thickness and composition on ever shrinking solder bumps and back bumps are addressed by the specially designed µXRF metrology channels and tools. The industry roadmap for advanced packaging applications including HBM dictates in turn an aggressive roadmap for metrology equipment development to maintain the required performance in terms of process control and CoO. Technology inflections are expected which will require continued innovation for future process control development.

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KEYWORDS

Advanced Packaging, High Bandwidth Memory (HBM), Micro bumps, X-ray fluorescence (XRF)

Orbitrap™-SIMS for Accurate Quantification of Arsenic in SiGe Across Blanket and Fin-Type Geometries

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INTRODUCTION

Accurate quantification of arsenic (As) in silicon germanium (SiGe) alloys is critical for advanced CMOS technologies, where As acts as a n-type dopant in source/drain regions and junctions [1]. As device architectures evolve from planar to 3D geometries such as FinFETs, nanosheets and cFETs (Complementary Field-Effect Transistor), the integration of SiGe in confined volumes amplifies the need for bulk composition and dopant metrology with high sensitivity and chemical specificity. Conventional microanalysis techniques (TEM-EDX/EELS) are invaluable for structural mapping but fail at technologically relevant doping levels (10^{17}–10^{20} cm^{-3}) due to detection limits and spectral overlaps (e.g., Ge-L vs As-L lines). Similarly, traditional SIMS platforms, such as Time-of-Flight (ToF), quadrupole, and magnetic-sector (MS) analyzers, struggle with severe mass interferences, such as As^- vs GeH^- and $AsGe^-$ vs Ge_2H^-, and insufficient mass resolving power, especially in Ge-rich matrices and patterned features. We implemented Orbitrap™-SIMS combined with Self-Focusing SIMS (SF-SIMS) to overcome these limitations. The Orbitrap™ analyzer delivers >250,000 mass resolving power and sub-ppm mass accuracy, enabling clean separation of critical overlaps in the As/Ge cluster region. Blanket SiGe standards spanning 0–100% Ge and patterned Ge/Si_xGe_{1-x} fins with top-only As doping were analyzed under comparable conditions (Cs^+ sputter beam at 2 keV). SF-SIMS exploits cluster-ion formation (e.g., $AsSi^-$, $AsGe^-$) to confine signals to the feature of interest, filtering out contributions from surrounding materials. Calibration curves for Ge content and As dopant concentration were established using SF-SIMS ratios in the Orbitrap™-SIMS ($Ge_2^-/SiGe^-$ and $AsSi^-/SiGe^-$ or $AsGe^-/SiGe^-$), and allowed the accurate determination of the bulk composition and dopant level in the patterned sample.

SELF FOCUSING – SIMS CONCEPT

A complete description of the SF-SIMS concept can be found elsewhere [2]. Briefly, the formation of a secondary ion cluster (such as AA, AB) can be due to either of the following mechanisms [3]: (1) direct emission model and (2) atomic combination model. While in the first mechanism, the origin of the detected cluster in the sample is obvious (cluster constituents bonded together in the material), one can think in the latter case about the possibility of combination above the sample surface of particles located far away in the material. However, SF-SIMS works on the principle that the formation process of secondary ion clusters, i.e., AA, AB, requires a close temporal, spatial, and even energetic overlap in the emission process of the constituents in order to have a sizeable probability for cluster ion formation [4]. Hence, 90% of the constituent particles of the formed cluster are initially first or second neighbor atoms at the sample surface, i.e., their points of origin are very close together, i.e., <0.5 nm [4]. This is illustrated by the formation of the AB cluster ion as shown in Figure 1, which can only be formed if both A and B constituents

come from the same area. Hence, as the formation of a cluster AB with constituents from different regions (AA and BB) is not possible, no interfering signal is produced masking the composition to be determined. As a result, the problem of lateral resolution of the SIMS method can be overcome and the composition of films grown in confined volumes can be determined (using calibration curves based on specific clusters). In practice, the SF-SIMS is applied on multiple similar structures repeated over a large area and thus provides an average composition value. This averaging over many trenches leads to relatively large analyzed volumes, high counting statistics, and thus a "good signal/ noise ratio." This averaging over many identical features is key to statistically relevant and sensitive metrology (in particular, for process control and monitoring purposes) and a clear advantage compared to high resolution methods (like APT, TEM/EDX) which only measure one isolated structure and may suffer from the accidental analysis of a "defected" area (empty or not entirely filled structures, not ideal shape of the structure) as well as from sensitivity limitations in view of the small analyzed volume.

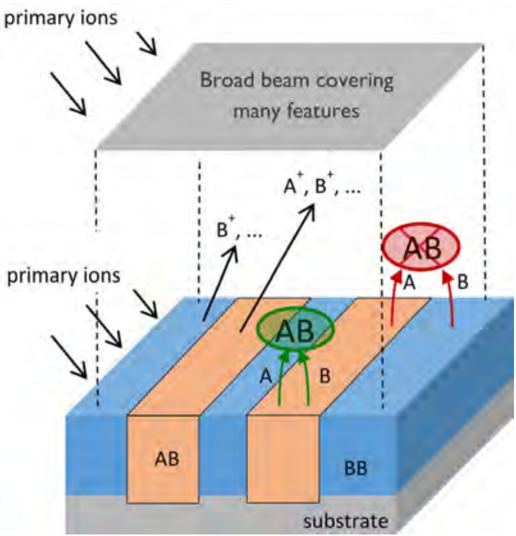

FIGURE 1. Schematic representation of the Self-Focusing-SIMS concept.

RESULTS AND DISCUSSION

Thanks to its exceptional mass resolving power (MRP), we demonstrate that Orbitrap™-SIMS eliminates dominant interferences that compromise conventional SIMS workflows for As dopant in SiGe. For blanket SiGe:As, Orbitrap™-SIMS achieves As detection limits down to 10^{17}–10^{18} at.cm^{-3} and expands dynamic range by >20× compared to ToF-SIMS and MS-SIMS, for which the As detection limit remains overlap-limited near 10^{19}–10^{20} at.cm^{-3}. In patterned sample, i.e. $Ge_{1-y-z}Si_ySn_z$:As on Ge fins, Orbitrap™-SIMS recovers the physically correct top-only As distribution, while ToF-SIMS overestimates by >3× due to unresolved cluster overlaps and inflated backgrounds (see Figure 2). SF-SIMS calibration curves reveal a two-regime strategy: $AsSi^-/SiGe^-$ for Si-rich alloys and $AsGe^-/SiGe^-$ for Ge-rich alloys. These findings confirm that SF-SIMS in Orbitrap™-SIMS provides robust quantification across both blanket and fin-type geometries. This study demonstrates a complete, quantitative route to As dopant level in SiGe that functions across blanket and patterned samples and remains faithful to device reality. Scanning Spreading Resistance Microscopy (SSRM) of the patterned Ge/Si_xGe_{1-x}:As sample confirms the Orbitrap™-SIMS results and highlights the presence of As only at the top of the structure.

In the broader context of device metrology, SF-SIMS in the Orbitrap™ mass analyzer supplies chemically selective dopant profiles at concentrations that matter for junction design, with sufficient MRP to operate in the cluster space that patterned features demand. Looking forward, practical refinements promise even better fidelity for gate-rich geometries like cFETs, such as pushing the Cs^+ sputter energy in Orbitrap™-SIMS measurements into the sub-keV regime to improve depth resolution while maintaining SF-useful cluster yields [5]. This will further stabilize

quantitative dopant metrology in confined fin and gate-all-around structures, ensuring that dopant engineering keeps pace with the architectural innovations of the next logic nodes.

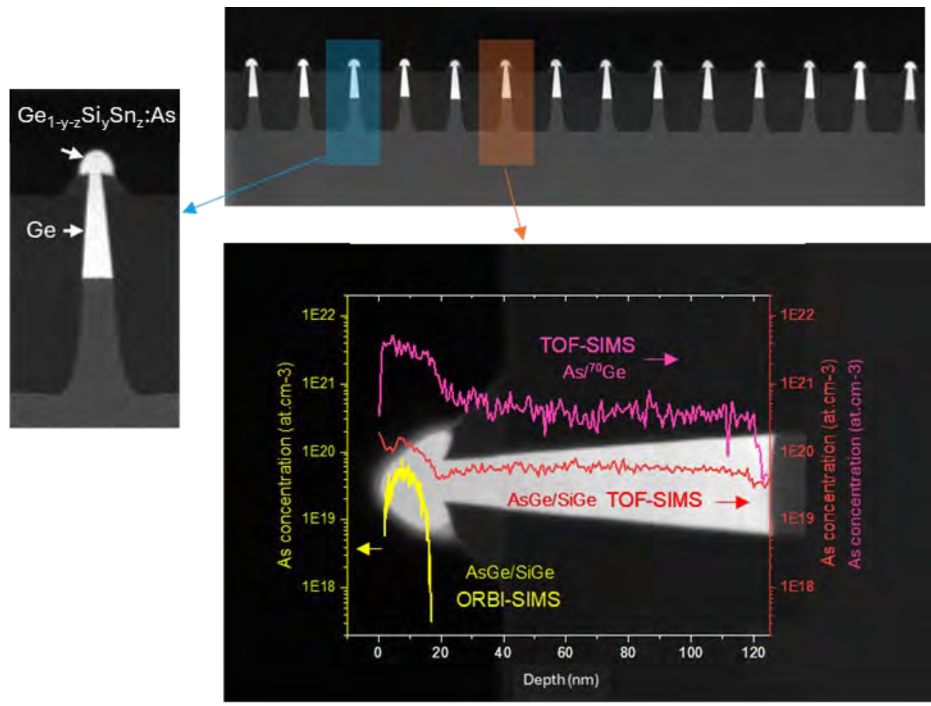

FIGURE 2. Depth profiles of As concentration in $Ge_{1-y-z}Si_ySn_z$:As / Ge fins comparing Orbitrap™-SIMS (yellow) and ToF-SIMS (pink and red). Orbitrap™ resolves the top-only As doping accurately, while ToF-SIMS shows artificial tails due to unresolved interferences.

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KEYWORDS

Arsenic (As) quantification, Silicon–germanium (SiGe), Orbitrap™-SIMS, Self-Focusing SIMS, Dopant depth profiling, High mass resolving power, FinFET fins

Infrared Photo-induced Force Microscopy (PiFM-IR) As A Substitute For EDS In Defect Review

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INTRODUCTION

Current industry standard protocols for wafer defect review and failure analysis is SEM-EDS spectroscopy, while TEM is also used. SEM-EDS best characterizes surface morphology and bulk sample composition,[1] and TEM best characterizes the internal structure of defects with resolution down to 50 pm.[2] EDS imaging provides elemental analysis and elemental mapping in a chosen area.[3]

While they are useful and highly efficient methods of locating and characterizing defects, SEM-EDS and TEM have limitations. Most notably, there is a high risk of wafer damage, damage to the defect, or obliteration of the defect with SEM-EDS due to the accumulation of thermal energy within the sample, causing melting and chemical decomposition. Additionally, the defects' chemical signature can be compromised due to the interaction of ambient organic contaminants (from ambient exposure and potentially from the SEM chamber surfaces) on the sample surface with the defect with the aid of the e-beam energy. SEM- and EDS-specific damage is visible by subsequent AFM topography imaging, routinely visible as a darker square over the site of SEM imaging, while EDS analysis often causes sharp point burns.[4] A second important limitation is that EDS can only capture elemental composition without any bonding or molecular information, thus greatly restricting chemical characterization of defects.[1]

We present the application of our patented technique, photo-induced force microscopy (PiFM), to defect review as a safer novel method of defect review, with particular applications as both a standalone technique and as a complementary technique to TEM.

PiFM IN DEFECT REVIEW

Photo-induced force microscopy (PiFM) couples IR spectroscopy to atomic force microscopy. This is accomplished through frequency mixing between the second eigenmode of the cantilever (f_2), at which the cantilever is dithered, and the difference between the first and second eigenmodes of the cantilever ($f_2 - f_1$), at which the IR laser is modulated. This produces a sideband frequency in the sample at the cantilever's f_1, which the cantilever resonates with. The two signals from the cantilever can then be separated, allowing for simultaneous recording of both AFM topographical and PiFM spectroscopic information.[5–8]

The most significant advantages to using PiFM are twofold: (1) PiFM interprets molecular information instead of merely elemental data via PiF-IR spectra, which are essentially identical to FTIR spectra; and (2) AFM topography provides quantitative height information in addition to the lateral shape information of the defects. PiF-IR spectra enable the use of spectral libraries for primary and multi-component analysis to discover potential compound matches for particles and defects that are far too small to be analyzed using an FTIR, and even EDS. Additionally, because our cantilever is operated in non-contact mode, there is a much lower risk for sample damage than with using EDS-based techniques. Other advantages of using PiFM for defect review is our instrument's ability to read KLARF files from wafer inspection tools, navigate to KLARF coordinates at sub-micron stage accuracy, and automatically acquire images and spectra. PiFM results notably show 3D topography and IR spectrum of defects as small as 5 nm (Figure 1). The figure also highlights an EDS-associated crater discovered with PiFM, which essentially destroyed the defect in the process.

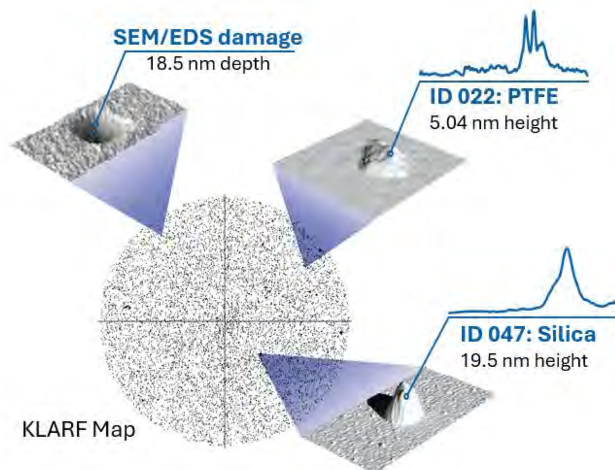

FIGURE 1. Summary of the capabilities of PiFM for defect review in comparison to SEM/EDS damage, denoting an example of EDS damage (top left) and two separate examples of defects located, topographically characterized, and chemically identified with PiFM.

In addition to particulate defects, PiFM-based defect review can effectively deal with residue-like and widespread defects, as demonstrated in an advanced packaging process where the chip was evaluated after a glue cleaning process (Figure 2). While topography showed relatively uniform raised speckling on the sample, PiFM was able to reveal relatively uniform spherical defects that the topography image alone could not identify. This was accomplished by imaging at an IR wavenumber associated with the glue used, which was able to be differentiated both from copper (I) oxide (Figure 2a) and silicon dioxide (Figure 2b).

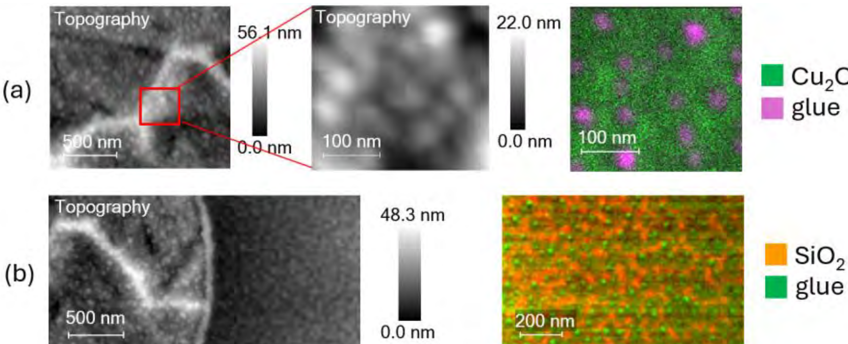

FIGURE 2. PiFM analysis of an advanced packaging process. (a) Topography and combined PiFM image of glue residue on copper (I) oxide. (b) Topography and combined PiFM image of glue residue on the dielectric surface (silicon dioxide).

Supplementing TEM Results With PiFM Analysis

By combining TEM with PiFM analysis, both internal structures from TEM and nanoscale chemical mapping from PiFM can be used to characterize not only defects but also various semiconductor processes. One of the limitations of scanning probe microscopy (SPM) based techniques is their inability to effectively deal with trenches or holes with a large aspect ratio (large depth : narrow width). Given the excellent PiFM spatial resolution (routinely sub-5 nm), PiFM can provide useful complementary information that EM-based techniques cannot if cross-section samples are characterized. Newer techniques for the preparation of TEM lamella, such as plasma FIB, which removes the risk of Ga contamination (which can effectively shield IR excitation), indicates tantalizing potential for PiFM. A method we propose for simultaneous TEM/PiFM analysis would be to analyze two similar lamellae mounted on the same TEM grid. The x-section lamellae would first be cut closely to each other (Figure 3a) and a pocket could be cut on the TEM grid for PiFM analysis: one lamella would be mounted by the standard method for TEM analysis, and the other would be placed into the PiFM pocket (Figure 3b). Finally, TEM could be performed on one lamella, while PiFM could be performed on the other (Figure 3c). Ideally, a TEM grid manufacturer could customize TEM grids with lamella pockets as well to eliminate that step on the user end.

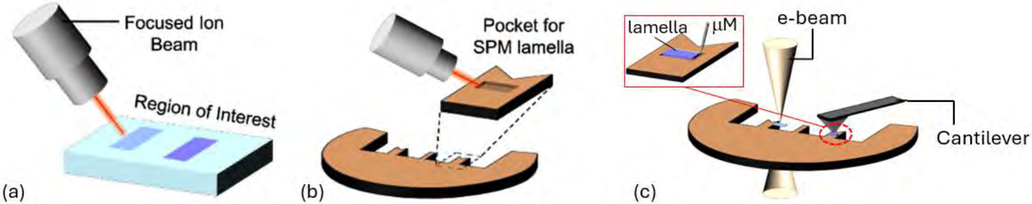

FIGURE 3. Proposed process for TEM/PiFM analysis. (a) Adjacent lamellae are cut from a sample via FIB. (b) A pocket is etched into an FIB TEM grid for the PiFM-analyzed lamella. (c) Both TEM and PiFM can be performed on the same TEM grid.

To showcase a TEM/PiFM correlation, we share an earlier work on a wood cell (Norway spruce), where we were able to observe the individual elementary cellulose fibers identified as cellulose from its IR peak at 1051 cm^{-1} (Figure 4).[9] While this data is not on a silicon wafer, we expect to be able to produce similarly compelling results on semiconductor samples by the time of the conference.

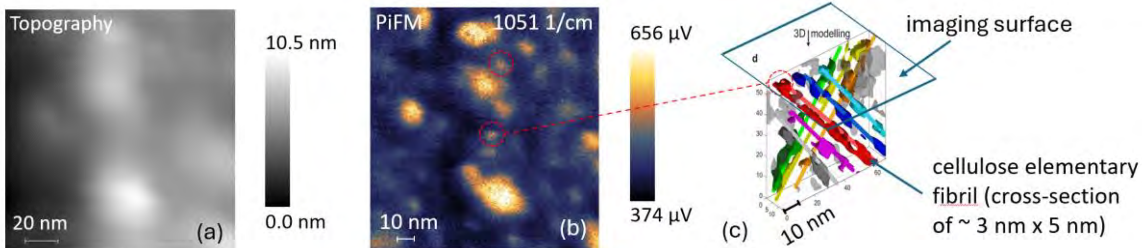

FIGURE 4. Topography (a), PiFM (b), and TEM (c) images of a lamella of a wood cell. Single fibers are individually colored in (c).

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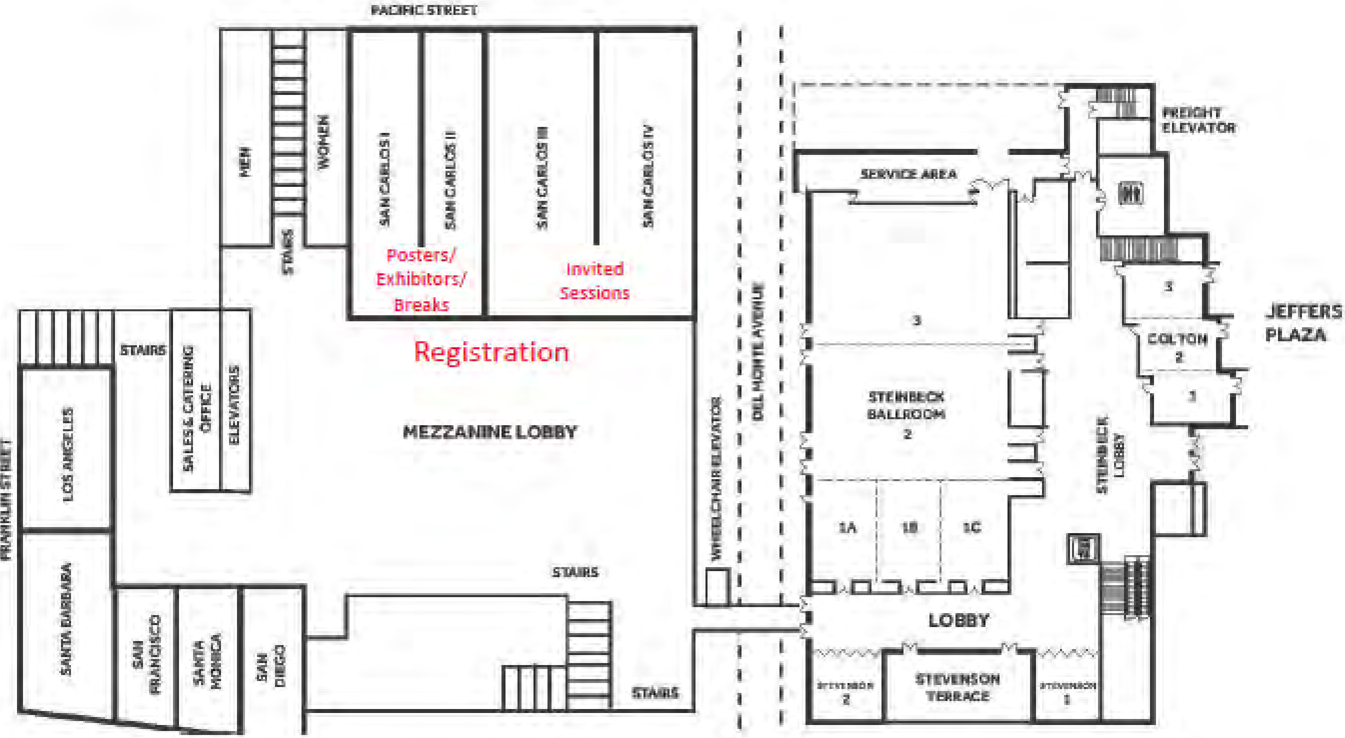
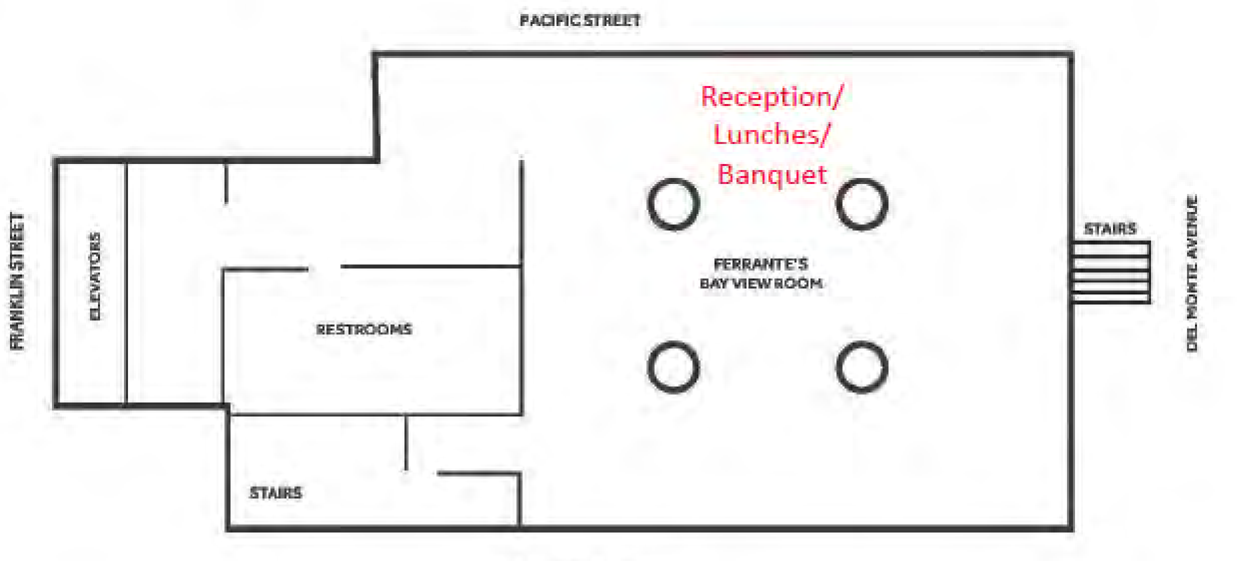
KEYWORDS

Defect review, failure analysis, photo-induced force microscopy, AFM, IR, SEM

MEZZANINE FLOOR



TENTH FLOOR



Program at a Glance

	Morning	AM Sessions	PM Sessions	Evening
Tuesday March 17th	**7:00** Registration / Attendee Check-in	**9:00** Conference Opening **9:15** Plenary I **10:00** Industry Trends	**1:30** Materials Characterization I **3:00** Materials Characterization II **5:00** Inline Metrologies I	**5:30** Poster Session **7:00** Banquet
Wednesday March 18th	**7:45** Registration / Attendee Check-in	**8:30** Inline Metrologies I **9:30** Inline Metrologies II	**1:00** Automation **3:00** Virtual Metrology & Correlative Approaches	**4:30** Poster Session
Thursday March 19th	**8:00** Registration / Attendee Check-in	**8:30** Plenary II **9:15 AM** Advanced Packaging **11:15** EUV and Beyond EUV	**1:30** Novel methods to support novel CMOS memory and logic R&D **1:30** Novel methods to support beyond CMOS device R&D **4:30** Plenary III	