

Metrology Requirements for Nanoimprint Lithography

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What am I doing here?

- Canon has developed a novel Nanoimprint Lithography capability which has unique challenges relative to more standard 4x reduction methods
- The purpose of this presentation is to introduce our technology, highlight some of the challenges and get folks thinking about metrology methods suitable for this technology*
- In this presentation, we will discuss two inkjet-based applications that require advanced measurement methods

**But promise not to derive anything from Maxwell's equations during the talk*

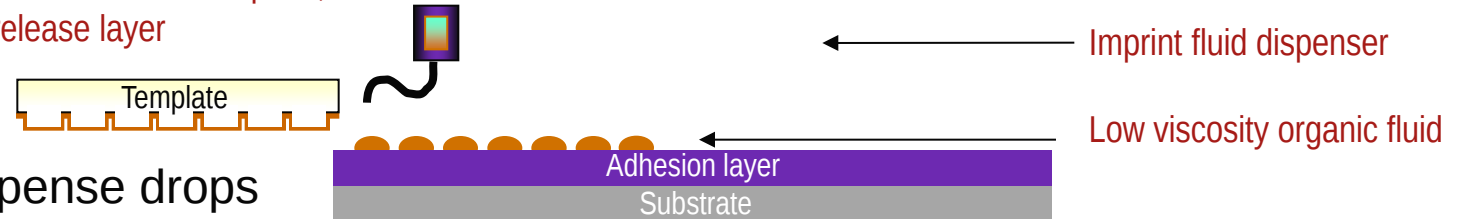
Nanoimprint Basics

Canon's Approach to Nanoimprint (NIL)

- The Canon NIL process uses a transparent mask and jetted resist to create pattern
- This method enables an easier approach to overlay and optimizes the residual layer thickness uniformity beneath the imprinted features
 - First introduced by Grant Willson in 1999

High resolution fused silica template, coated with release layer

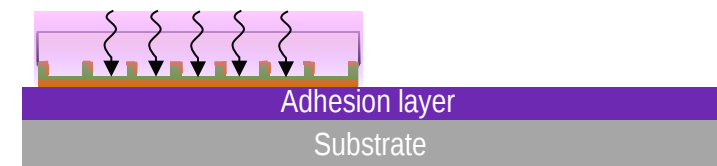
Step 1: Dispense drops



Step 2: Lower template and fill pattern

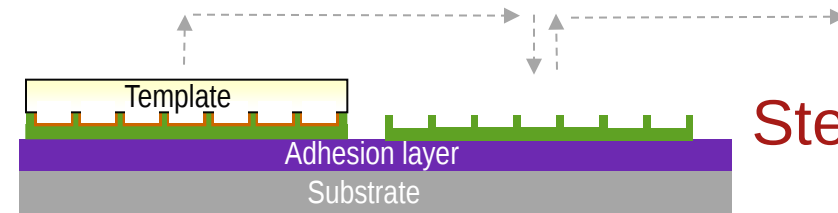


Step 3: Polymerize imprint fluid with UV exposure



Same Process Used for Step & Repeat and Whole Substrate Patterning

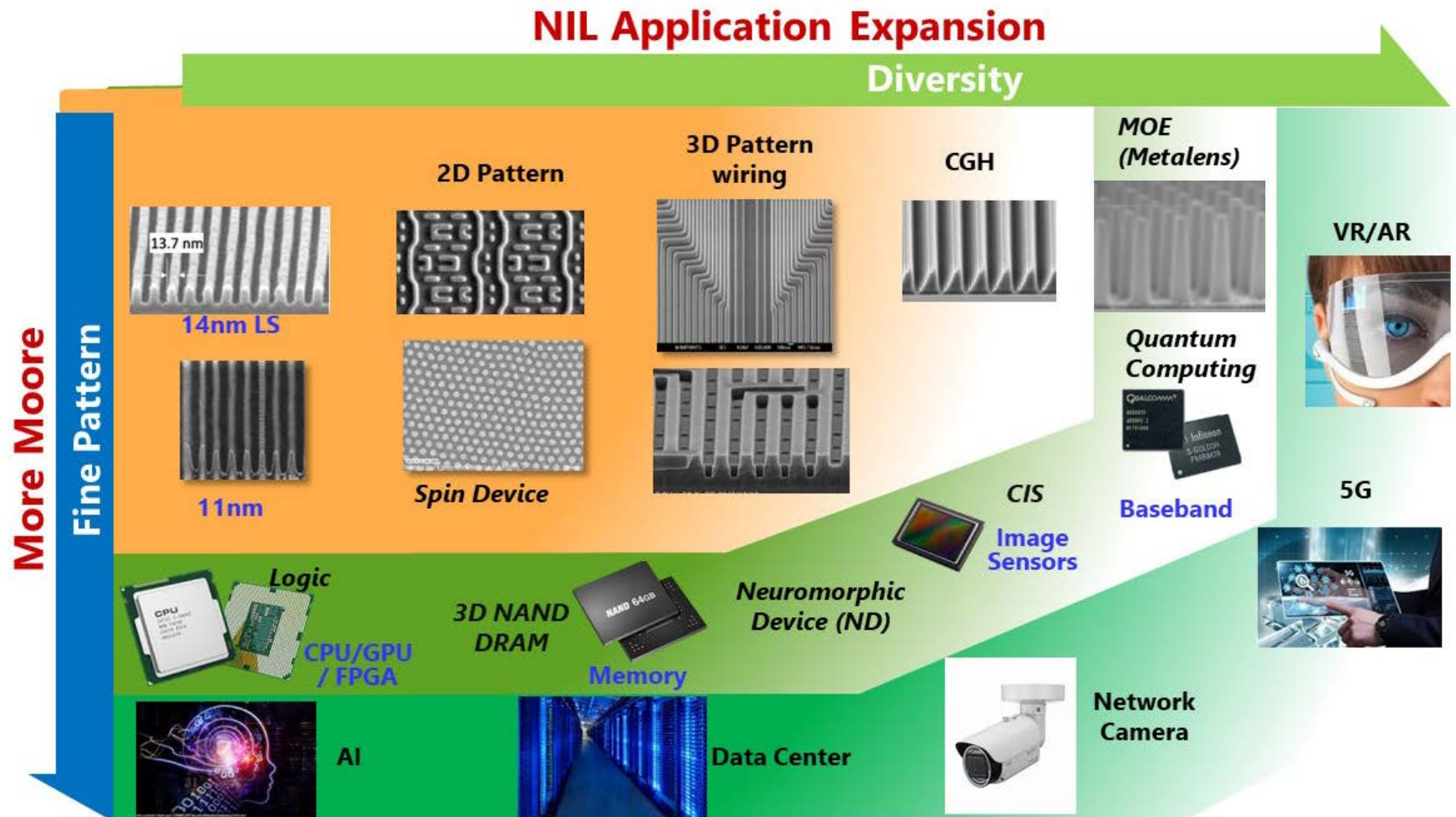
Step 4: Separate template from substrate



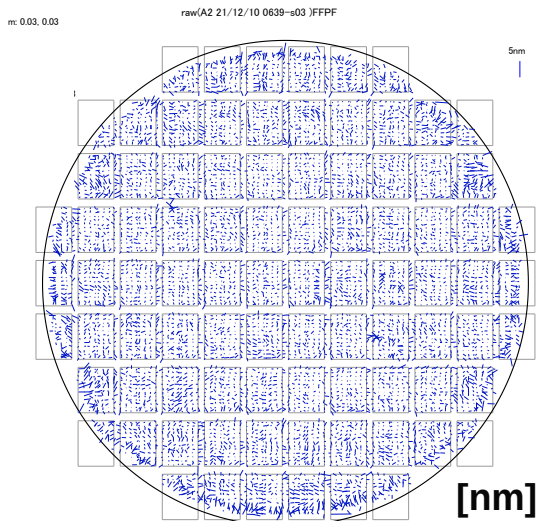
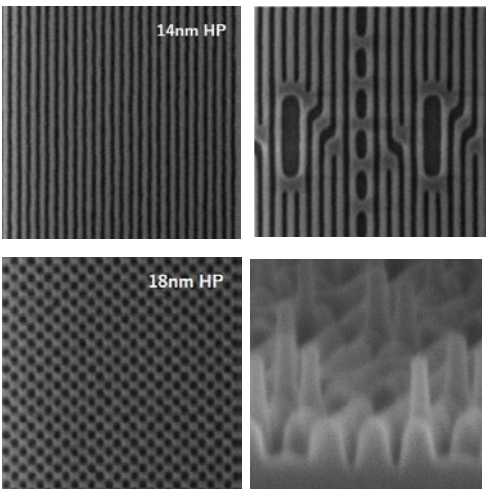
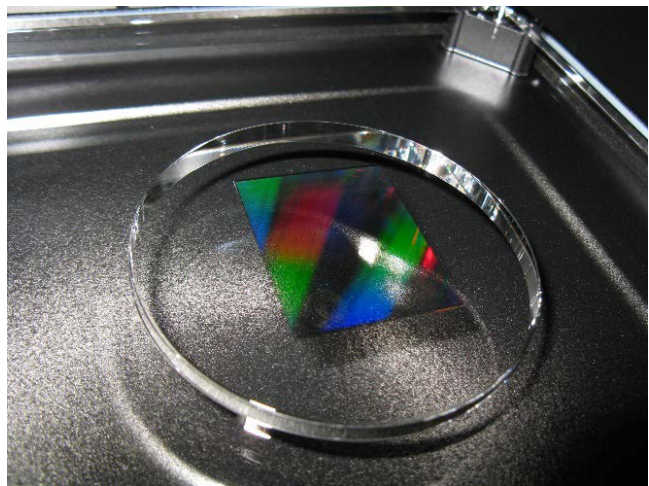
Step & Repeat

NIL Application Space

- Unlike other lithographic methods, NIL provides the pattern flexibility and a cost structure at address a much larger application space
- But any application requires a supporting ecosystem to enable a suitable production solution



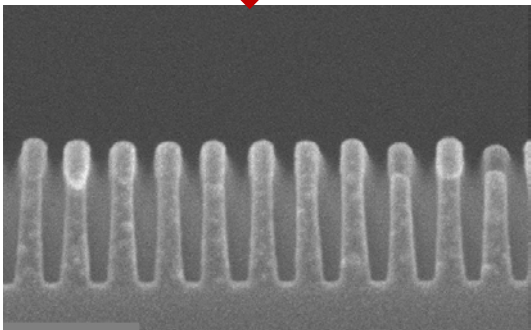
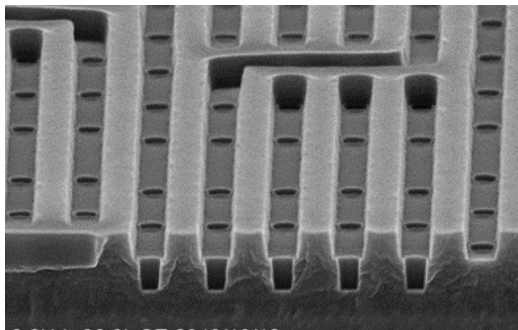
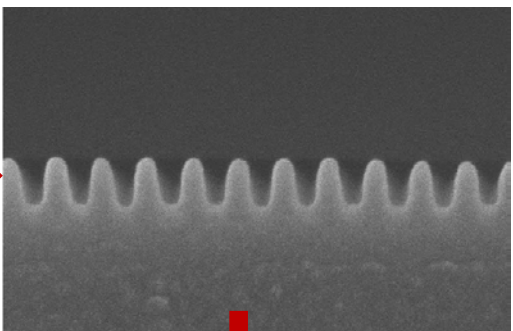
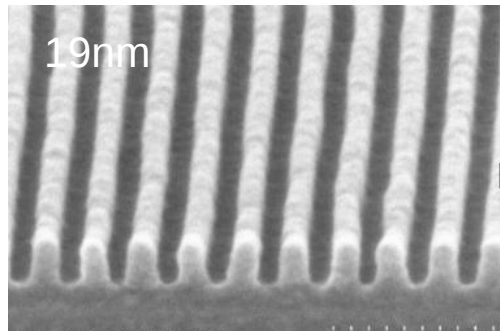
NZ2C performance



5nm

FPA-1200 NZ2C
NIL to ArF-IML
Evaluated with 96
locations per field
Full field + partial field

m+3σ	X	Y
Best Wafer	2.20	2.10
Average	2.42	2.24



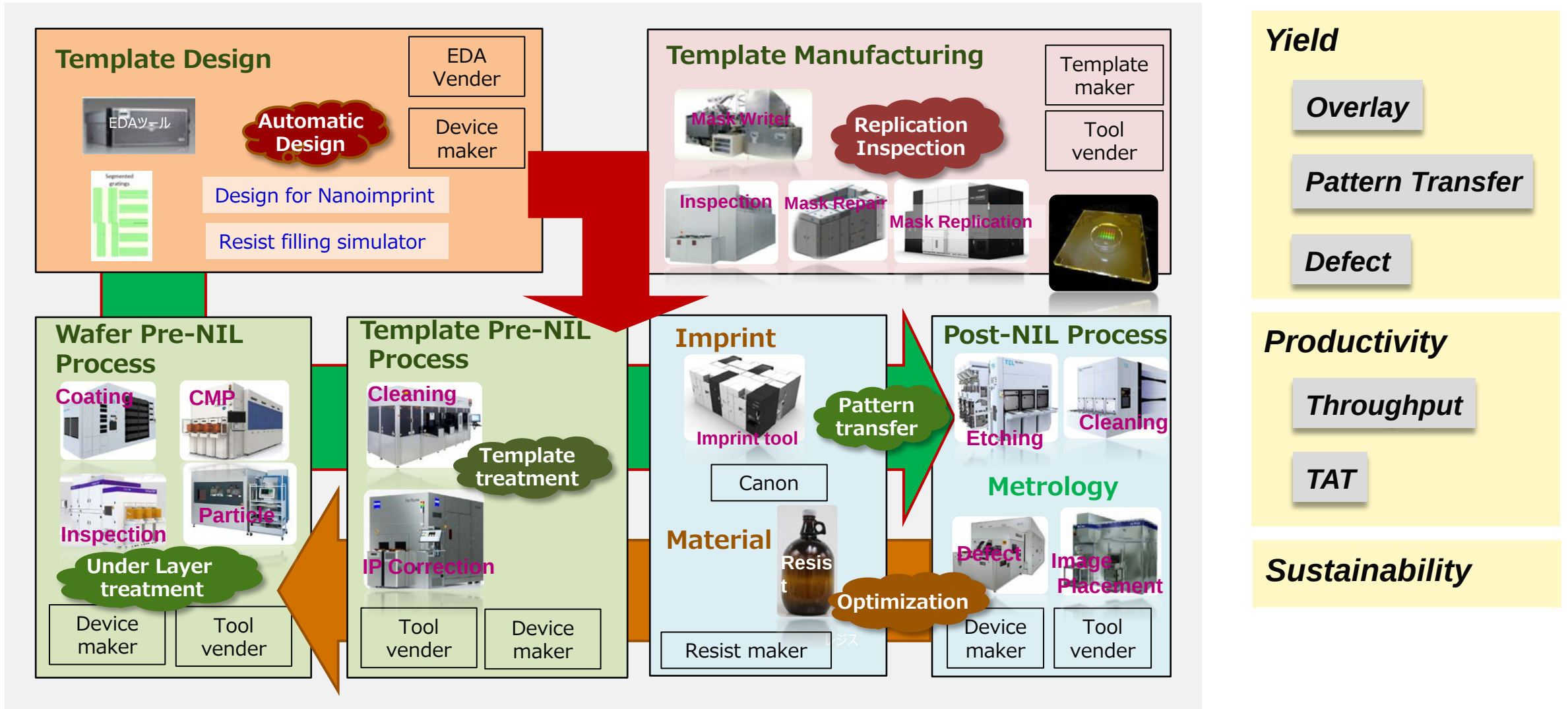
Cut layer demonstration

Metalens



NIL Metrology Requirements

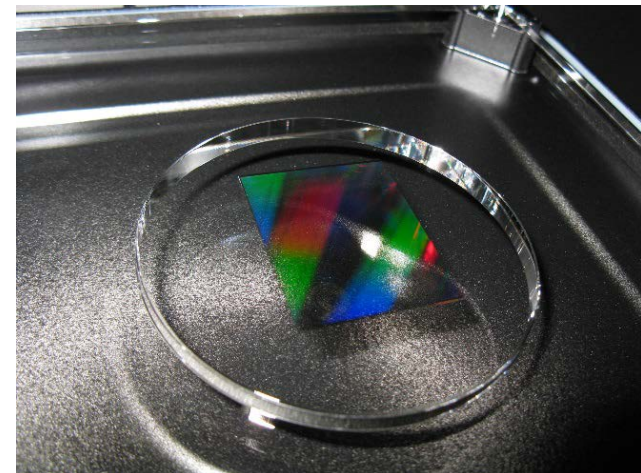
Nanoimprint Ecosystem



Many ecosystem requirements are connected with the imprint mask (template)

The NIL Mask

- ❑ One clear advantage of NIL is that the pattern formed on the mask is what is printed on the wafer – no complex computational lithography
- ❑ But everything we need to measure must be done on a 1x pattern
 - There is no 4x reduction
- ❑ In addition, replica masks are required since the lifetime of the mask is limited by defects induced during the imprint process
- ❑ Key metrics to be measured include
 - Critical dimension (CD), CDU and linewidth roughness (LWR)
 - Image placement
 - Defect inspection
 - Defect repair



Master Mask Fabrication

- The basic mask pattern is defined using a very typical process sequence

Master



- For best resolution and lowest linewidth roughness, non-chemically amplified resists are used
 - These resists require higher doses, but the higher dose creates more secondary electrons, which reduce LWR
 - Non-chemically amplified resists also minimize the stochastics introduced from acid diffusion that occurs during the post exposure bake process
 - Years ago, the e-beam resist of choice was ZEP520A
 - Best performance was achieved by biasing the features in the GDS (smaller), increasing exposure dose and using diluted developers to enhance resist contrast
 - Newer materials, including chemically amplified resists and metal oxide resists with even better performance may be available

Master Mask CDU and Image Placement

- 1nm image placement has been demonstrated using an MBMW-101*

2x nm LS

		Master
Defects	pcs/cm ²	-
CDU (3 σ)	nm	0.44
IP (3 σ)	nm	1.52/0.91

2x nm pillar

		Master
Defects	pcs/cm ²	-
CDU (3 σ)	nm	0.65
IP (3 σ)	nm	0.97/1.02

*MBMW-101 is an 8-year-old tool with a global registration spec of 2nm

Source: SPIE 2023

Mask Replication Tool

- Canon makes an FPA-1100NR2 for the purpose of fabricating replica masks
- NR2 is located at a DNP manufacturing site and at Utsunomiya
 - An older legacy tool is also located at DNP
- Tool specifications are shown in the table to the right
 - Replica mask costs are low (compared to a master mask), and driven by the throughput of the mask replication tool

**FPA-1100 NR2
Mask Replication Tool**



Target Specifications		
Throughput	4	Mask/hour
CD Uniformity (3 σ)	0.8	nm
Image Placement Accuracy (3 σ)	1.0	nm
Particle	0.002	pcs/Mask

Mask CDU and Etch Depth

CDU

- Mask CDU for lines typically < 1nm*

Mask Type	Typical pattern	Feature size	CD* [nm]	
			Ave.	3σ
Master	L/S	19nm	20.12	0.34
		32nm	38.86	0.49
		54nm	65.59	0.66
Replica	L/S	26nm	33.61	1.07
Replica	Hole	17nm	18.04	1.70
		18nm	19.91	1.45
		20nm	22.68	1.27

* Imprinted measurements

Etch Depth

- Mask Feature Etch Depth is very well controlled.
- Shown is a run of six replica masks with a targeted etch depth of either 40nm or 50nm

Mask ID	1	2	3	4	5	6	7
Target (nm)	40.0	40.0	40.0	40.0	40.0	50.0	50.0
Mean	40.2	40.6	40.3	40.0	39.5	52.2	51.6
STDEV	0.17	0.25	0.22	0.21	0.20	0.20	0.25
Max	40.5	41.0	40.8	40.3	39.8	52.5	51.9
Min	40.0	40.3	40.1	39.5	39.3	51.8	51.3
Range	0.52	0.68	0.68	0.77	0.52	0.67	0.66

Replica Imprint Mask Results: Image Placement

- This slide demonstrates Image placement mapping across three replica masks.
- Image placement is ~ **1nm** and the results are repeatable, replica to replica

Template Matching Example

- 3 replica masks were generated from a single master mask
- 322 measured locations per field

Replica 1

	X	Y	unit
3 σ	1.17	1.11	nm
max	1.12	1.29	nm
min	-1.17	-1.10	nm

Replica 2

	X	Y	unit
3 σ	1.16	0.91	nm
max	0.99	1.11	nm
min	-1.25	-0.78	nm

Replica 3

	X	Y	unit
3 σ	1.17	0.81	nm
max	1.09	0.86	nm
min	-1.22	-0.74	nm

IP difference = (2) - (1)

	X	Y	
3 σ	0.38	0.34	nm

IP difference = (3) - (1)

	X	Y	
3 σ	0.33	0.40	nm

IP difference = (3) - (2)

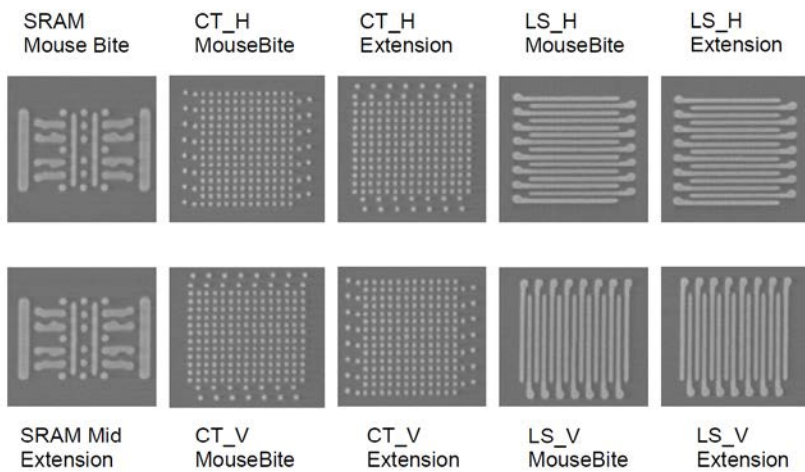
	X	Y	
3 σ	0.35	0.37	nm

Mask Inspection

- NIL direct mask inspection has been done with both e-beam and optical systems

- E-beam Inspection

- Hermes Microvision eScan 315xp



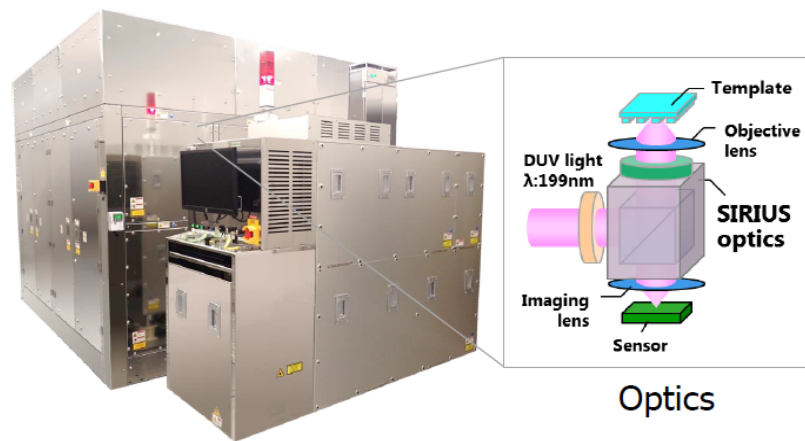
Bacus 2009

- Optical Inspection

- NuFlare

- ✓ **New inspection tool NX-8000 was developed by NFT which specialized for the nano-imprint pattern inspection featuring**

- **199nm inspection wavelength**
- **High inspection throughput : 60min@26x33mm**
- **3 inspection modes for NIL inspection**



Optics

NIL template inspection tool NX-8000

Inspection mode

Mode	Defect Sensitivity*	Through put
RIGEL	24-28nm	20min
VEGA	24nm	40min
SIRIUS	15nm	60min

*Detectable defect size on L/S pattern

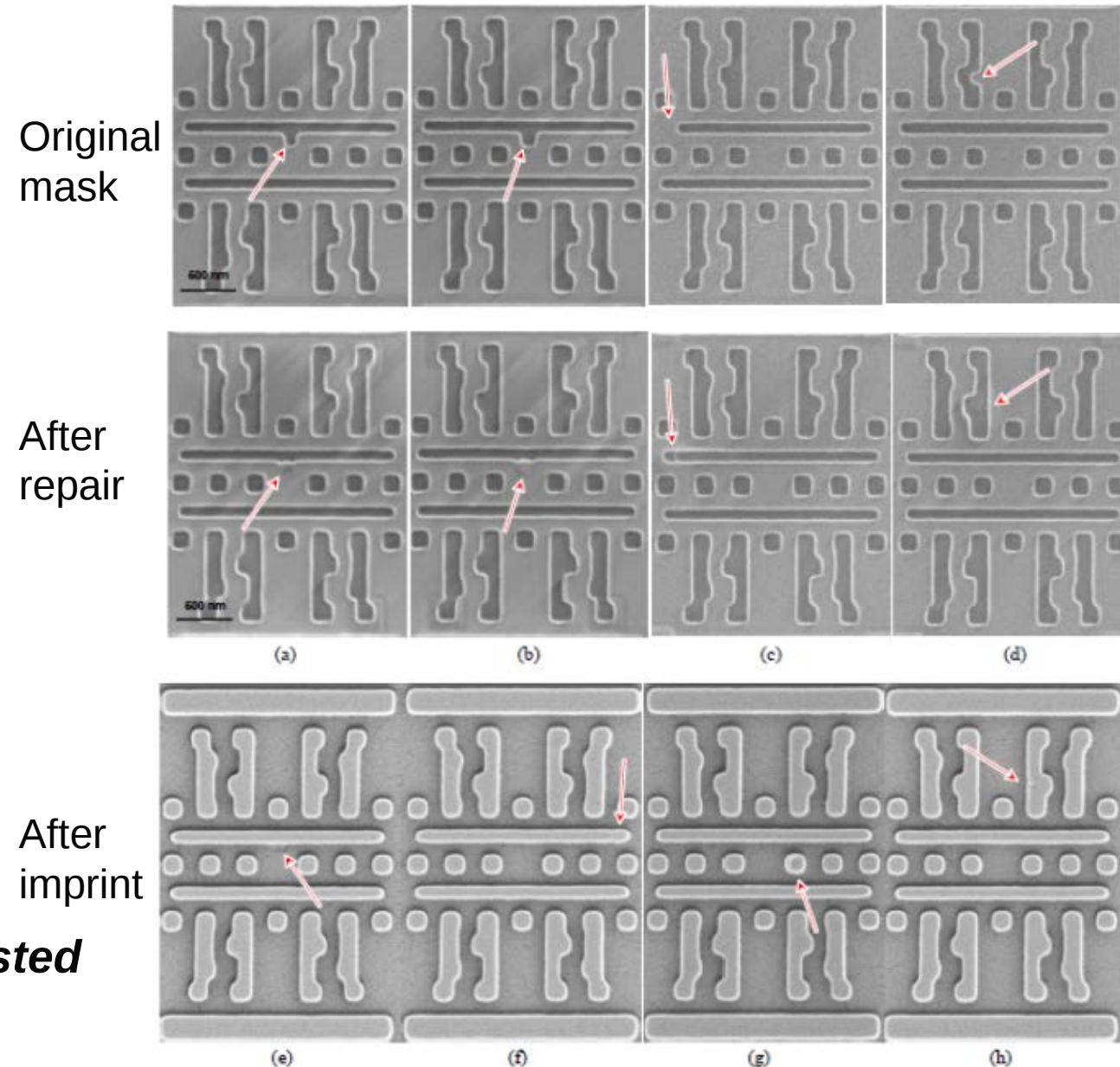
SPIE 2017

E-beam has acceptable resolution but is too slow. Optical inspection has reasonable throughput, but resolution is lacking

Mask Repair

- The most advanced repair work has been done using an e-beam repair system from Nawotec (now Zeiss)
 - 32nm pattern
 - SPIE 2008
 - Nawotec was later acquired by Zeiss (tool name is MeRiT)
 - Both subtractive (glass etching) and additive (deposition of an oxide) repairs are possible

Repair of smaller pitch features is largely untested



Want more mask metrology?

zoom

Support English ▾

https://spie-org.zoom.us/webinar/register/9617563205851/WN_cczRJVM1S6SFSOek9hWCKg#/registration



Mask Metrology for Advanced Nodes

Date & Time Mar 20, 2026 08:00 AM in [Arizona](#)

Description Photomasks are an essential component of the lithography process. With increasingly tighter requirements on edge placement error (EPE), controlling crucial mask parameters—such as pattern placement, critical dimension (CD), and induced phase changes by absorbers—is necessary to ensure optimal chip production yields.

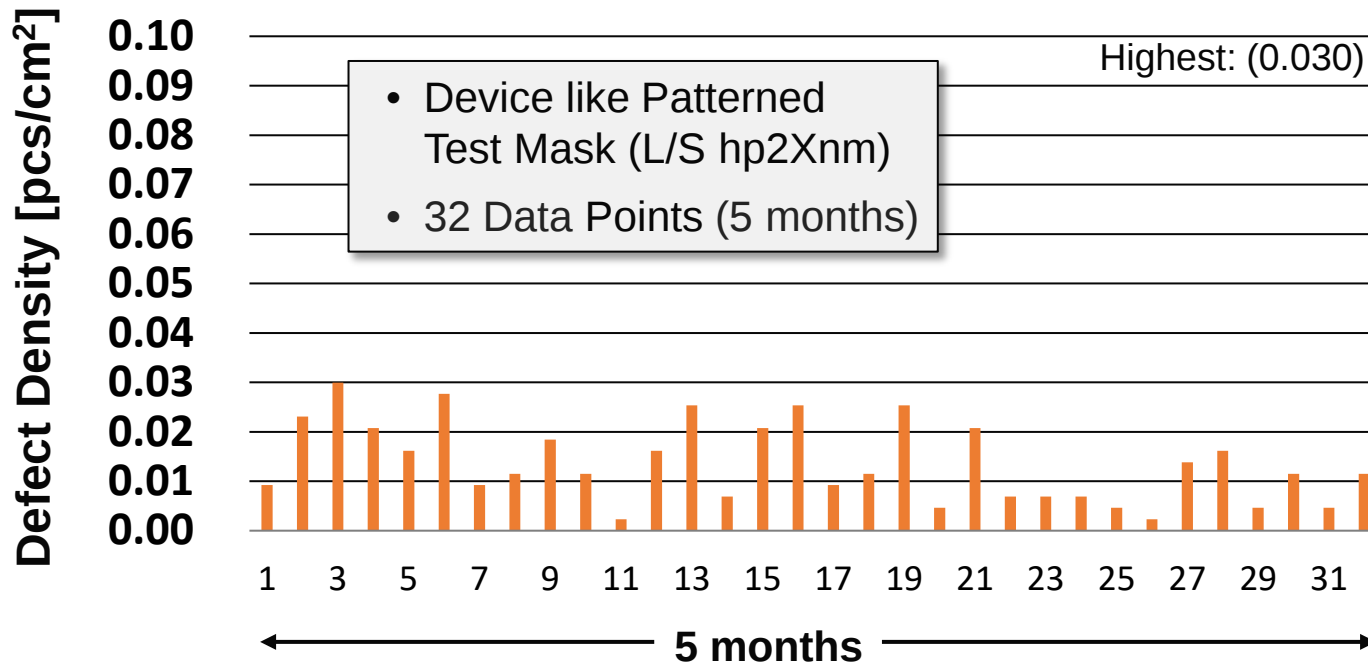


NIL Defectivity

There are two defect modes that need to be tracked: Random and Repeating

Random Defects

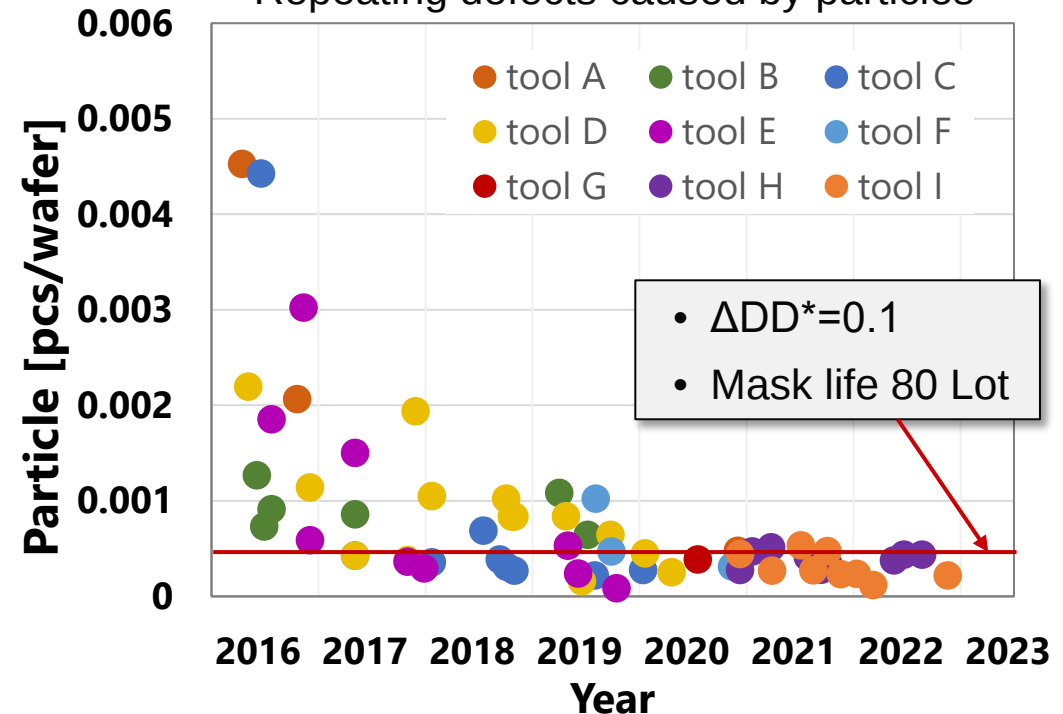
Main source of random defectivity: non-fill and feature collapse



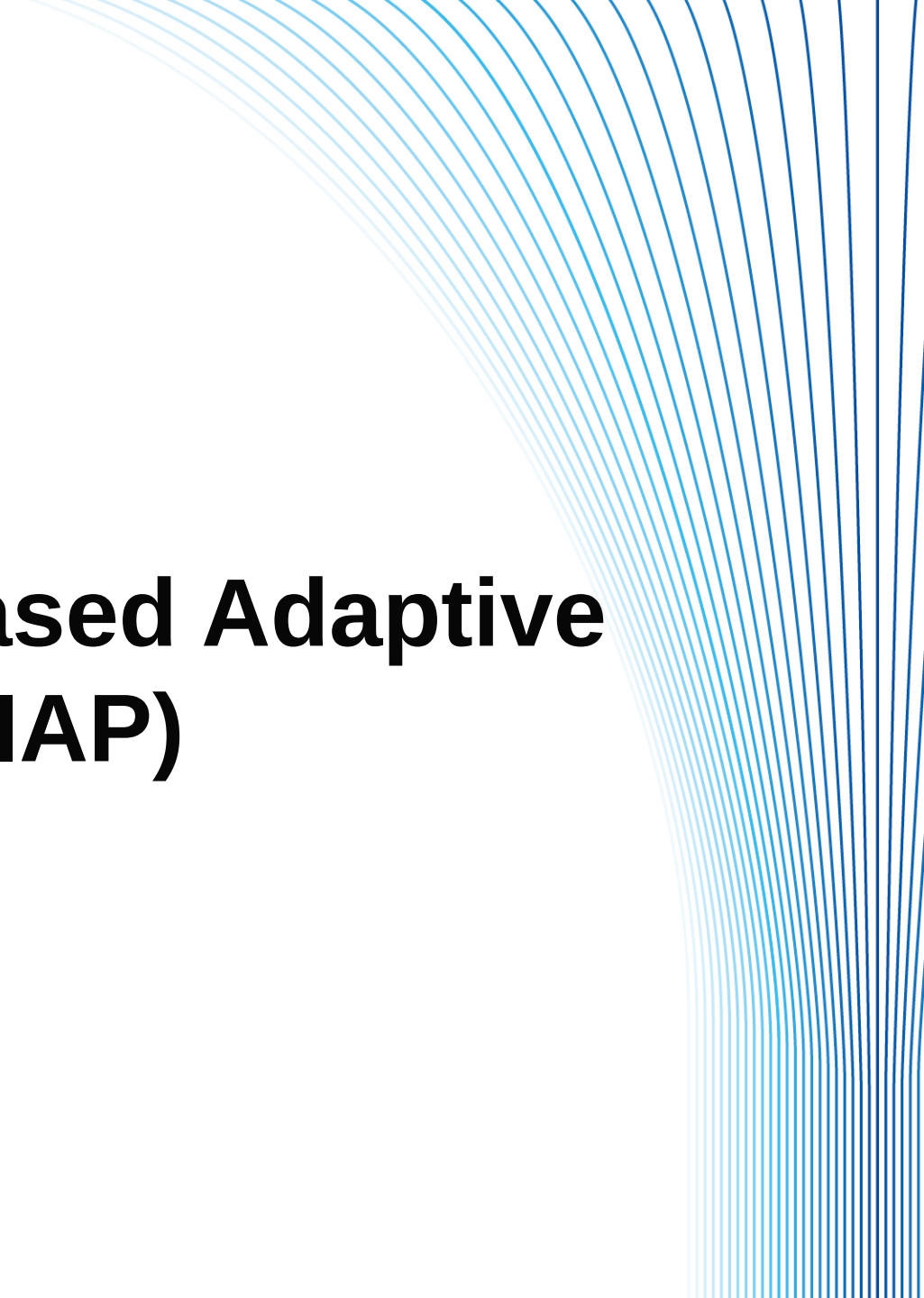
Day-to-day Defect stability meets 3D NAND mass production level.

Repeater Defects

Repeating defects caused by particles



Particle adder target is one defect every 2,500 wafers and is now being achieved in multiple stations



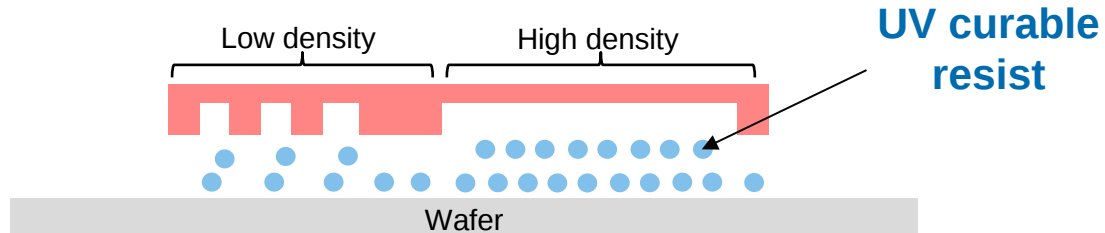
Introduction to Inkjet-based Adaptive Planarization (IAP)

NIL vs IAP

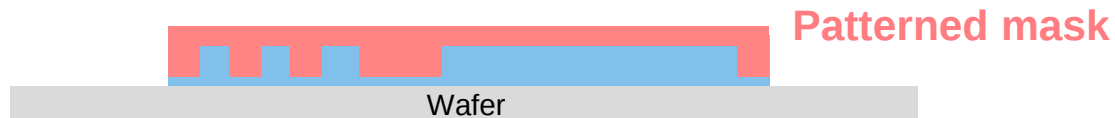
- Inkjet-based technology can be used both to create patterns and to remove topography from a wafer surface

Nanoimprint Lithography

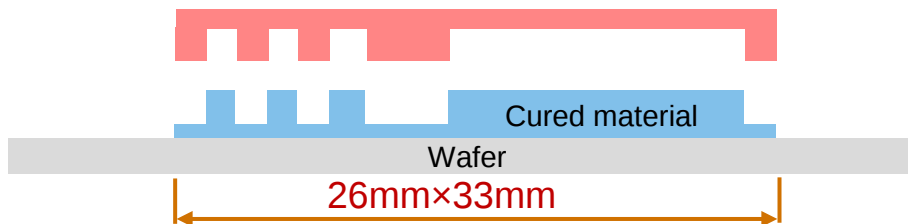
Step 1. Jetting of droplets onto a wafer



Step 2. Mask contacts a liquid resist

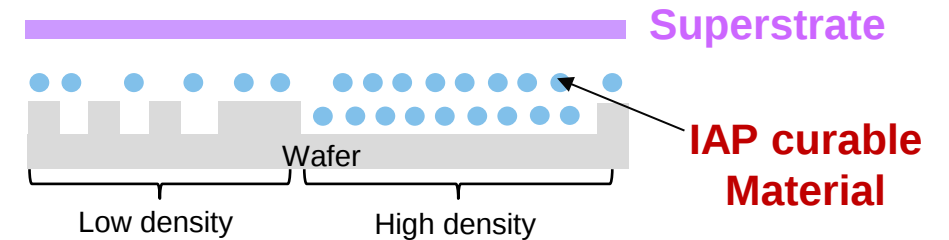


Step 3. UV Cure and Separation



Inkjet-based Adaptive Planarization

Step 1. Jetting of droplets onto a wafer



Step 2. Glass superstrate contact to an IAP Material



Step 3. UV Cure and Separation



Why take a full wafer approach?

There are three primary reasons:

- ❑ **Throughput**: We can process a wafer faster with a single print than we can having to do it in a step and repeat fashion ~ 100 times
- ❑ **Field stitching**: A whole wafer process avoids the field stitching problem and allows easy printing of a contiguous film across the entire wafer
- ❑ **Minimize Defectivity**: If I pick up a repeater defect in a 26mm x 33mm field, I now repeat that defect in every printed field. With a full wafer approach, that defect gets repeated only once on a wafer

Why does topography matter?

- ❑ Advanced lithographic technologies and all device types are all impacted by topography
 - For ArF immersion, topography affect depth of focus (DOF)
 - Reduced DOF impacts CDU and therefore device performance
 - For EUV, topography affects both DOF and overlay
 - EUV masks have a 3D component. Topography shifts pattern placement, which again impacts yield
 - For NIL, topography affects residual layer thickness uniformity, overlay and resist fill time
 - Impacting CDU, throughput and yield

- ❑ Topography generally takes on two forms:

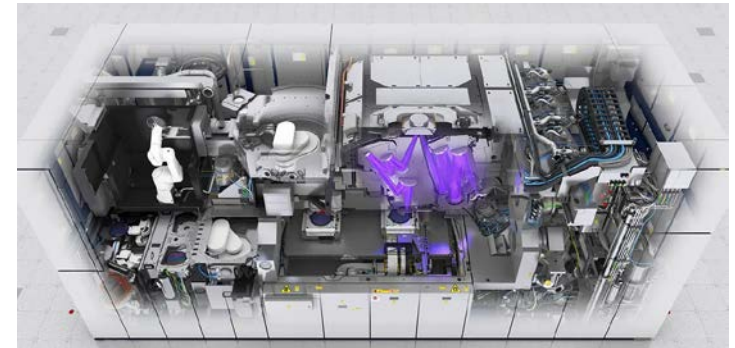
- Topography induced from the 300mm wafer
 - Pattern topography

- ❑ The industry routinely uses CMP to remove topography, but there are many device levels where this does not work

ArFi



EUV

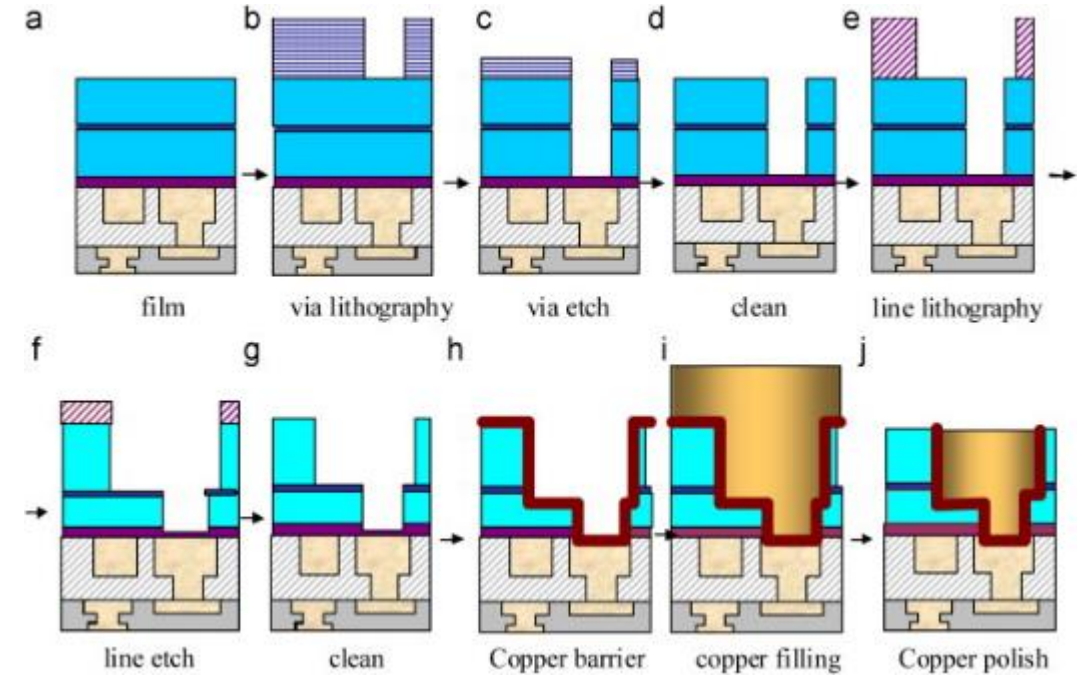
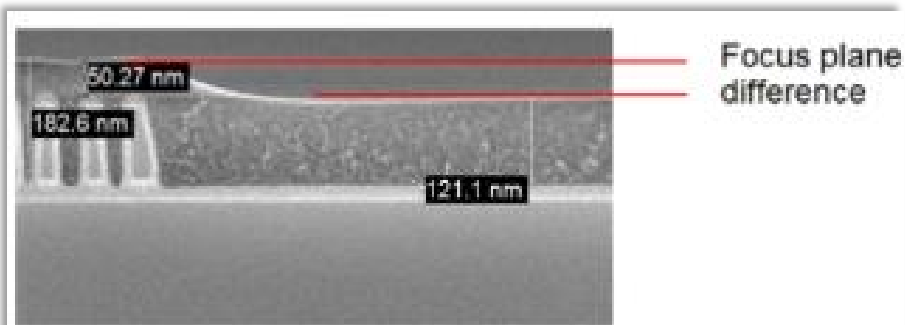
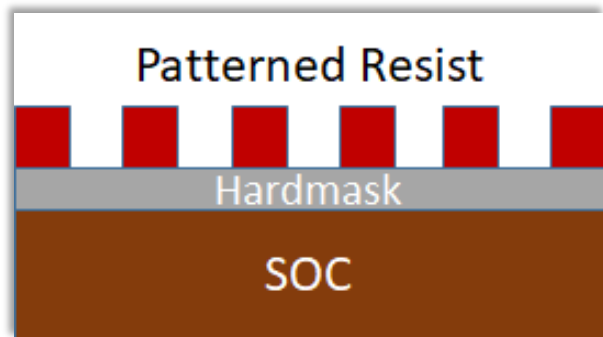


NIL



Dual-damascene illustrates challenges

- Back-end metal levels use a dual damascene process
- This introduces pattern topography



- So, what do device manufacturers do?
 - Apply multi-level resist stacks, e.g., SOC, to minimize the pattern topography
 - SOC does not correctly planarize larger features
 - Sometimes, multiple step processes are needed
 - Restrict design layouts
 - Smaller features, dummy patterns
 - Adversely affects device performance and adds cost

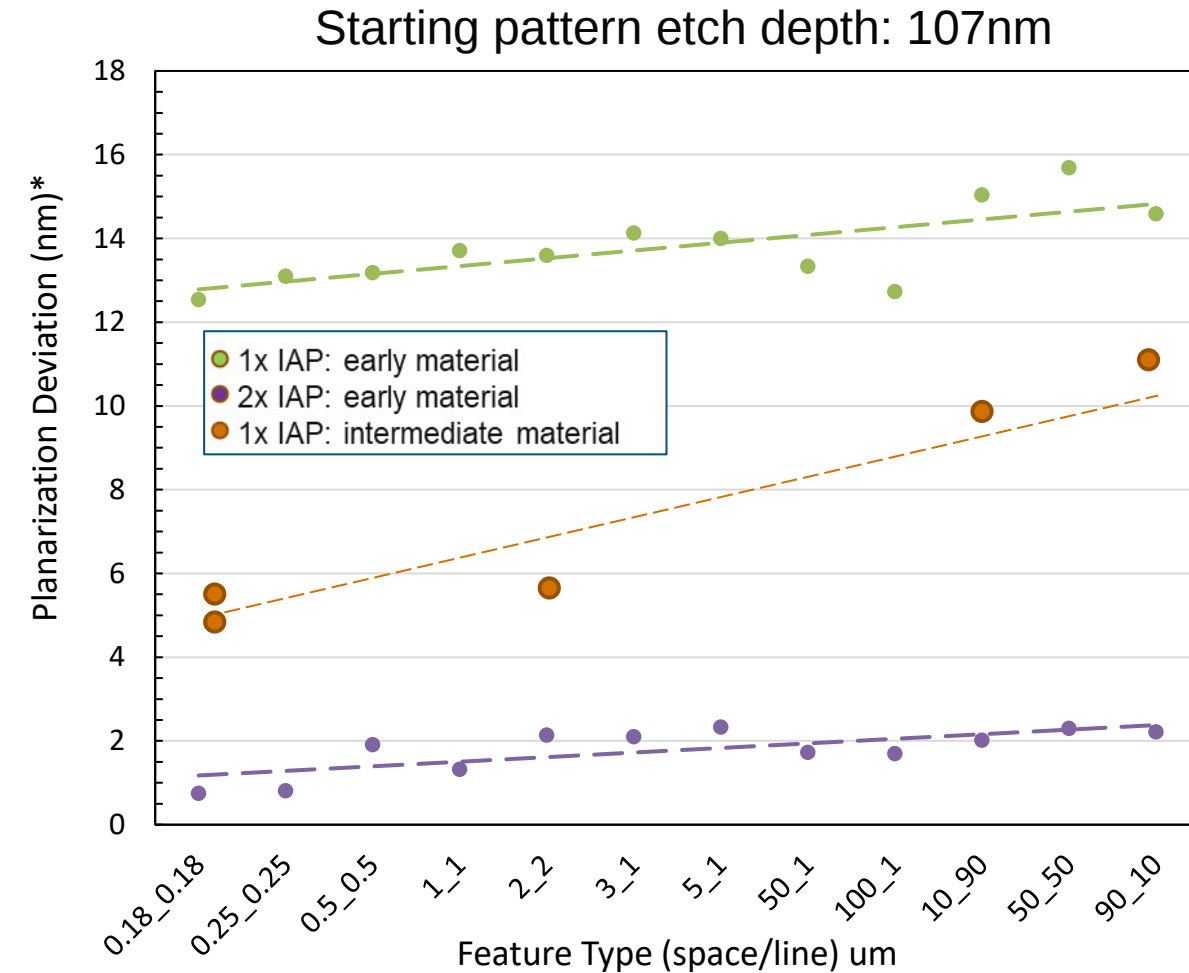
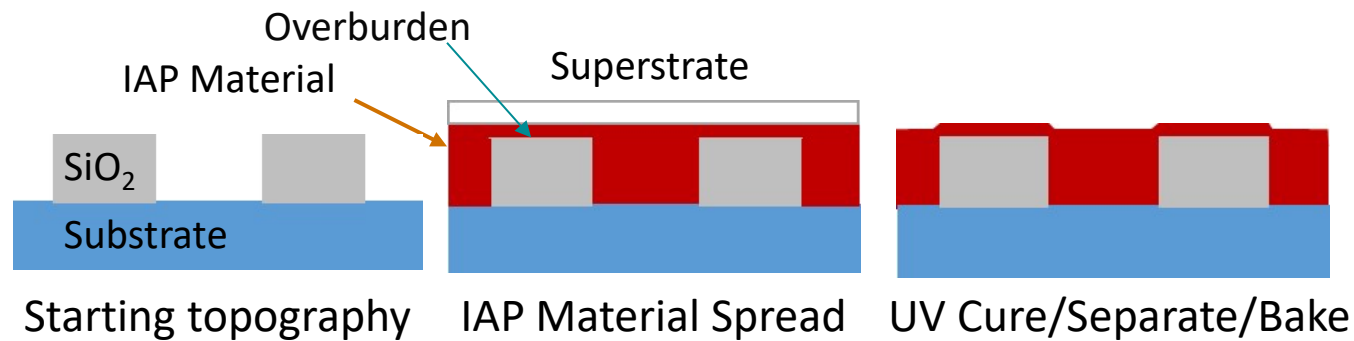
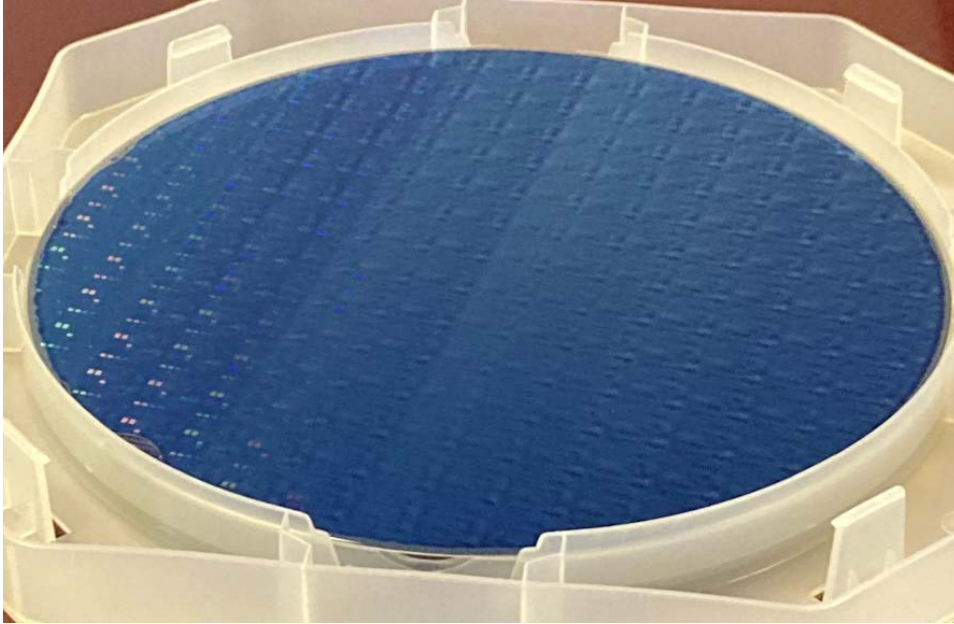
What does the industry require?

- Planarization technology that:
 - Reduces topography, allows more design freedom, improves performance
 - Is lithography agnostic
- Planarizes existing pattern topography ***and*** conforms to wafer topography
 - ***With excellent gap-fill***
 - ***Producing a uniform overburden needed for downstream processes***
 - ***With materials that allow robust post-processing***
- Cost-effective
 - One tool that puts down the required planarization layer and readies that layer for all the required downstream processes



IAP Results

Local Planarization: Initial Results*

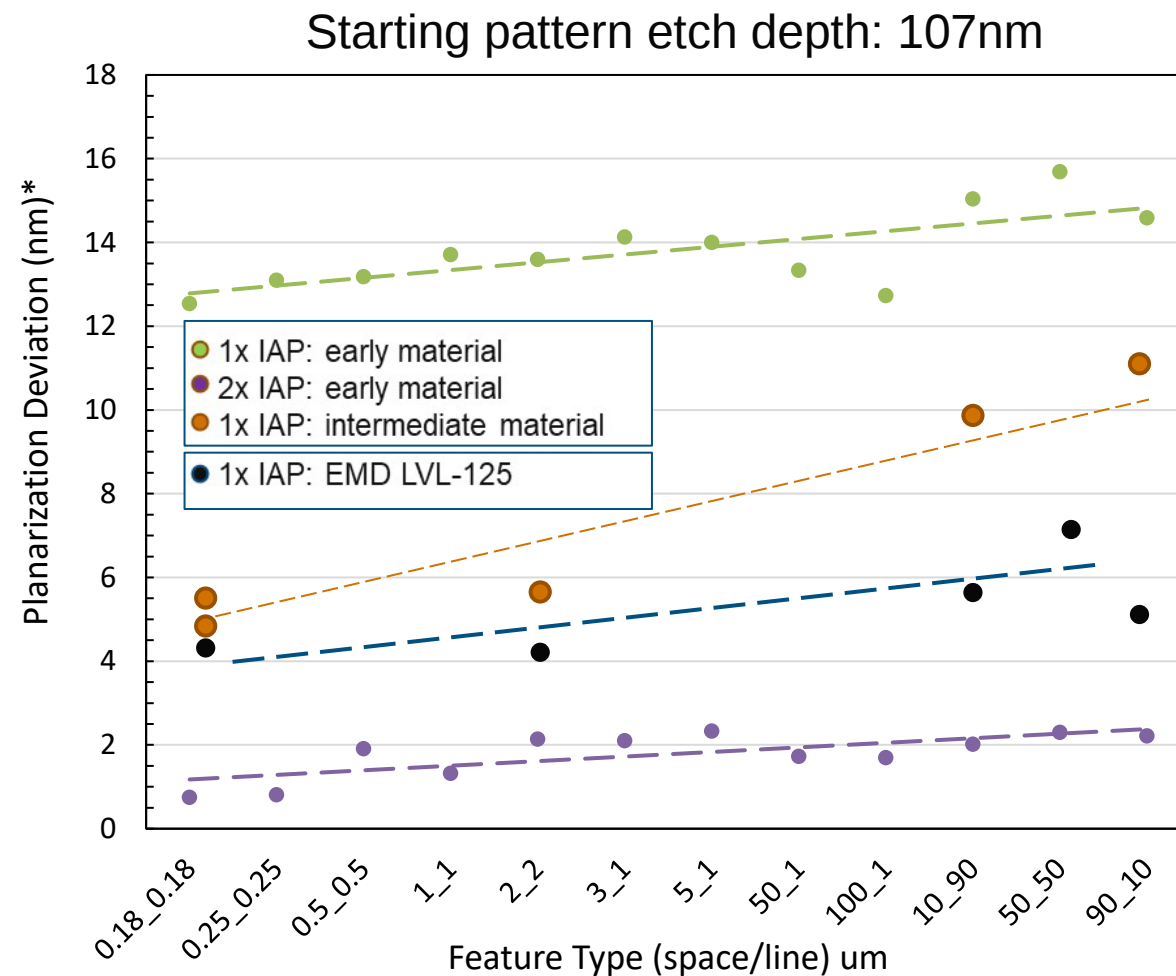
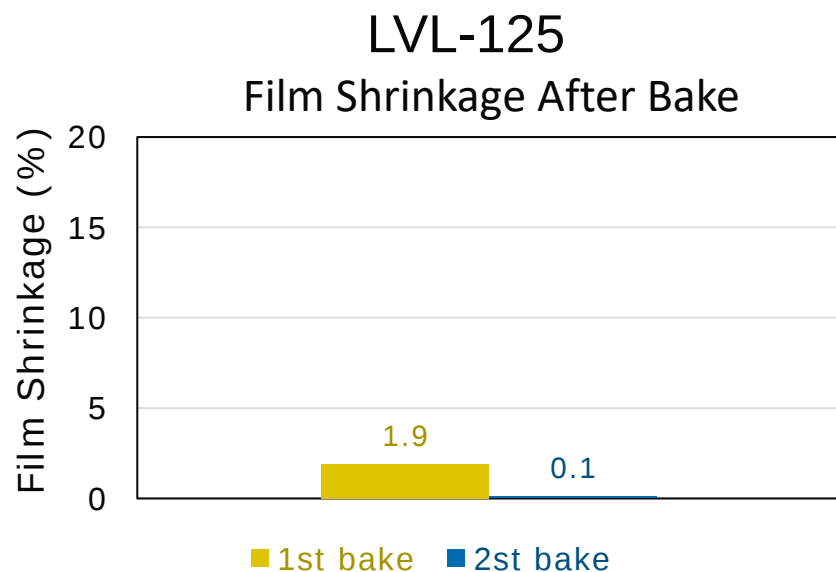


- NIL resists and early IAP formulations were subject to shrinkage during UV cure and bake

* Measured using a Bruker Insight tool in AFM mode

Local planarization: Recent Results

- By developing new IAP materials with reduced shrinkage after UV cure and bake, it is possible to significantly improve IAP performance after a 1X IAP process*

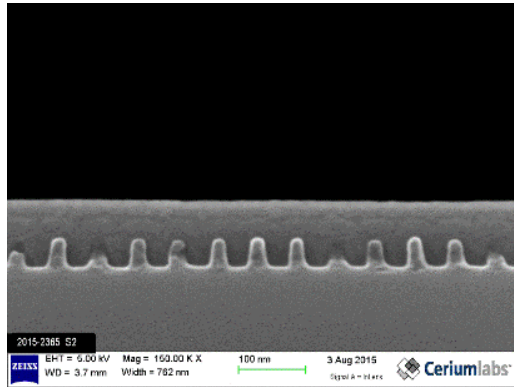


- 1x IAP results better than 7nm for all features
- 2x IAP results better than 3nm for all features

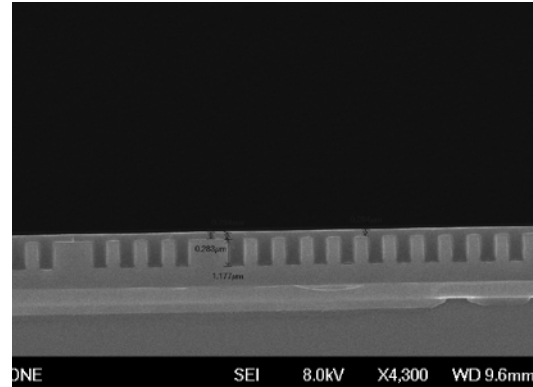
*See paper by Sekito-san for more details

Local Planarization Results

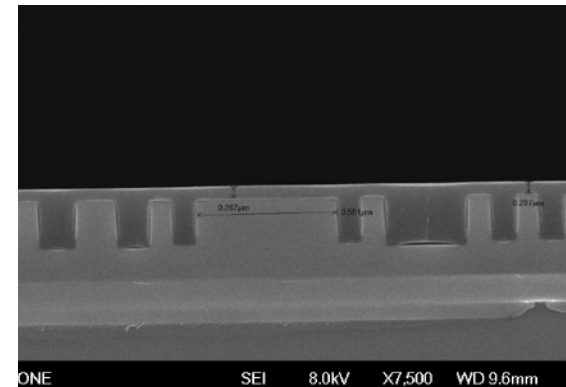
Excellent planarization across small and large pitch features



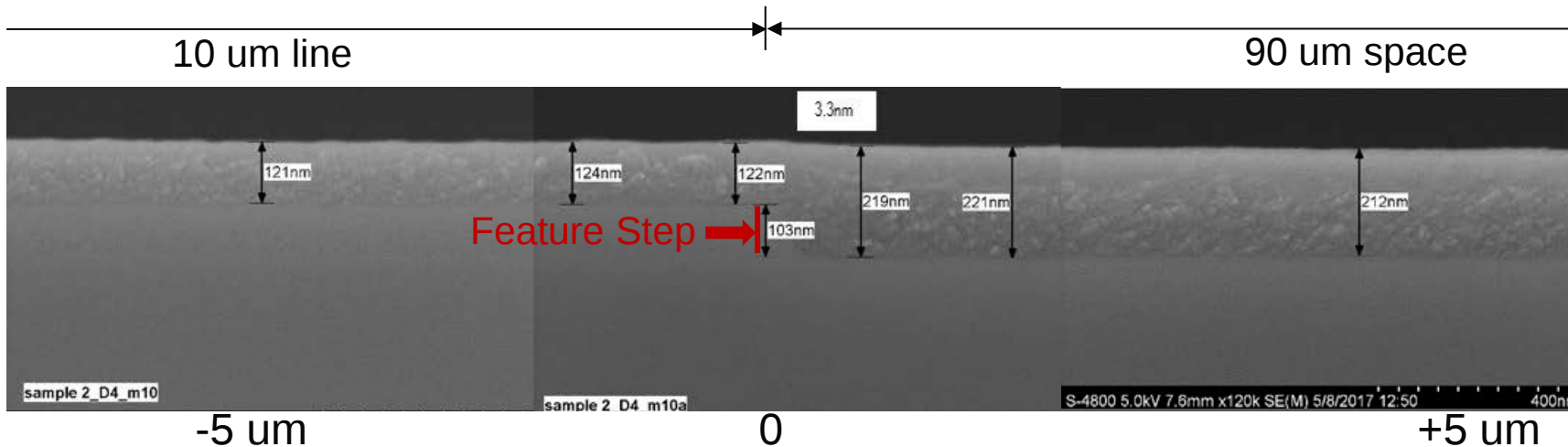
30nm HP lines



750nm HP lines



Dense and semi-dense lines

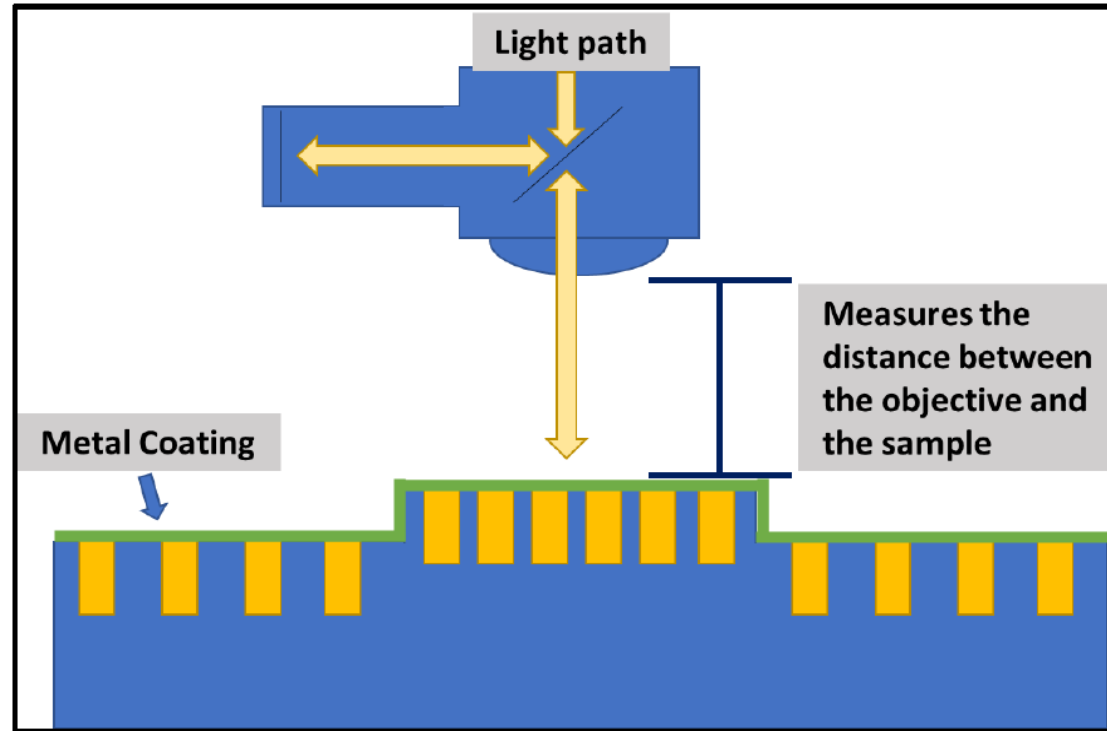


Large Area Planarization

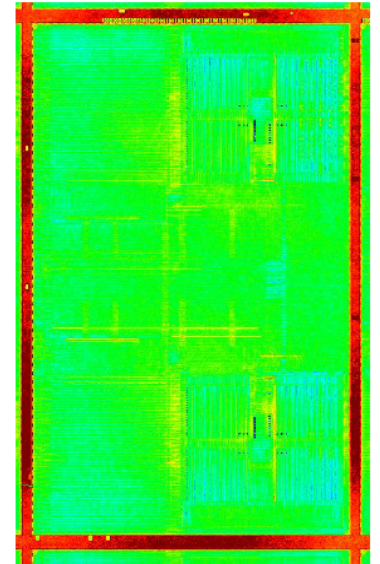
- Measuring pattern topography requires methods other than AFM or SEM x-section.

- White light interferometers, are used for high-precision, non-contact 3D surface mapping, measuring surface topography, roughness, and finish.

Interferometry Measurement



Images the entire reticle



Pixel size is $\sim 2.5 \times 2.5 \mu\text{m}$

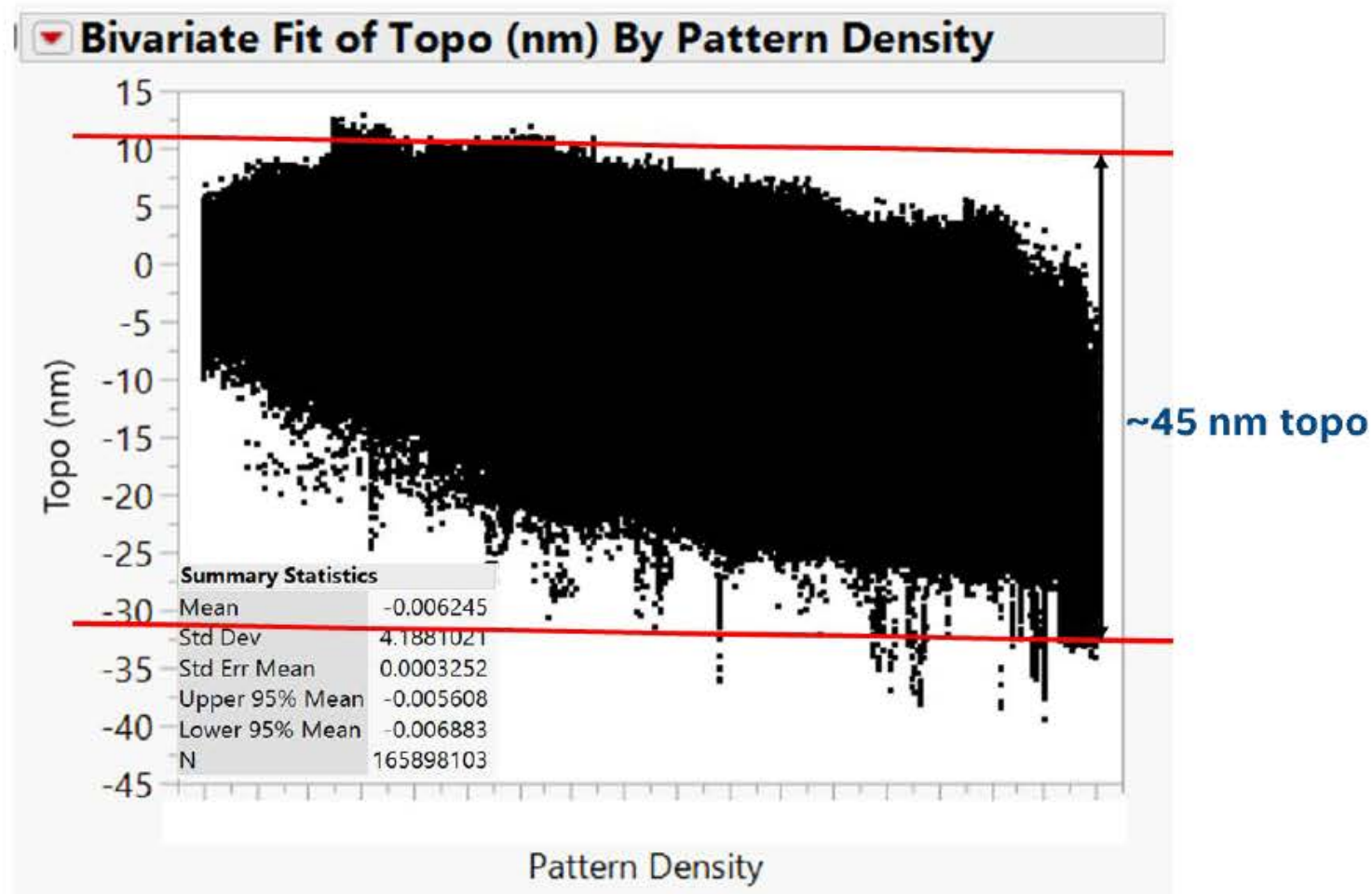
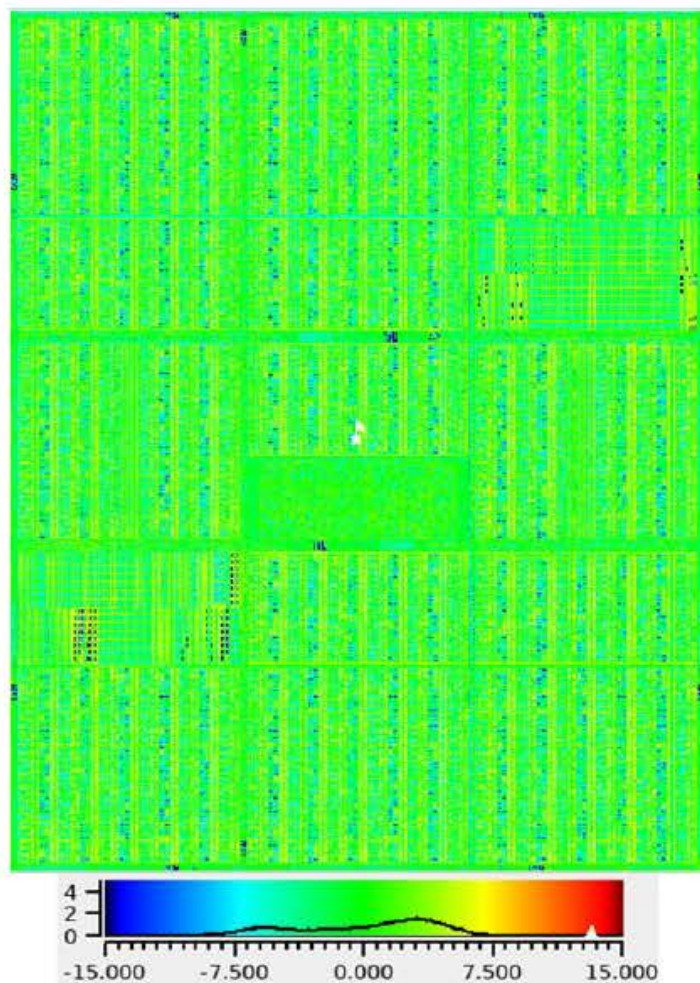
LTD Litho

Intel Confidential

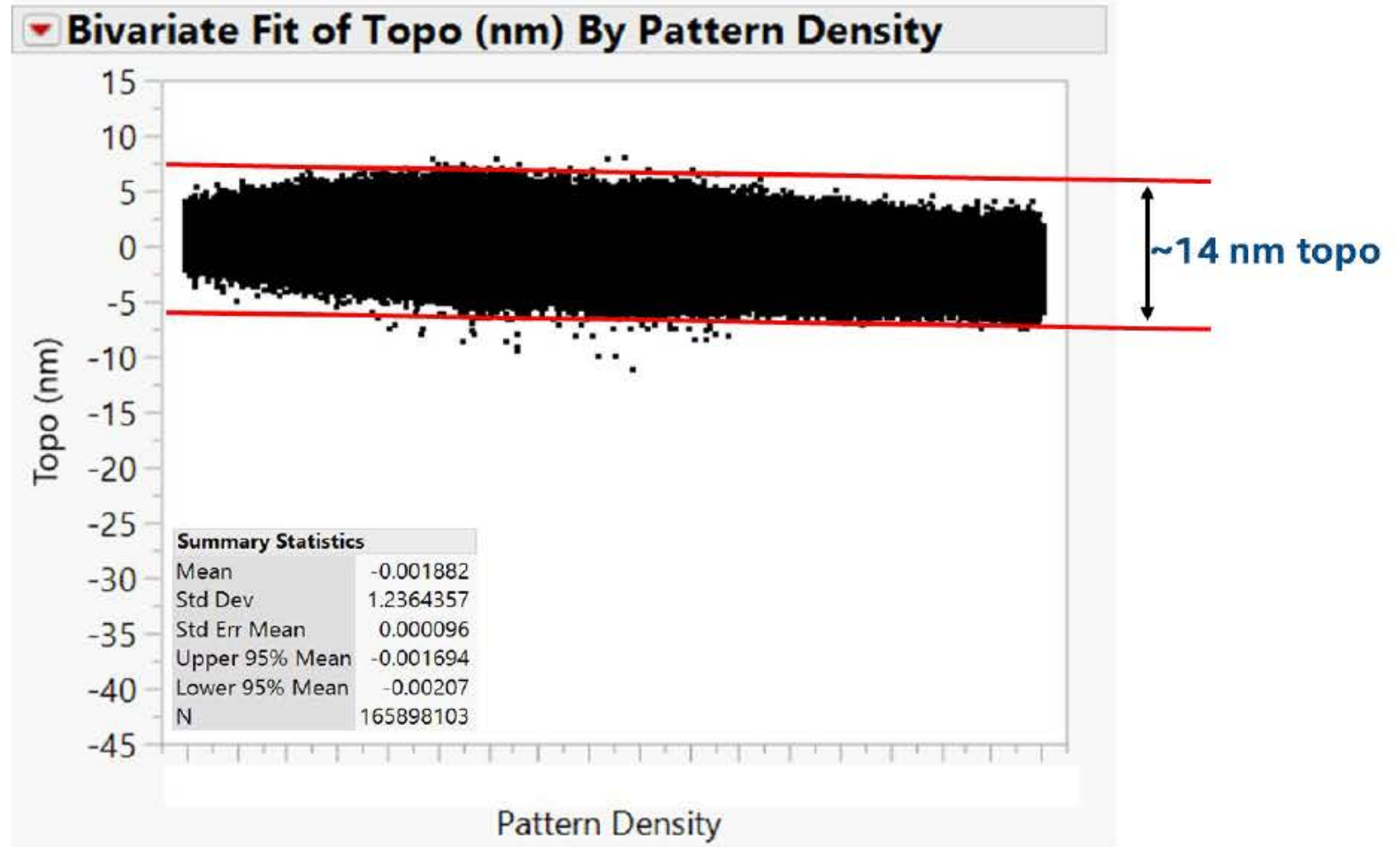
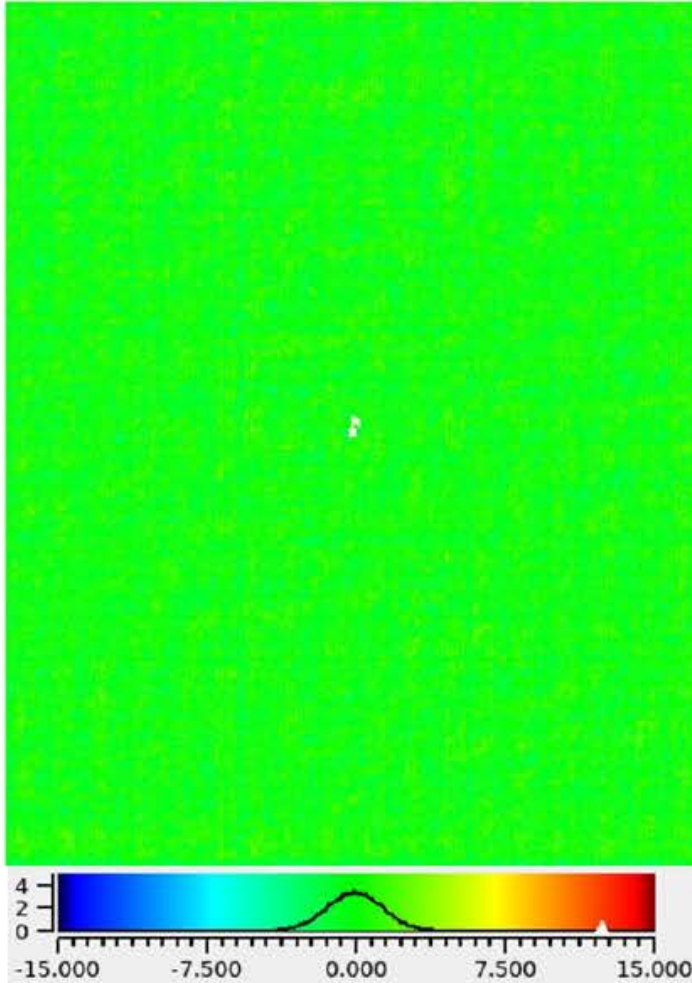
intel
foundry

Good for understanding overburden uniformity trends, but numbers reported within a single pixel are averages

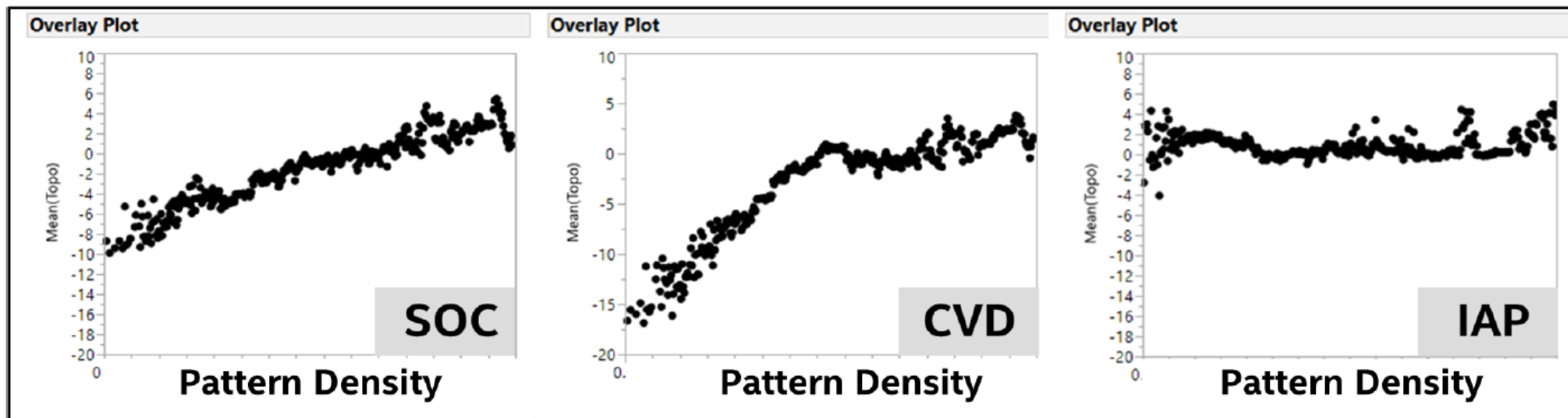
Full Field Topo with SOC



Full Field Topo with IAP – Rev 0 Recipe



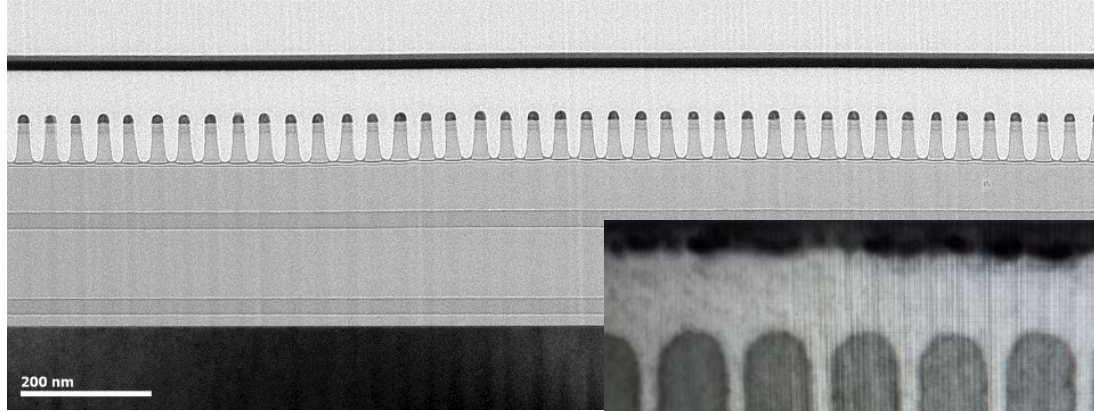
Topo vs Pattern Density



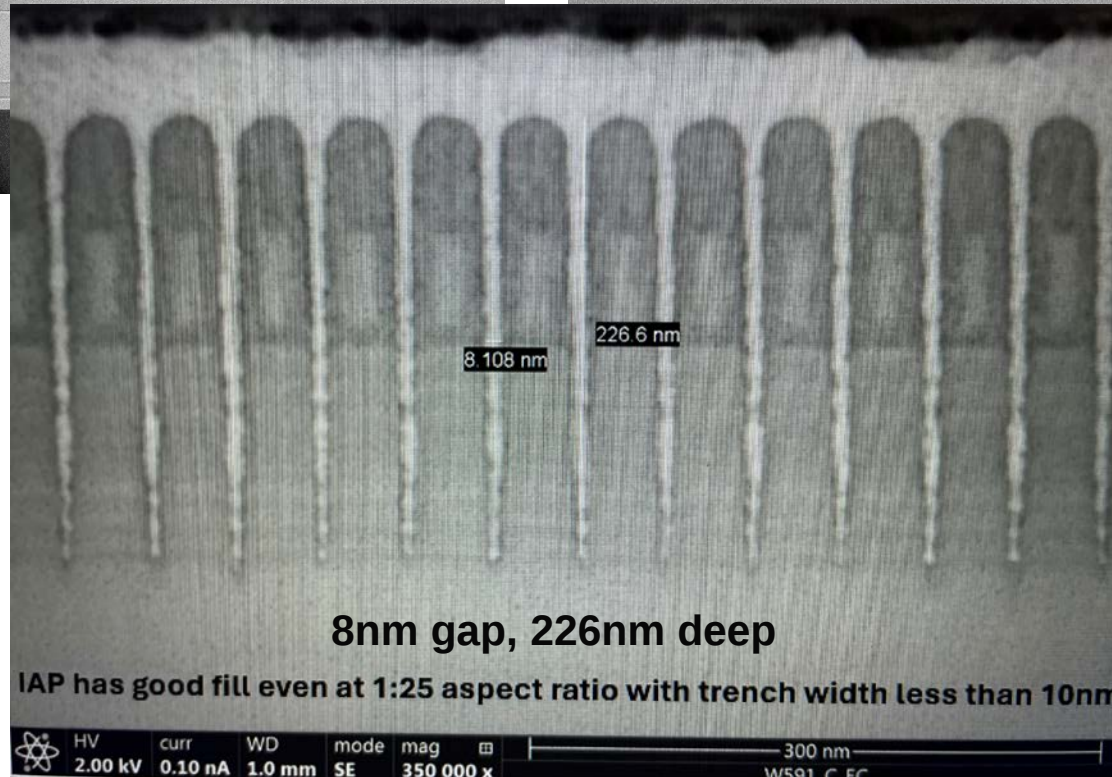
- SOC shows almost linear dependence on pattern density
- CVDs can have additional tunability for targeted pattern densities and structures but are still conformal over a larger range
- IAP shows little to no variation with pattern density

Gap Fill

20nm HP Aspect ratio~5:1



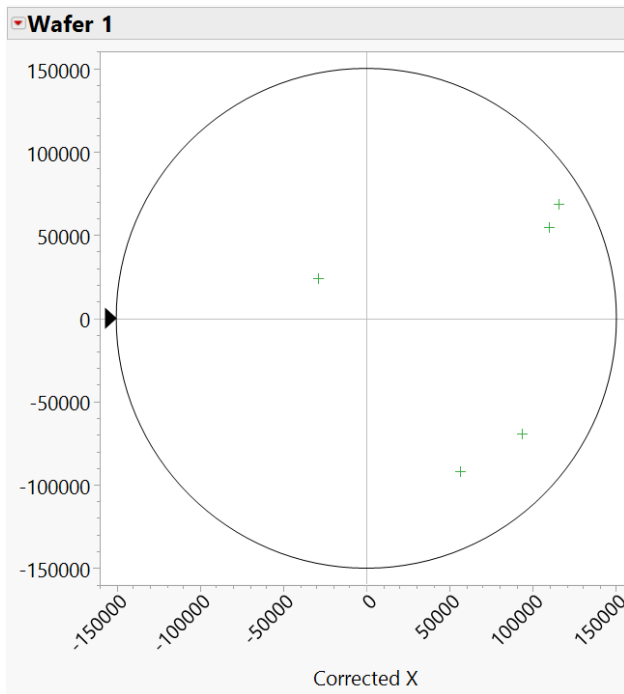
20nm and 40nm isolated lines



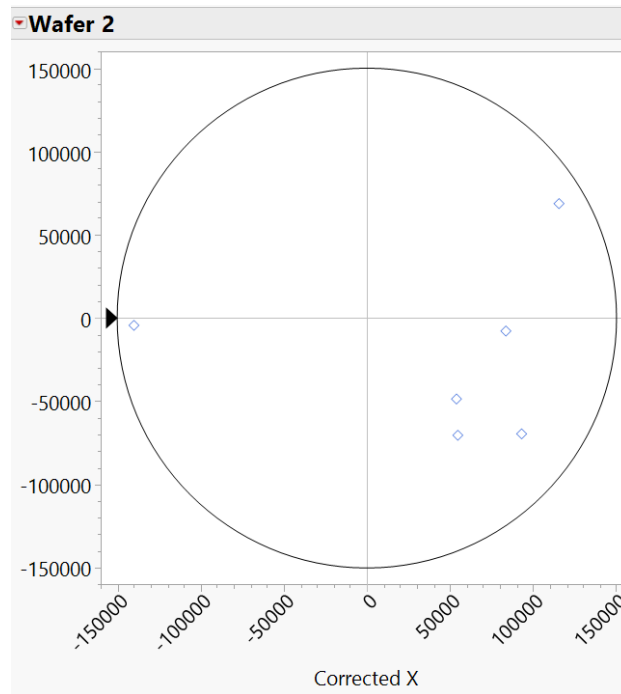
Gap fill performance is driven by the capillary force induced with thin overburden

Defectivity after IAP

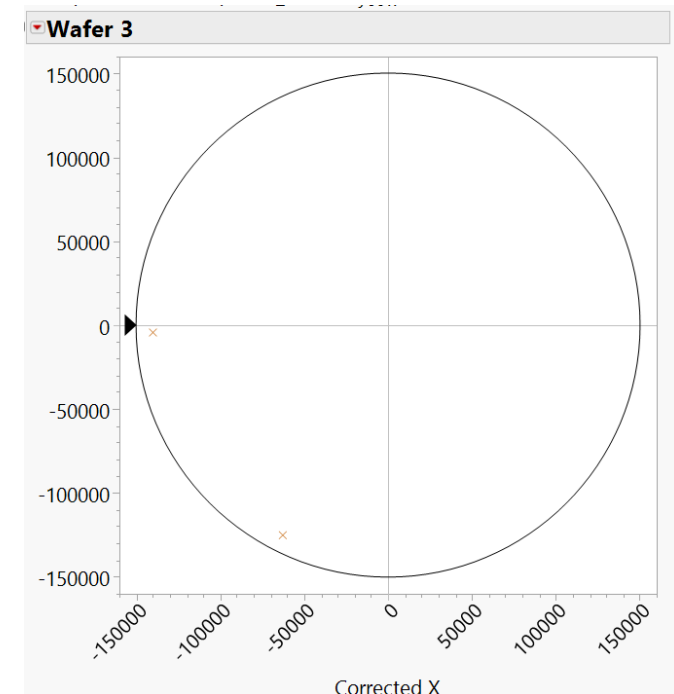
- Defectivity was also studied by applying a uniform film using IAP and using an SP7* to measure the number of defects after the process
- The defect target was $<0.01/\text{cm}^2$, meaning < 7 defects/wafer



Defect count: 5



Defect count: 6



Defect count: 2

Conclusions

Conclusions

- ❑ Two Inkjet-based technologies, were discussed
 - Nanoimprint Lithography (NIL)
 - Inkjet-based Adaptive planarization (IAP)
- ❑ NIL is challenged, from a metrology point a view, since all mask features are “1x” patterns
- ❑ Defectivity is a key metric that will decide how NIL gets used in production
- ❑ IAP is promising new technology that works with all advanced lithographic methods
- ❑ What can be done to better understand local planarization and overburden uniformity across large areas?

*Many thanks to DNP and Intel for providing some of
the data used in this presentation*

Leading the Future with Technology

CANON INDUSTRIAL GROUP