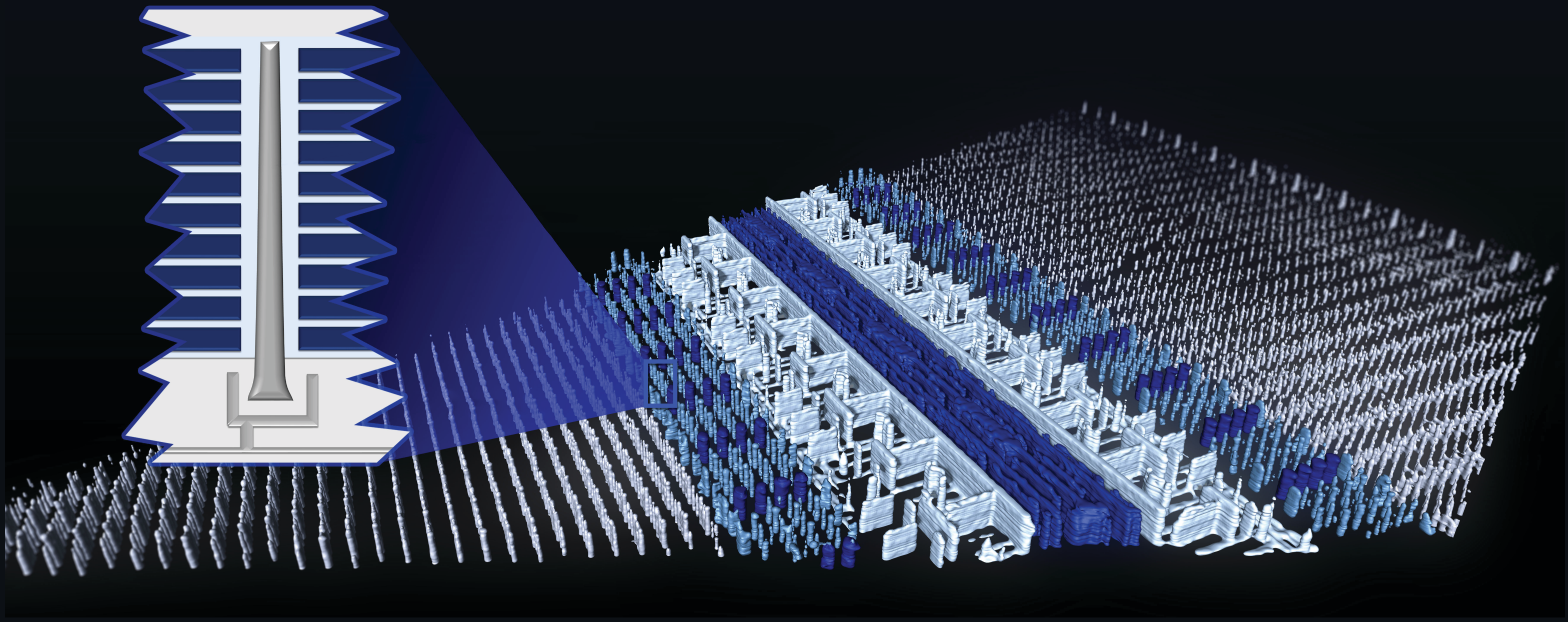
Frontiers of Characterization and Metrology for Nanoelectronics 2022

June 20-23, 2022
Monterey, California

fcmn2022.avs.org



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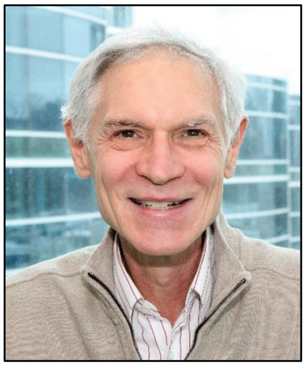

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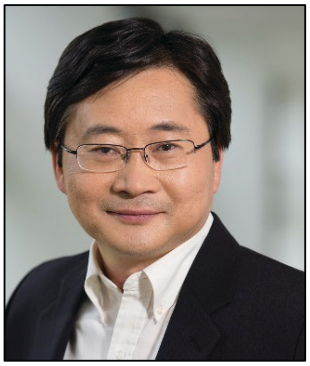

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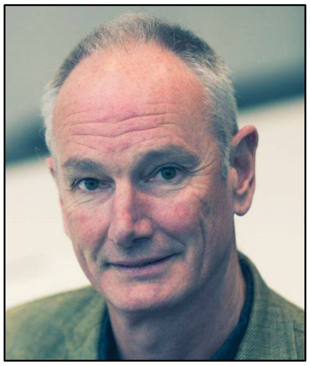
Intel



Paul van der Heide
imec

Committee Members

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- Jean-Paul Barnes, CEA-Leti
- Alan Brodie, KLA-Tencor
- Michael Current, Current Scientific
- Frank de Jong, Thermo Fisher
- Ye Feng, Intel
- Songhee Han, Samsung
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- Baohua Niu, TSMC
- Shinichi Ogawa, AIST
- Erik Secula, NIST
- David Seiler, NIST
- Usha Varshney, NSF
- Ehrenfried Zschech, deepXscan

Cover Caption: Reconstructed nano CT scan of a semiconductor memory chip from a commercial micro sd card (SanDisk 32 GB microSDHC UHS-I) measured with a sampling of 98 nm. This figure shows a 3D rendering of the internal metallized structures, where the individual contacts with an expected size between 100 nm and 200 nm can be clearly identified. Image is acquired using an Excillum NanoTube X-ray source, courtesy of Dominik Müller, Department of Experimental Physics (X-ray Microscopy), University of Würzburg.

2022 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Welcome to the 2022 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN)! Our goal is to bring together scientists and engineers interested in all aspects of the characterization technology needed for nanoelectronic materials and device research, development, integration, and manufacturing. All approaches are welcome: chemical, physical, electrical, magnetic, optical, in situ, and real-time control and monitoring. The semiconductor industry is evolving rapidly: the conference will highlight major issues and provide critical reviews of important materials and structure characterization and nearline/inline metrology methods, including hardware, data analysis, and AI and machine learning, as the industry both extends the technology deep into the nanoscale and increases the diversity of devices and systems. It is hoped that the invited talks, contributed posters, and informal discussions will be a stimulus to provide practical perspectives, breakthrough ideas for research and development, and a chance to explore collaborations and interactions on a world-wide basis.

We are pleased to have Dan Hutcheson (CEO and Chairman, VLSI Research), Rajiv Joshi (Research Staff Member and Key Technical Lead, IBM), and Jeffrey Welser (VP of Exploratory Science and University Partnerships, IBM), as keynote speakers for the event! Over thirty other invited talks will offer exciting overviews in the sessions that follow. Posters will supplement these overviews with the latest frontiers of metrology-based research results. These posters represent significant contributions to the latest developments in characterization and metrology technology, especially at the nanoscale.

The 2022 FCMN is the 13th in the series of conferences devoted to metrology frontiers for the semiconductor industry. It emphasizes the latest advances in characterization and metrology that is helping shape the future of the nanoelectronics revolution. The proceedings for many of the previous conferences in the series were published as hardcover volumes by the American Institute of Physics, New York. Most of these proceedings as well as many archived presentation slides are available to view for free on-line at www.nist.gov/pml/engineering-physics-division/fcmn-publications-and-talks.

For the third time in a row, the committee is excited to bring the FCMN to Monterey, California! Monterey is a scenic California coastal city that rises from the pristine Monterey Bay to pine forested hillsides with sweeping bay views. We hope you enjoy your time here!

It is our sincere hope that you find this conference stimulating and enjoyable!

With best wishes from the Committee Co-Chairs,

J. Alexander Liddle, NIST;
Alain Diebold, CNSE, SUNY Polytechnic Institute;
Markus Kuhn, Rigaku
Zhiyong Ma, Intel; and
Paul van der Heide, Imec

Purpose and Goals

The FCMN brings together scientists and engineers interested in all aspects of the characterization technology needed for nanoelectronic materials and device research, development, integration, and manufacturing. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed in the semiconductor industry for advancing silicon nanoelectronics and beyond.

Contributed Posters

One of the major emphases of this conference is on the contributed posters. These extended poster abstracts selected by the committee represent significant contributions to the frontier, state-of-the-art materials, and device characterization.

Poster authors are responsible for setting up their displays, being present for the poster sessions on Tuesday and Wednesday afternoon, and removing their displays by the end of the conference on Thursday.

Poster Sessions

The poster sessions with complimentary snacks and beverages are scheduled for 5:00 PM on Tuesday and Wednesday in San Carlos I and II at the Monterey Marriott.

Banquet

A dinner banquet will be held on Tuesday, Jun. 21st, at 6:45 PM in the Ferrante's Bay View Room on the 10th floor of the Monterey Marriott.

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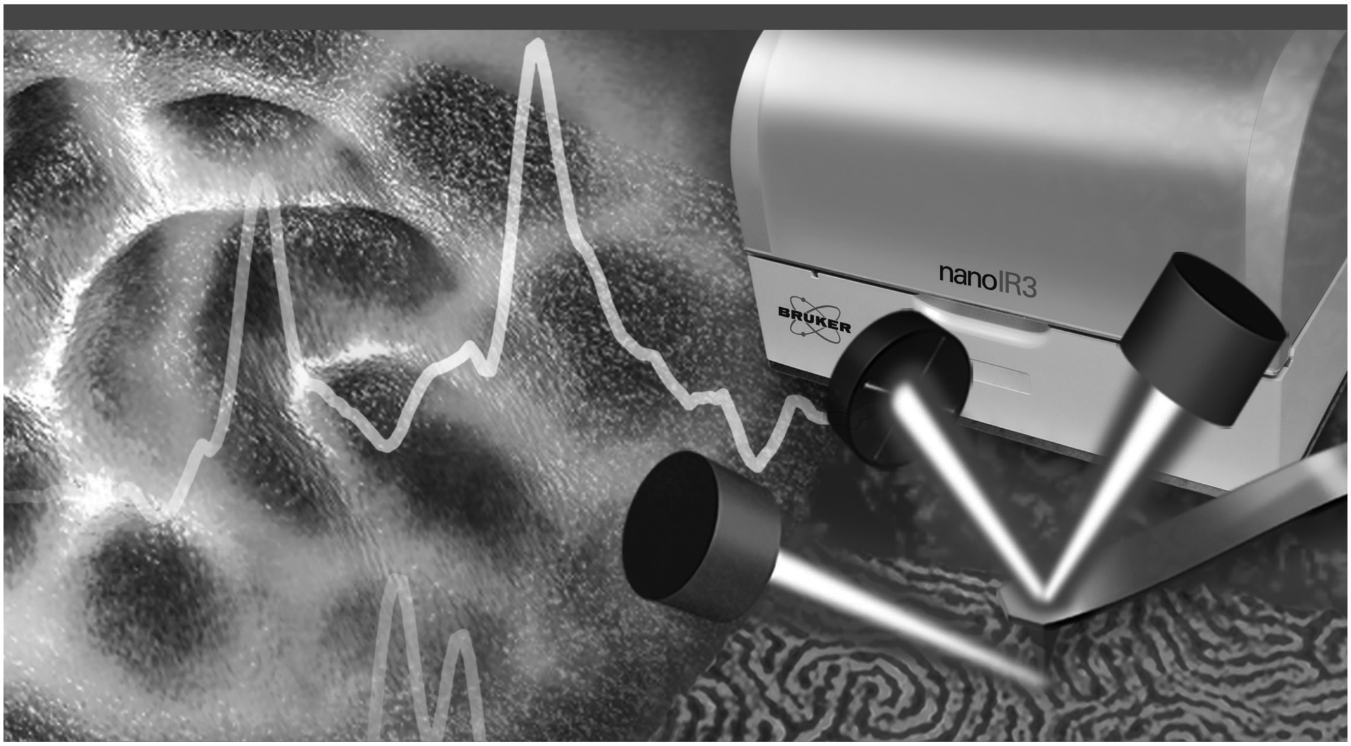
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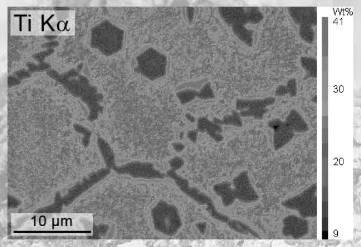
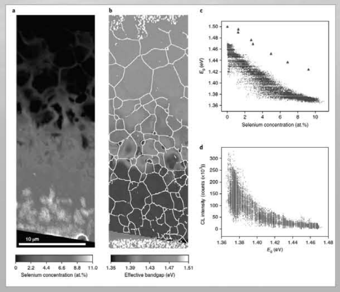
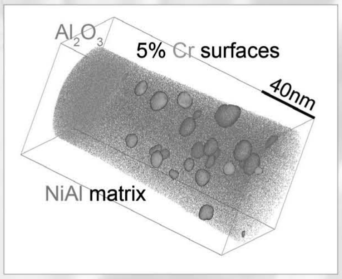
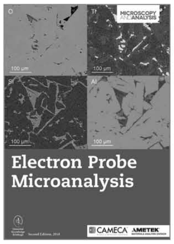
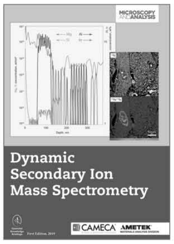
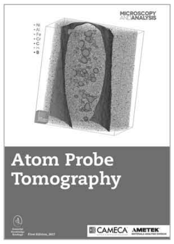

Ti Kα
Wt%
41
30
20
9
10 µm

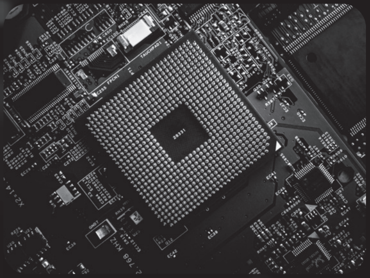

a
b
c
d
10 µm
Selenium concentration (at.%)
Effective bandgap (eV)

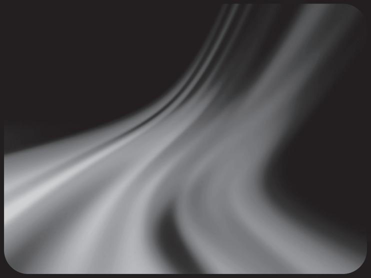

Al2O3
5% Cr surfaces
40nm
NiAl matrix

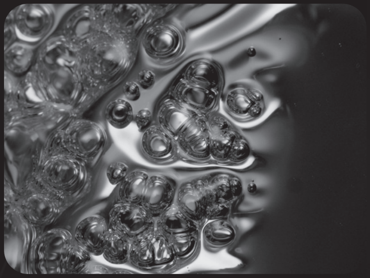

Electron Probe Microanalysis

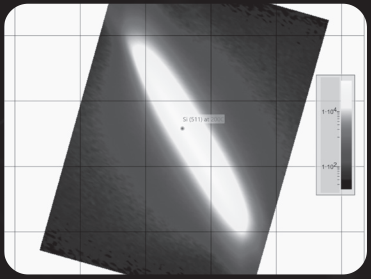

Dynamic Secondary Ion Mass Spectrometry

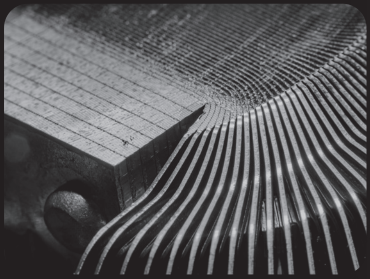

Atom Probe Tomography

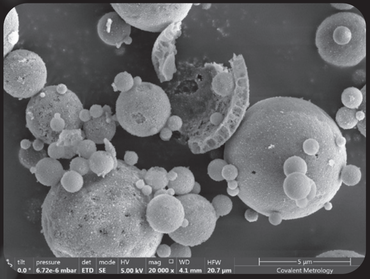


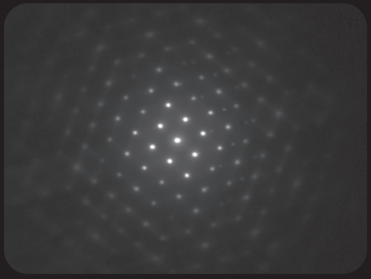


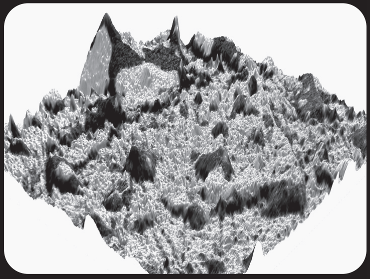










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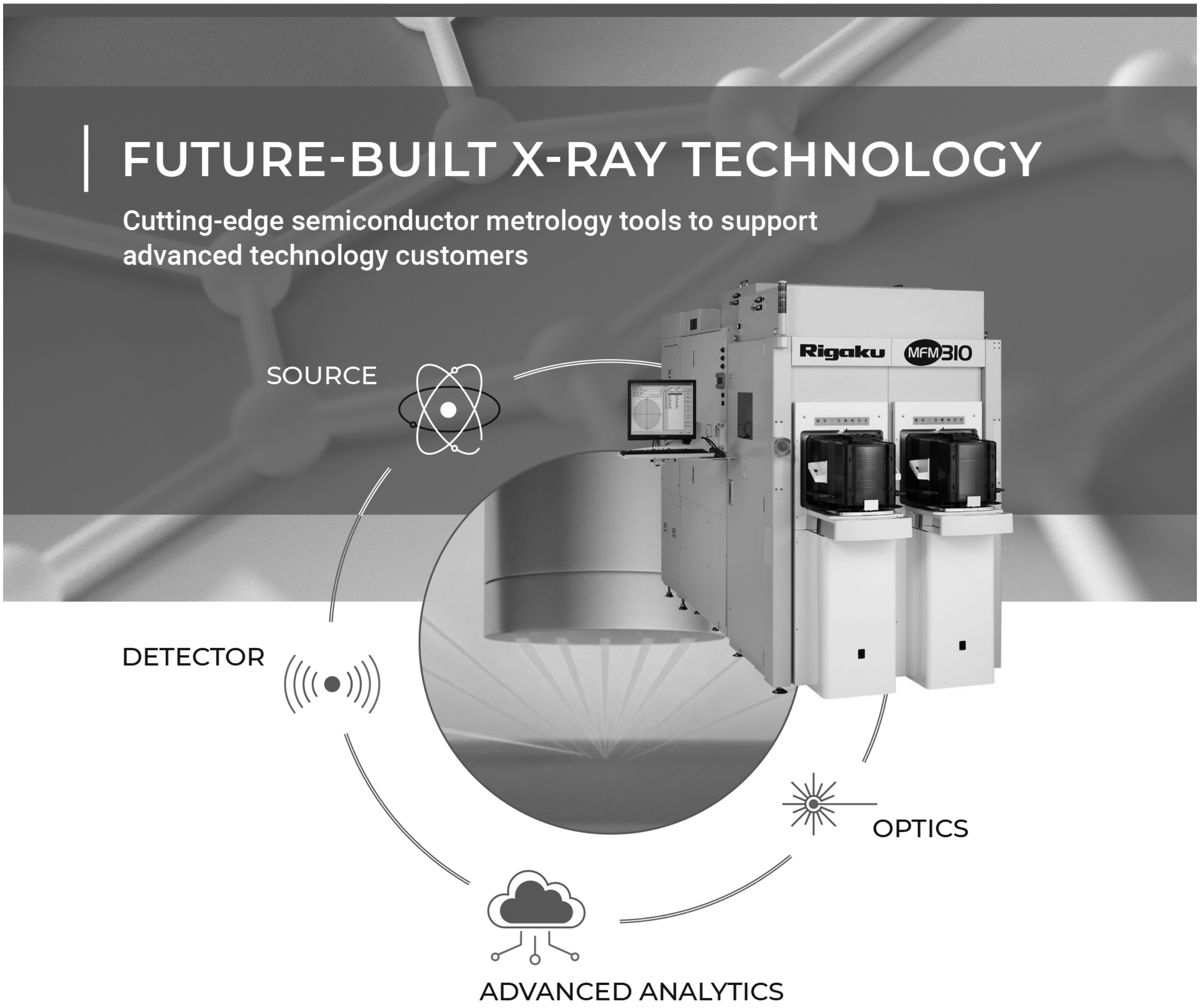
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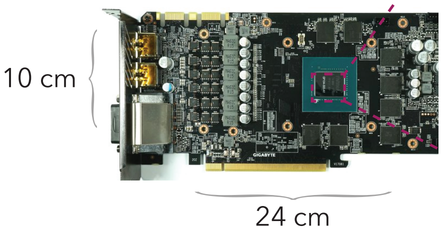

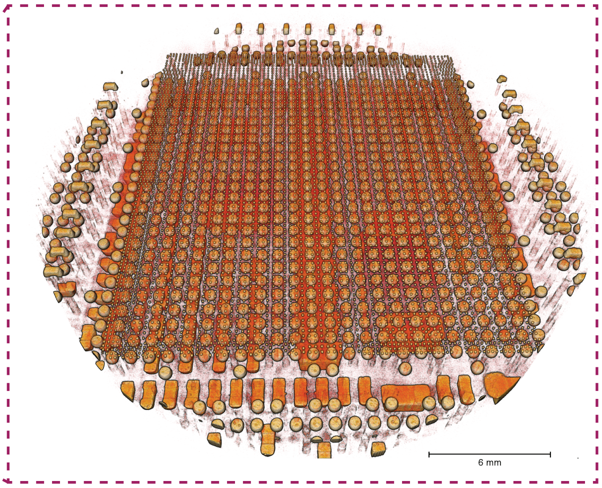

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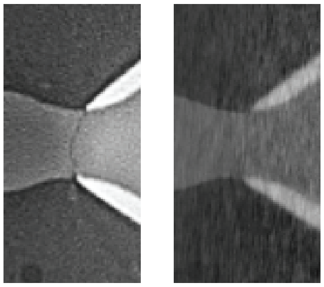

Sigray Apex

Other

Left: Crack in RDL clearly visualized in a large package with Apex XCT. Even leading XRM could not resolve.

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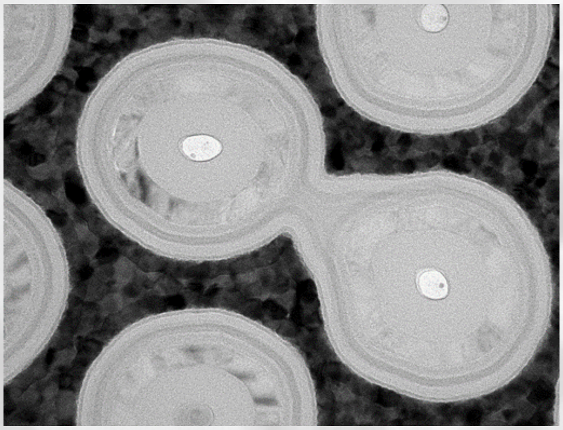
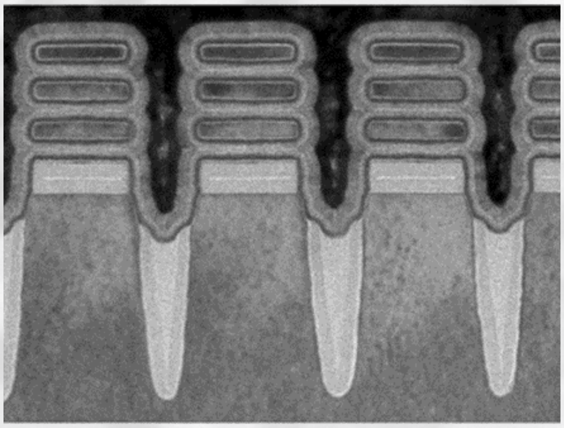
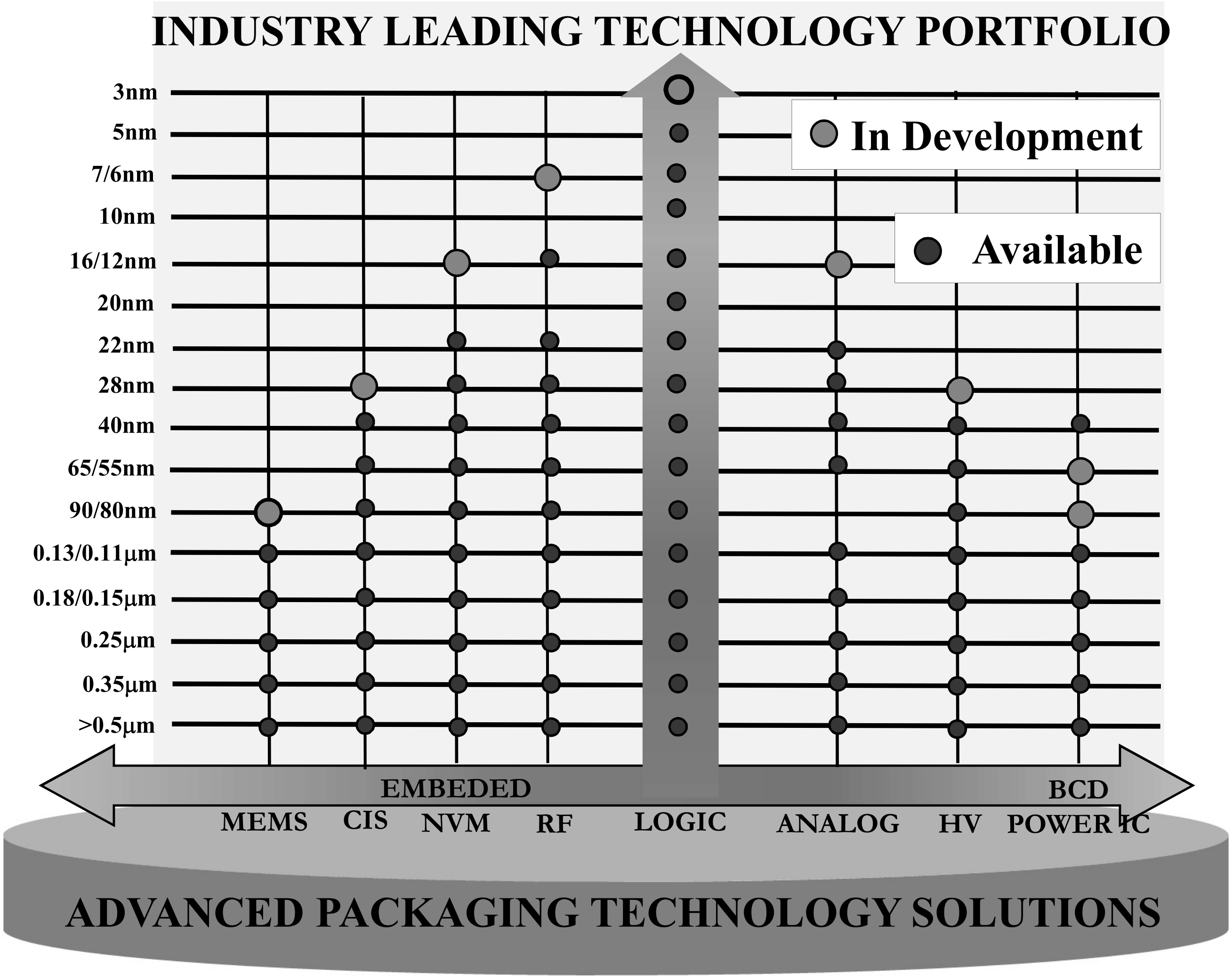
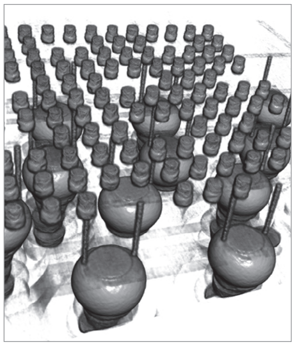


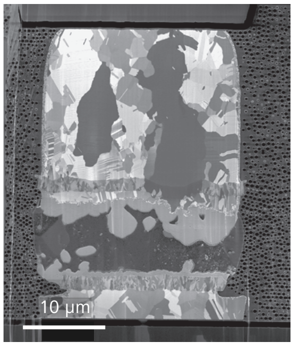
3D NAND

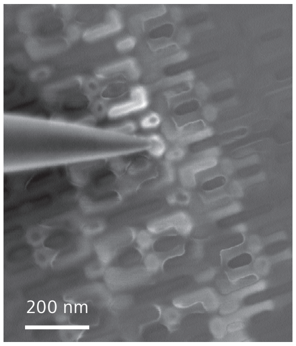


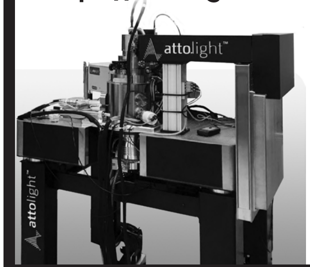
Gate-All-Around FETs


INDUSTRY LEADING TECHNOLOGY PORTFOLIO
3nm
5nm
7/6nm
10nm
16/12nm
20nm
22nm
28nm
40nm
65/55nm
90/80nm
0.13/0.11µm
0.18/0.15µm
0.25µm
0.35µm
>0.5µm
In Development
Available
MEMS
CIS
EMBEDED NVM
RF
LOGIC
ANALOG
HV
BCD POWER IC
ADVANCED PACKAGING TECHNOLOGY SOLUTIONS




10 µm


200 nm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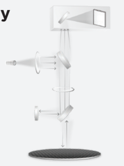
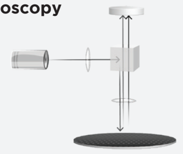
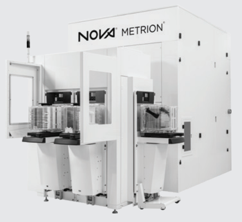



NOVA PRISM




NOVA ELIPSON


NOVA METRION

Program at a Glance

	Morning	AM Sessions	PM Sessions	Evening
Tuesday Jun. 21st	**7:00** Registration / Attendee Check-in	**9:00** Conference Opening **9:15** Plenary	**1:30** Industry Trends **3:30** Microscopies I	**5:00** Poster Session **6:45** Banquet
Wednesday Jun. 22nd	**7:45** Registration / Attendee Check-in	**8:30** Tomographies **10:30** New Developments in Chemical / Electrical Characterization	**1:30** Microscopies II **3:00** New Techniques for Emerging Devices / Beyond CMOS **3:30** Advanced Manufacturing Metrology	**5:00** Poster Session
Thursday Jun. 23rd	**8:00** Registration / Attendee Check-in	**8:30** EUV and Advanced Patterning **10:30** Advanced Packaging	**1:30** Emerging Materials and Devices **3:30** Spintronics-Based Devices	

Monday, Jun. 20

Reception and Registration

7:00 PM – 9:00 PM

Ferrante's Bay View Room, 10th Floor, Monterey Marriott

Tuesday, Jun. 21

Registration and Breakfast

7:00 AM – 8:30 AM

Conference Opening

9:00 AM

Conference Opening

J. Alexander Liddle, NIST, Conference Co-Chair

1. Plenary

Session Chairs: J. Alexander Liddle (NIST) and Alain Diebold (CNSE, SUNY Polytechnic Institute)

9:15 AM

Frontiers of Challenge = Opportunity for the Semiconductor Industry 33

Dan Hutcheson, VLSI Research

10:00 AM

Coffee Break and Poster/Exhibit Viewing

10:30 AM

From Deep Scaling to Deep Intelligence 37

Rajiv Joshi, IBM

11:15 AM

Quantum Computation with Superconducting Qubits 41

Jeffrey Welser, IBM

12:00 PM – 1:30 PM

Lunch and Poster/Exhibit Viewing

2. Industry Trends

Session Chairs: Paul van der Heide (Imec) and Markus Kuhn (Rigaku)

1:30 PM

A New Paradigm of Process Control Solutions for Advanced Semiconductor Devices. 44
Sang Hyun Han, Nova

2:00 PM

CD-Driving In-Fab High Aspect Ratio Memory Solutions with CD-SAXS. 47
Jon Madsen, KLA Corporation

2:30 PM

Advanced Manufacturing using Virtual Metrology and Equipment Intelligence 50
David Fried, Lam Research

3:00 PM

Coffee Break and Poster/Exhibit Viewing

3. Microscopies I: New Developments in Chemical/Property Characterization

Session Chairs: Markus Kuhn (Rigaku) and Songhee Han (Samsung)

3:30 PM

Latest Developments in X-ray Metrology for Semiconductor Structures 51
Juliette van der Meer, Bruker

4:00 PM

The Reverse-Sample-Tip SPM approach: A Paradigm Shift in Data Collection 56
Umberto Celano, Imec

4:30 PM

Time-Resolved Transmission Electron Microscopy from 1 Hz to 10 GHz in Stroboscopic Mode 58
June Lau, National Institute of Standards and Technology

5:00 – 6:30 PM

Poster Session (with Drinks and Hors d’oeuvres)

6:45 PM

Banquet at Hotel

Wednesday, Jun. 22

Registration and Breakfast

7:45 AM – 8:30 AM

4. Tomographies

Session Chairs: Frank de Jong (Thermo Fisher) and Ehrenfried Zschech (deepXscan)

8:30 AM

New Developments in Atom Probe Tomography 63
David Larson, Cameca Instruments, Inc.

9:00 AM

Recent Advances in Electron Tomography and Applications in the Semiconductor Industry 66
Jean-Paul Barnes, CEA-Leti

9:30 AM

High Volume 3D SEM Metrology on Advanced Memory. 69
David Tien, ThermoFisher

10:00 AM

Coffee Break and Poster/Exhibit Viewing

5. New Developments in Chemical/Electrical Characterization

Session Chairs: Paul van der Heide (Imec) and JJ Lee (TSMC)

10:30 AM

Methods for Achieving Atomic-Scale Analytical Tomography 72
Brian Gorman, Colorado School of Mines

11:00 AM

Ultra Low Energy SIMS Depth Profiling of 2D Materials 74
Sylwia Kozdra, Łukasiewicz - IMiF

11:30 AM

Photoelectron Spectroscopy in Device Technology: from XPS to HAXPES 77
Olivier Renault, CEA-Leti

12:00 – 1:30 PM

Lunch and Poster/Exhibit Viewing

6. Microscopies II: New Developments in Dimensional Characterization

Session Chair: Ofer Adan, AMAT

1:30 PM

Advanced Electron Microscopy Techniques to Investigate New Semiconductor-Related Materials and Devices. 80
Yu-Tsun Shao, Cornell Univ.

2:00 PM

2:30 PM

Coffee Break and Poster/Exhibit Viewing

7. New Techniques for Emerging Devices / Beyond CMOS

Session Chair: Ye Feng, Intel

3:00 PM

8. Advanced Manufacturing Metrology

Session Chair: Tuyen Tran, Intel

3:30 PM

4:00 PM

4:30 PM

5:00 – 6:30 PM

Poster Session (with Drinks and Hors d’oeuvres)

Thursday, Jun. 23

Registration and Breakfast

8:00 AM – 8:30 AM

9. EUV and Advanced Patterning

Session Chair: Alain Diebold, CNSE, SUNY Polytechnic Institute

8:30 AM

Soft X-Ray Scatterometry: At-Resolution, 3D Metrology for the EUV Era 93
Christina Porter, ASML

9:00 AM

Extending Optical Critical Dimension Metrology into the Mid-Infrared Range 96
Andy Antonelli, ONTO

9:30 AM

Ebeam Technology for CD and Overlay Addresses 2D Scaling Challenges and 3D Edge Placement Errors 99
Ofer Adan, AMAT

10:00 AM

Coffee Break and Poster/Exhibit Viewing

10. Advanced Packaging

Session Chairs: Ehrenfried Zschech, deepXscan

10:30 PM

Fast and High-resolution Micro-XCT and Nano-XCT Imaging of Advanced Packaging Structures Using New X-ray Sources 102
Bjoern Hansson, Excillum

11:00 AM

In-situ Micro-DCB / Nano-XCT Test to Ensure the Robustness of Leading-edge Cu/ULK BEOL Stacks . . 105
Kristina Kutukova, Fraunhofer IKTS

11:30 AM

High Throughput (<Minutes) Sub-Micron 3D X-ray for Failure Analysis & Wafer Level Packaging 108
WenBing Yun, Sigray

12:00 – 1:30 PM

Lunch and Poster/Exhibit Viewing

11. Emerging Materials and Devices

Session Chair: Jean-Paul Barnes, CEA-Leti

1:30 PM

2:00 PM

2:30 PM

3:00 PM

Coffee Break and Poster/Exhibit Viewing

12. Spintronics-Based Devices

Session Chair: Ajey Jacob, University of Southern California

3:30 PM

4:00 PM

4:30 PM

Conference End

Poster Presentations

Frontiers of Challenge = Opportunity for the Semiconductor Industry

G. Dan Hutcheson

TechInsights
2025 Gateway Place, Suite 370
San Jose, CA 95124

INTRODUCTION

The first two years of the 2020s have brought unprecedented challenges. There was COVID in 2020. Then the chip shortage in 2021. The general expectation was that 2019 would be extended. Instead, there was a strong upturn to the surprise of most. This plenary shows why the unexpected upturn came to be. It also delves into the drive for technology sovereignty, the China enigma, the Taiwan hyper-coherence issue,[1] and what it all means for metrology and inspection.

COVID AND THE GREAT IC SHORTAGE OF 2021

In 2020, COVID threw a curveball at the semiconductor industry's late 2019 recovery from the 2018 memory market bubble. By March of 2020, it looked like a drive off a cliff into the ocean to many, because if the 2008 financial crisis taught our industry anything it was that it the economy is tightly coupled to the economy. Instead, there was a decoupling from the macroeconomy. The longer-term trend towards digitization was pulled-in, as the COVID shutdown sent the world went on a war footing. The WAHE (Work At Home Economy) transformed the economy at a level unseen since America's mobilization of industry to supply the Allies in WW II. Data rates soared with demand for electronics. Central banks flooded their economies with money to avoid a repeat of 2008. This made 2020's possible.

But executives throughout multiple levels of the supply-chain reacted slowly, as confirmation bias caused them to see only the downside. Shutdown had to be bad for the economy. Data rates soaring was just a reflection of everyone sitting at home streaming entertainment series. And the central banks flooding money in? That was seen as a Hail-Mary to slow the inevitable. Worse, there was minimal data available. With the shutdowns there was zero visibility in March – 1Q 2020 results would not be available until Early May.

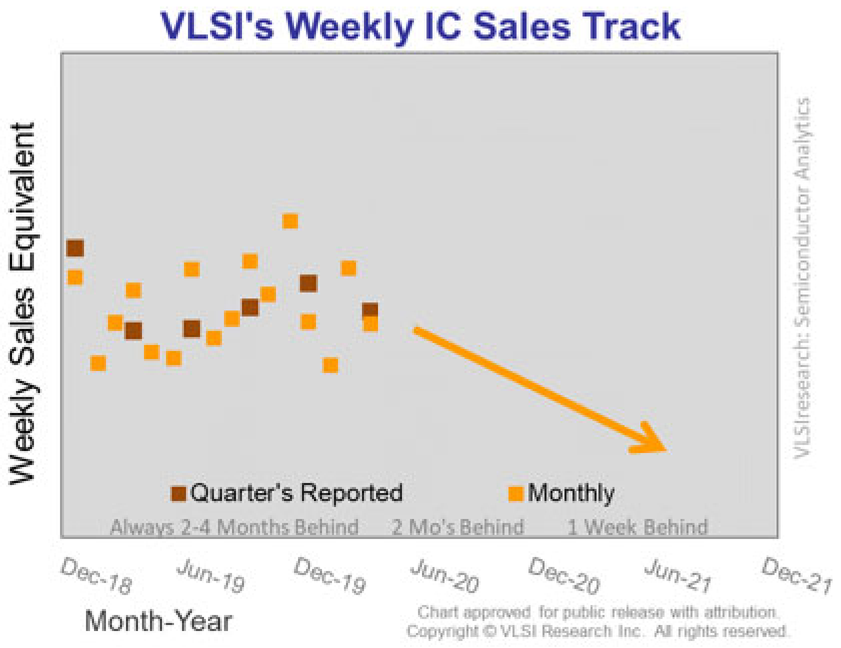


FIGURE 1. Monthly and Quarterly IC sales December 2018 to March of 2020[2]

This would set the supply-chain up for the perfect storm that would result in a massive shortage that would severely constrain the economy as it tried to recover. While the equipment market continued to grow, capacity would be constrained by lack of fab whitespace. This was particularly true for More-than-Moore fab capacity that was so essential to the auto industry. Meanwhile, the auto industry was hitting the brakes hard with the COVID shutdown.

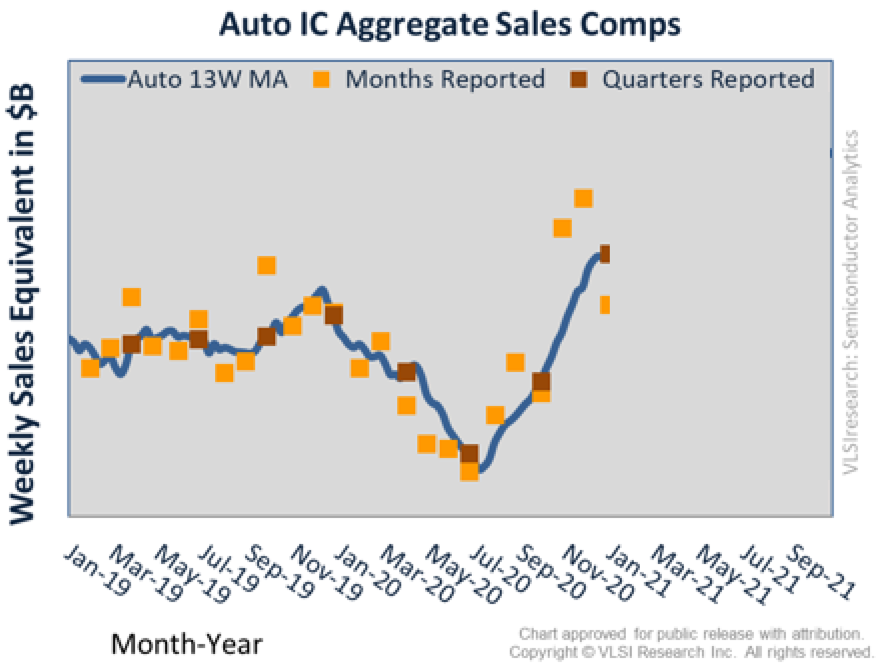


FIGURE 2. Auto IC sales: 2019 to 2020[2]

The auto industry had been ramping IC purchases towards the end of 2019, after relatively flat sales through the first three quarters of the year. Then they slashed IC buys severely deep into mid-year as vehicle sales slowed with the COVID shutdown. Then as the shutdown eased, people got bored with streaming, they wanted to drive somewhere, had plenty of government money in their pockets, and wanted a new car. They began to use up IC inventory as they ramped production. As they used up inventory, IC production was not rising fast enough due to the extreme complexity of their supply chain. It's five levels and their low visibility into due to minimal contact with foundries would result in vehicle assembly line shutdowns and soaring used car prices:

1. Auto suppliers who buy from…
2. Module suppliers who buy from…
3. Distributors who buy from…
4. IC suppliers who buy from…
5. Foundries

In the end, the shortage would be good for the semiconductor industry. 2021 semiconductor sales would blow past a half-a-trillion dollars and Logic a quarter-of-a-trillion! To paraphrase, Sean Parker's famous quote, 'A Billion is no longer cool for the chip industry. Now … only a Trillion Dollars is cool.'[3]

The impact of COVID and the shortage on the market for Process Diagnostic Tools soared. Growth in 2020 and 2021 was almost 30% year/year and was four times the 15-year average between 2005 and 2019.In 2021, the size of the Process Diagnostic market reached $10B for the first time and was double that achieved five years earlier. Of course there are important factors driving this growth beyond COVID and the shortage. The end of the 300mm holiday, the failure of the industry to bring 450mm to market, and a new drive to displace test-in quality with built-in quality for reliability reasons are important ones. But they too lengthy and not in the scope of this document to write about here.

THE DRIVE FOR TECHNOLOGY SOVEREIGNTY

The drive for Technology Sovereignty is a response to the death of globalization in 2016. President Xi Jinping and China's 13th Five Year Plan to lead the semiconductor industry by 2030 infected globalization in 2015.[4] President Donald Trump became the super-spreader in 2016 with his administration's aggressive anti-trade policies. Out of this tension arose multiple government efforts to counter China, including the CHIPS act in the U.S. These tensions were made worse by the IC shortage as the world began the realize the hyper-coherence risk of a supply chain so dependent on Taiwan for leading edge capacity. And it's not just Taiwan. Taiwan and Korea combined represented roughly half of the world's semiconductor production in 2021. The EU and US have been losing share since the 1960s and now are minor players. Japan peaked around 1990 and has been declining since. Meanwhile, China reached parity with the US in 2020 and is rising fast. With the world woken up by the auto IC shortage to the importance of semiconductors, Technology Sovereignty has become a major geopolitical issue in this decade.

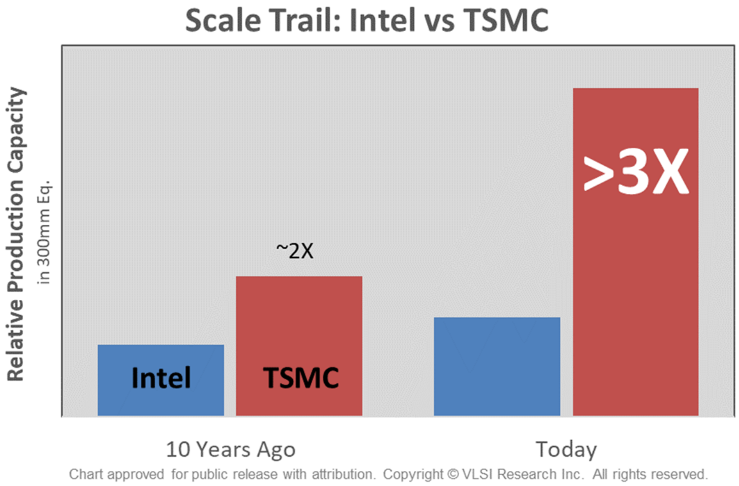


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FIGURE 3. Relative Production Capacity, past and present, TSMC vs. Intel[1]

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KEYWORDS

Semiconductor, Market, Trends, COVID, Chip-Shortage, Inspection Market, CHIPS-act

From Deep Scaling To Deep Intelligence

(Plenary Talk)

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Extended Abstract

Historically, transistor scaling provided higher performance, lower power, and lower cost-per-transistor. Technology-Circuit-System co-design really helped to deliver low power, high performance nano processors. Innovations in process and devices have been essential for scaling and for extending Moore's Law as show in Figure 1[1]. Process technology has implemented continual transitions from bipolar to CMOS, voltage and power-efficient scaling, and System-on-Chip design. Significant processing innovations in CMOS include tungsten plugs, trench isolation, CMP (chemical mechanical polishing), copper interconnects, strained silicon, high-κ/metal gates and 3D devices like FinFETs. The introduction of strained silicon increased transistor drive currents. High-κ/metal gates reduced standby leakage and helped improve heat dissipation. FinFETs addressed limitations of electrostatics and short-channel effects. Beyond FinFET, nanowires and nanosheet technology with gate-all-around [2] is expected to control the short channel effect which is a major problem under technology scaling. IBM's recent announcement of Vertical Transport FET (VTFET) would allow further scaling to 2nm [3]. Also interconnect technology has made significant progress from the introduction of low k dielectric to airgaps in dielectrics to improve performance. Another major emerging development is related to the use of buried power rails to simplify the backend stack, deliver robust power, improve chip area and pin access capability as shown in Figure 2 [4,5].

On the system side, dual-core to multi-core activity drove parallelization of system architecture and thereby enhancing performance. Circuit techniques such as power gating (where a transistor is used between the supply and main functional blocks) to reduce static power, and dynamic voltage scaling (i.e. reducing supply voltages on demand) for reducing dynamic power were introduced. However, functionality, performance, bandwidth and yield for SRAM became a major issue in the nm era. To address these issues, read/write assist techniques were introduced, along with dual power supplies for arrays versus peripheral logic, and the utilization of thin cells and shorter bitlines [6].

As deep learning and artificial intelligence (AI) workloads rose in prominence in the 2010s, specialized hardware units were developed or adapted from existing products to accelerate AI tasks [7]. Various AI accelerators are shown in Figure 3; in this domain, performance is strongly dependent on memory bandwidth. Memory efficient algorithms are critical as well. Internet of things (IoT) devices are expected to generate zeta-bytes of data and need efficient algorithmics and compute platforms for analysis and prediction. To increase the bandwidth and resolve the memory wall in broadly memory-critical AI accelerator context, e-DRAM was introduced along with high bandwidth memory (HBM) with DRAM stack [8]. However, DRAMs are slower and dissipate power due to the refresh process [9]. Figure 4 shows a new emerging approach for improving performance and power by marching towards the use of 3D caches and other memories [10].

To further improve the memory bandwidth as well as reduce power a wide variety of non-volatile memories (NVM) have been explored across industry and academia [11]. Types of memory that have received significant attention include Resistive RAM, Phase Change Memory (PCM), Ferro-electric RAM (FeRAM), as well as others (Figure 5). However, one of the key problems for further scaling of new technologies and memories (VM or NVM) is variability due to process, voltage and temperature conditions (PVT). The variability in memory devices and materials affects performance, power, functionality and yield. Achieving high yield requires detailed analysis and accuracy in modeling at the tails of parametric distributions. Conventionally, the Monte Carlo technique is used to analyze yield. However, this approach is extremely time-consuming, especially for analyzing the tail regions of the distribution. Our novel techniques based on Mixture Importance Sampling (MIS) shown in Figure 6 overcame majority of the problems associated with the baseline Monte Carlo approach, and predicted critical parameters and circuits degrading macro yield [12]. MIS employs uniform sampling for the generating center of gravity (COG) for failures and subsequently shifting the distribution to the COG, followed by importance sampling. This technique thus effectively allows sampling in the tail region, improving simulation time over six orders of magnitude compared to Monte Carlo analysis. Many machine learning techniques are also employed in conjunction with uniform sampling to further improve the runtime [13]. Major variation can occur through some or all of these key parameters - Random Dopant Fluctuation (RDF), Metal Grain Granularity (MGG), and Line Edge Roughness (LER) [14]. The back end of the line (BEOL) or interconnect variations also add to variability (Figure 7). Such critical parameters and their variations need to be captured accurately over large sample sizes.

For measuring parametric variation accurately and assigning this variation's distribution in a statistically correct manner over large numbers of samples, metrology is a key step. High quality metrology requires sophisticated instruments such as X-ray, Electron Microscopy, spectroscopy, scatterometry, taking the I-V characteristics of thousands of devices, and many other techniques. Such measurements generate large amounts of data which must be analyzed in-situ with efficient feedback on mean and distributions needed for yield analysis. It is in this context where ML and AI techniques can play a critical role. Noack et al have outlined methodology addressing this space using AI automation, in particular showing how X-ray analysis data can be analyzed autonomously [15]. They have developed an autonomous decision-making algorithm that is physics-agnostic, generalizable, and operates in an abstract multi-dimensional parameter space (Fig 8).

Recently developed methodology to measure the local critical dimension uniformity (LCDU) using optical scatterometry with machine learning is described in [16]. The reference data used to train the machine learning algorithm were obtained by analyzing critical dimension scanning electron microscopy (CDSEM) images with subsequent filtering to remove outliers and mitigating the differences related to the number of vias measured with each tool. This approach corroborates and validates the accuracy of the machine learning technique for post development and post etch. It also proves that the technique is suitable for in-line characterization (see Figure 9 for application of this technique).

In summary, as we march from deep scaling to deep intelligence, AI-driven techniques to improve automation in analysis, optimization and prediction via metrology to enhance yield is extremely critical.

The expected wish list from metrology should cover material characteristics (microstructure, mechanical, thermal and electrical properties and variation), geometric analysis (such as length, width, diameter and their mismatches etc) for front and back end of the line structures. Generating accurate models from the beginning and end of life reliability from inline, offline and field measurement from machine learning techniques would be key. Early prediction of failure and learning to improve the technology would immensely help to reduce production time and improve product robustness

Acknowledgements

Management support and useful discussions with Daniel Schmidt and Mary Breton are well appreciated.

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Keywords

Deep Scaling, Machine Learning, predictive analytics, LER, MGG, Yield, AI Automation

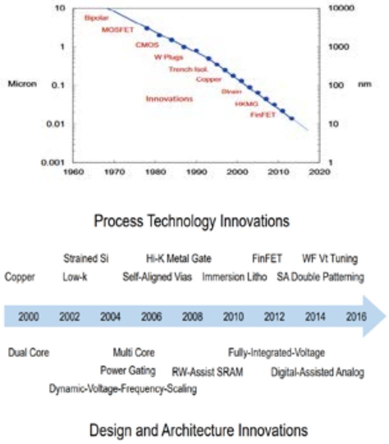


Fig. 1 Key Technology-Circuit-Systems Innovations [1]

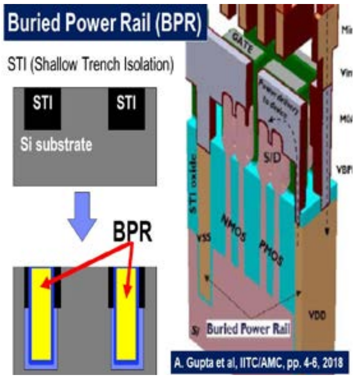


Fig. 2 Buried power rail [4]

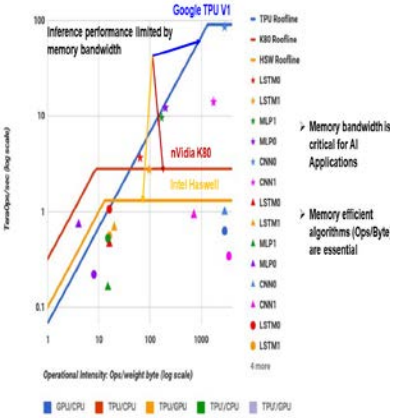


Fig.3 Stars are for the TPU, triangles are for the K80, and circles are for Haswell. All TPU stars are at or above the other 2 rooflines [7]

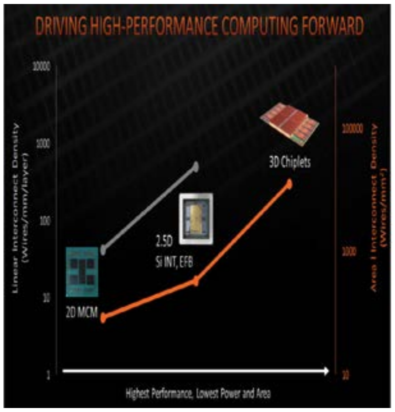


Fig.4 3D Roadmap from AMD [10]

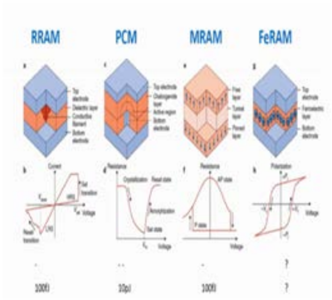
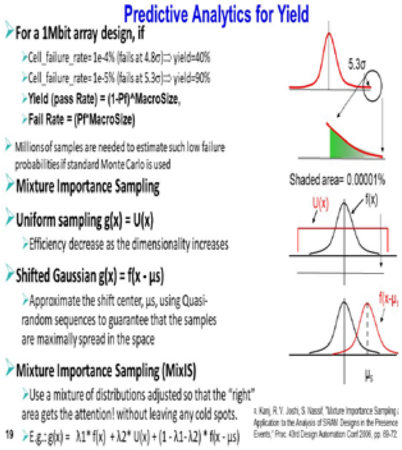


Fig.5 Non-Volatile Memories [11]


Predictive Analytics for Yield

- For a 1Mbit array design, if
  - Cell_failure_rate=1e-4% (fails at 4.8σ)⇒ yield=40%
  - Cell_failure_rate=1e-5% (fails at 5.3σ)⇒ yield=90%
  - Yield (pass Rate) = (1-Pf)^MacroSize,
  - Fail Rate = (Pf*MacroSize)
- Millions of samples are needed to estimate such low failure probabilities if standard Monte Carlo is used
- Mixture Importance Sampling
- Uniform sampling g(x) = U(x)
  - Efficiency decrease as the dimensionality increases
- Shifted Gaussian g(x) = f(x - μs)
  - Approximate the shift center, μs, using Quasi-random sequences to guarantee that the samples are maximally spread in the space
- Mixture Importance Sampling (MixIS)
  - Use a mixture of distributions adjusted so that the "right" area gets the attention! without leaving any cold spots.
  - E.g.: g(x) = λ1* f(x) + λ2* U(x) + (1 - λ1-λ2) * f(x - μs)

19

Fig.6 Predictive Analytics [12]

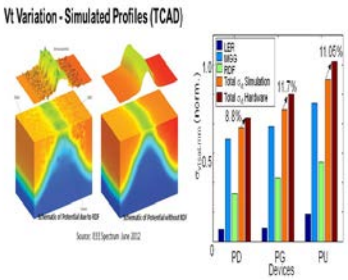


Fig.7 Key Factors affecting device Variability [14]

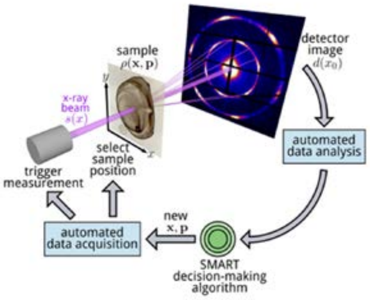


Fig.8 Schematic of an autonomous x-ray scattering experiment. Automated AI application [15]

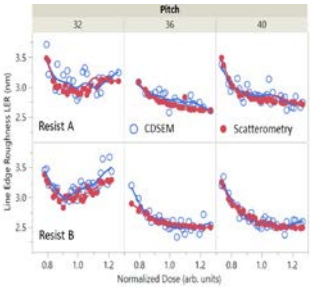


Fig.9 Line edge roughness as measured by CDSEM (open circles) and scatterometry machine learning (solid circles) [16]

Quantum Computation with Superconducting Qubits

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INTRODUCTION

Forty years ago, Richard Feynman asked: “What kind of computer are we going to use to simulate physics?” His answer was a new kind of computer capable of exploiting quantum mechanics, called a quantum computer. Further research has demonstrated that a large enough quantum computer could solve problems across industries from materials science to machine learning that are intractable to today’s most powerful supercomputers.

IBM is developing cloud-based quantum processors using the superconducting transmon qubit architecture, where transmon qubits are quantum anharmonic oscillators with nonlinearity introduced by the presence of a Josephson junction. To date, IBM Quantum has released 24 processors with as many as 127 superconducting qubits by adapting lessons from semiconductor signal delivery and packaging into a technology node for maturing and scaling quantum hardware. Simultaneously, IBM Quantum is developing a runtime environment for co-located quantum and classical systems to support containerized execution of quantum circuits at speed and scale, while fostering a global community of over 400,000 quantum computing users.

MATURING SUPERCONDUCTING QUBITS

A core goal for the industry is to maximize the amount of useful work that a quantum computing system can accomplish by increasing performance on three fronts: scale, quality, and speed. IBM feels that superconducting qubits are a natural choice for high-performance quantum computation as the only quantum architecture that can excel at all three of these attributes.

Scale, Quality, and Speed

Each of these three performance attributes comes with a corresponding metric. Scale is measured by number of operational qubits, indicating the amount of information that we can encode into a quantum processing system. Improving the scale of a quantum processor requires developing higher coherence, higher reliability, and lower cost qubits. The IBM Quantum development roadmap details a plan to employ agile hardware development processes and knowledge gleaned from semiconductor development in order to increase the scale of quantum processors to over 4,000 qubits by 2025 with the help of chip-to-chip couplers and quantum communication links.

Quality is measured by Quantum Volume, or how faithfully hardware can implement quantum circuits. Quantum Volume is a measure of the largest square circuit that a quantum processor can successfully run. Improving Quantum Volume requires improvements in gate fidelities, implementation of error mitigation (and ultimately error correction) strategies, improvements to classical resources such as the compiler, and more. Today, IBM Quantum operates systems with Quantum Volumes as high as 256, with plans to at least double the Quantum Volume annually and a promise to achieve QV 1024 by year end 2022.

Speed is measured by CLOPS (Circuit Layer Operations Per Second), or how many circuits can run on hardware in a given time. Increasing CLOPS requires seamless synchronization of quantum and classical circuits in order to increase the circuit execution rate. Today, IBM Quantum operates systems with CLOPS as high as 2,900, with increases projected thanks to improvements in signal delivery and readout, better orchestration of near-time and real-time classical compute alongside co-located quantum processors, and more.

IBM Quantum is confident that superconducting qubits present a fast, scalable, and high-quality architecture capable of scaling to large-scale systems, and are therefore the optimal architecture on which to achieve high performance on all three of these metrics.

The IBM Quantum Development Roadmap

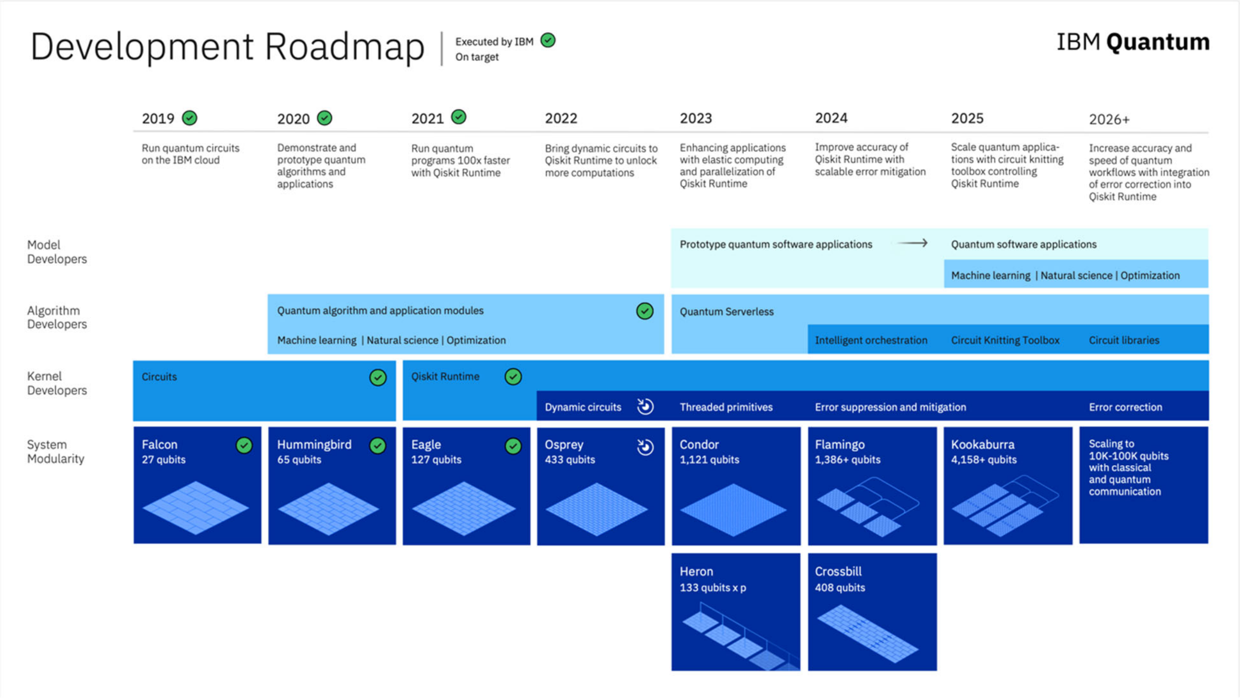

FIGURE 1. The IBM Quantum Development Roadmap

IBM Quantum has published a development roadmap (Figure 1) to keep the quantum computing community informed of our progress and plans. We have achieved or surpassed all the goals set for 2020 and 2021 in the first draft of the roadmap, including releasing the 127-qubit IBM Quantum Eagle processor, introducing the Qiskit Runtime programming model and service, and releasing quantum algorithm and application modules. The initial focus areas for our algorithms are for applications in natural science, machine learning, and optimization. The goal is to build a software stack that enables frictionless development, by eventually delivering Quantum application services to model developers and end-users.

This year, the team has extended that roadmap to 2025 with a plan for scaling quantum processors well into the future, while laying the groundwork for quantum-centric supercomputing. The roadmap also features a plan to utilize these increasingly large processors with dynamic circuits, threaded primitives, and error suppression techniques. Ultimately, IBM Quantum envisions a future of serverless quantum computation, with intelligent orchestration of jobs between CPU, GPU, and QPU resources.

CONCLUSION

Superconducting quantum processors sit at the center of a broader mission at IBM Quantum to develop full-scale quantum computers capable of solving hard classical computing processor. The team must continue to focus on improving processor scale, quality, and speed while following along the development roadmap. Looking further afield, continued improvement along this track will lead to further development in cryogenic infrastructure plus error mitigation and suppression techniques, and eventually error correction required for quantum computers to run production quantum algorithms.

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KEYWORDS

Quantum computing, superconducting qubits, transmon, IBM Quantum, Josephson junction

A New Paradigm of Process Control Solutions for Advanced Semiconductor Devices

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INTRODUCTION

The many achievements in performance and in scaling of semiconductor devices over the past ten years has further fueled eager demand for high-end applications, intensifying the focus on diversity and scaling of high-performance semiconductor device designs. Logic devices evolved from finfet to nanosheet architecture, in search of greater improvements in transistor performance and design flexibility [1,2]; NAND devices successfully broke through previous scaling limitations faced by 2D NAND devices by innovating to 3D architectures [3], continuously stacking word lines vertically to increase memory density with better performance [4]. In parallel, the need for high-performance DRAM devices drove adoption of pitch scaling and new processes to meet industry demand, leading to the development of various application-specific DRAM platforms for more efficient, customized systems [5].

These new, complicated processes diminished margins, making it increasingly difficult to maintain yield and reliability. Securing wide process margins requires precise process control below the sub-nano scale. However, ongoing challenges of accurately detecting process variations of sub-nano scaling continue to widen the gap between chip makers' performance requirements and the performance of the solutions offered by the metrology industry.

New systems of process control solutions are urgently needed. This paper offers a new paradigm of efficient process control solutions in fabs that would enable chip makers to achieve high yield and stable reliability in semiconductor devices.

Lab solutions to Fab in-line solutions

In-line metrologies traditionally used by fabs include film, optical critical dimension (OCD) metrology, overlay, Critical Dimension-Scanning Electron Microscope (CD-SEM), X-ray photoelectron spectroscopy (XPS), X-ray fluorescence (XRF)/X-ray diffraction (XRD), atomic force microscopy (AFM). However, these metrology tools are insufficient to provide all the physical parameters and material characterization required in complex 3D processes to identify the sub-nano scaled process variations of advanced devices. Labs, on the other hand, use significantly more metrology tools to characterize process changes, and are able to identify process drift and its cause by mapping physical and material parameters that in-line tools cannot serve. Metrologies widely used in labs include hard x-ray photoelectron spectroscopy (HAXPES), thermal desorption spectroscopy (TDS), self-focusing secondary-ion mass spectrometry (SIMS), angle resolved-X-ray photoelectron spectroscopy (AR-XPS), nano Raman spectroscopy, energy dispersive X-ray spectroscopy (EDX), critical dimensional-small angle X-ray spectroscopy (CD-SAXS), electron energy loss spectroscopy (EELS), scanning probe microscopy (SPM), atomic probe tomography (APT), Rutherford backscattering spectrometry (RBS), vibrating sample magnetometer (VSM), and auger electron microscopy (AES);

some research laboratories use CD-SAXS. The most popular reference metrologies in labs are transmission electron microscopy (TEM) and scanning electron microscope (SEM).

When processing wafers in fabs, in-line metrology should detect process drift and immediately shut down the problematic process equipment via SPC system based on in-line metrology data right after the process, in order to minimize e-test failures, or reliability failures. To do this, lab metrology tools can be converted and deployed by fab engineers to measure and analyze process variations currently going undetected by in-line metrologies, then immediately used to improve quality through process stabilization [6]. Successful deployment of lab solutions in fabs requires 300mm FOUP capability, fab automation, wafer & die alignment, communication with a host system, high throughput, data analytic process, SPC chart creation, small spot capability, tool to tool matching (TTTM), accuracy, precision, and long term stability. Additionally, both hardware and software must be optimized for the mass production environment to be efficiently utilized as fab in-line metrology. For example, lab Raman technology was recently introduced in fabs as in-line Raman; similarly, lab secondary-ion mass spectrometry (SIMS) technology was optimized and introduced in fabs as in-line SIMS. Both tools help fab engineers to obtain data right after the process and trigger immediate actions based on the data. As advanced devices scale down and increase in complexity, more lab metrology technologies should be transformed and adopted as fab in-line solutions [7,8]. This paradigm will enable new in-line metrologies to collect and analyze massive new data rapidly, thus helping to produce high-quality wafers by monitoring process parameters that have gone unmeasured by current in-line metrology solutions.

In-cell measurement

Fab engineers measure test structures made by mimicking the device cell structure in the scribe lines. But as devices shrink, it becomes increasingly challenging to correlate data on the test structures in the scribe lines with actual device performance; test structure on the pad is designed solely for metrology measurement, which has neither the same surrounding structures and materials, nor the same under structures, as the cell of the device. Therefore, the sensitivity of the test structures to process variation is neither as high nor as accurate as that of the cell pattern. This discrepancy drives fabs to move to in-cell measurement to better correlate metrology data from cell structures with e-test or yield variation. However, many metrology tools cannot directly measure the cell structures. To enable in-cell metrology, the spot size of metrology is important, and requirement of the spot size depends on device type such as logic, DRAM, and 3D NAND. In addition, some features need to be added to eliminate the influence of surrounding materials and structures. Nova Ltd. created vertically traveling scatterometry (VTS) to cut off the influence of underlayer structures at spectral interferometry (SI), resulting in accurate measurement of in-cell structures. Also, when measuring in-cell, the possibility of cell damage due to metrology cannot be overlooked. The device trend is already moving to 3D platform, so high aspect ratio (HAR) capability is also an area that needs further innovation.

Single solution to hybrid or combined solutions

New functions continue to be piled onto a single chip, forcing circuit designs to become increasingly complex and processes more sophisticated. No single metrology tool exists that can monitor process parameters with low SNR, and measure with high resolution, high throughput, high accuracy, and precisions needed by fab engineers for device mapping; this forced fabs to use a large variety of data gathering tools to detect subtle process changes that might significantly impact e-test parameters and yield performance. This triggered the advent of hybrid solutions [9], or combined solutions with multiple metrology technologies [10-13]. Combined solutions are needed when both contact CD data and material morphology data are required to clearly analyze the root cause of resistance variation of bitline contact in DRAM devices. Nova Ltd. provides Elipson (in-line Raman) and PRISM (OCD) for this application space as a combined solution. An example of a hybrid solution is a hybrid AFM which equips AFM and white light interferometry (WLI) in the same box [14]. Advanced 3D devices will need more and more layers which require hybrid metrology or combined metrologies.

AI solutions

In the search to extract meaningful insights from the big data generated by fabs that might predict process variables and map electrical performance, process and metrology industries have recently turned their attention towards solutions grounded in machine learning and deep learning [15-19]. For example, the HAR channel holes of 3D NAND processes require multiple physical parameters to understand the quality of etch process, because non-optimized etch process produces bowing, tilting, not open, hole ellipticity, non-targeted CDs, resulting in e-test failures or yield loss. To overcome the limitation of individual metrology tool induced by process complexity and scaled pitches, machine learning combined metrology solutions can help deliver critical data and insights to fab engineers to understand trend of process quality and make a decision to proceed with next production step. For this, Nova Ltd. provides NovaFit as a machine learning system for optical metrology. High demand for machine learning solutions will continue to drive the metrology industry to develop new machine learning algorithms and methodology to improve efficiency, accuracy, productivity, and time to solutions for high volume manufacturing.

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KEYWORDS

In-line metrology, In-cell metrology, Hybrid metrology, Combined metrology, Machine learning

Driving In-Fab High Aspect Ratio Memory Solutions with CD-SAXS

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INTRODUCTION

We have developed an industry-first, transmission, critical dimension small angle x-ray scattering (CD-SAXS) system for characterization of high aspect ratio memory layers. KLA's x-ray metrology system has been adopted by 3D NAND and DRAM memory manufacturers for inline measurement and control of critical device parameters during development and production. We describe here the motivation, development and capabilities of this technology for memory process control.

MOTIVATION

The continuous generation of information and the desire to archive more and more of it has created a significant increase in demand for memory capacity. The semiconductor industry has responded by developing 3D NAND technology, in which memory density is increased by adding more cells in a vertically oriented stack. DRAM manufacturers have struggled to scale recent nodes in part because the aspect ratio of storage capacitors continues to grow, impacting mechanical stability and shape control. As a result, high aspect ratio NAND and DRAM continue to present challenges for process control and metrology.

Until recently the best options for detailed shape characterization of high aspect ratio device structures have been destructive techniques, such as, FIB-SEM, XSEM, and XTEM. These methods can provide information for device characterization, but at the expense of yield and scrapped wafer costs. In addition, certain shape metrics critical for 3D NAND yield, like 3D NAND channel hole tilt and deck-to-deck overlay, are difficult to obtain using XSEM or XTEM. New x-ray dimensional measurement techniques like CD-SAXS have been under development, primarily due to laboratory efforts at NIST [1] [2]. CD-SAXS measurements have several advantages: (1) they scale well with decreasing pitch (2) the x-ray signal does not suffer from penetration depth issues (3) signal contamination from CMOS underlayers is less of a factor compared to optical tools, (4) the measured diffraction images are information-rich, containing a wealth of information on feature shape, and (5) they provide non-destructive shape measurement capability. We describe below our efforts to bring this technology to the fab in a production-worthy metrology system that helps 3D NAND and DRAM manufacturers find and monitor critical patterning parameters and processes.

DEVELOPMENT

Enabling CD-SAXS measurements in 3D NAND and DRAM fab environments requires extensive technical innovations and adaptations compared to the pioneering NIST prototype system (Figure 1). Previous implementations of CD-SAXS instruments outside of the semiconductor industry focused on research applications and lacked the automation and reliability required for 24/7 fab operations. We addressed these challenges to enable the first inline measurements by applying KLA's extensive experience with automation and design experience to x-ray systems. An efficient, intuitive user experience and seamless integration with fab automation and monitoring systems are provided by a newly developed user interface and control software. High reliability components and modular system designs coupled with a full suite of calibration, diagnostics and internal monitoring tools ensure tool availability and serviceability that meets stringent production fab requirements. Measurements leverage KLA's proprietary, industry-leading AcuShape® metrology modeling platform, and are supported by dedicated computational servers to ensure fast, real time measurement and data reporting.

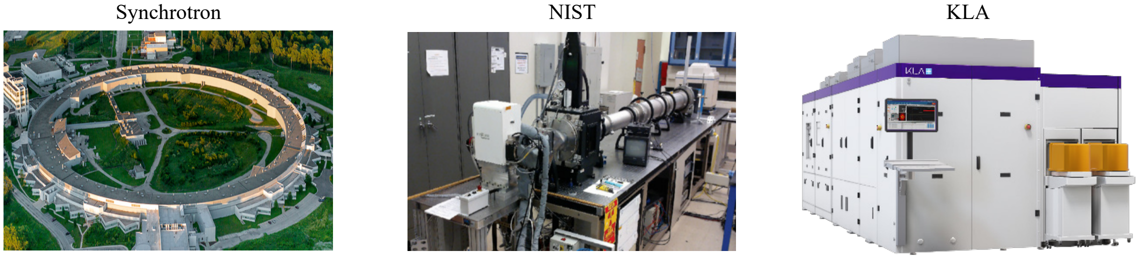

FIGURE 1. CD-SAXS metrology has evolved from synchrotron-based measurements [3] (left) to the pioneering NIST prototype system [4] (middle) to KLA's x-ray metrology system (right), which is a highly sensitive, production-capable metrology system for semiconductor manufacturers.

CAPABILITIES

Metrology Needs and Key Technology Strengths

Through extensive evaluations with our partners in the memory manufacturing industry, it has been proven that KLA's x-ray technology has strong capability for measuring high aspect ratio tilt, feature depth profile, ellipticity, and, in 3D NAND, deck-to-deck overlay. Feature tilt is a significant factor affecting overall device yield; a 3D NAND cell string or a DRAM container that has excessive tilt can cause an electrical short to an adjacent feature, as well as limit device pitch and memory density. In 3D NAND tilt measurement is important for control of cell string-to-cell string proximity and cell string-to-slit distance. The detection of non-zero tilt in the normal-incidence CD-SAXS diffraction image can often be done through visual inspection of the image brightness and symmetry. Depth profile of the tilt can be obtained by fitting a model to data collected over multiple angles of incidence. Critical dimension and ellipticity information can be obtained from the intensity pattern of diffraction orders in the diffraction images.

As an example of this, Figure 2 shows measured images [5] from a 3D NAND device after pillar etch and for different angles of incidence. The images show a strong sensitivity to pillar tilt, even at tilt levels < 1deg. Figure 2 also shows a tilt map collected across a 3D NAND wafer; such maps are very useful as a diagnosis of the pillar etch process and can be used in a feedback control method for optimizing etch processes. The tilt map shows a common pattern, in which the tilt on certain portions of the wafer points away from wafer center, while at other locations the tilt points towards wafer center. This kind of pattern can be indicative of conditions that existed in the plasma in the etcher when the wafer was being processed. Bending profile can also be measured accurately, which is preferred over destructive and costly measurements techniques like etch-back SEM.

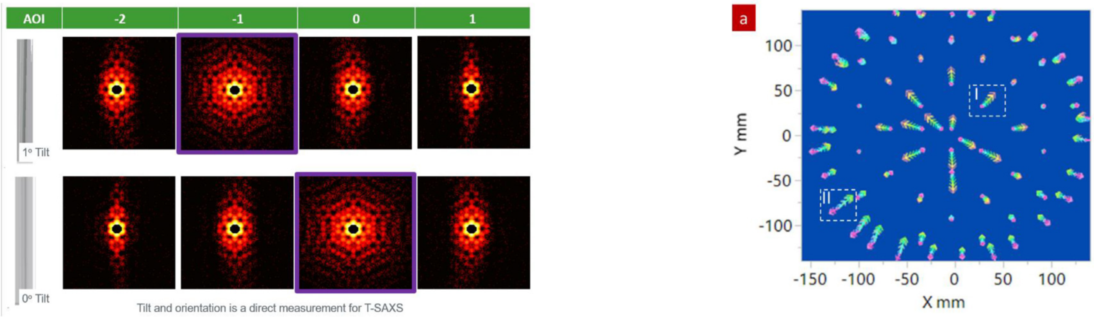

FIGURE 2. Production x-ray metrology data showing measured diffraction images from a 3D NAND device at different values of pillar tilt (left), and a tilt map collected across a wafer (right) [5].

In Figure 3 we showcase the ability of the x-ray metrology system to characterize CD depth profile. A CD difference between wafers in a design of experiment (DOE) set was easily detected. Critical dimension was reported at 13 locations along the depth, and the depth profile was consistent from wafer to wafer. The figure also shows the correlation of CD values to the memory manufacturer's reference metrology data. Excellent slope and R^2 values were obtained for all three wafers. Such high-resolution profile measurement is not practically achievable with other non-destructive techniques.

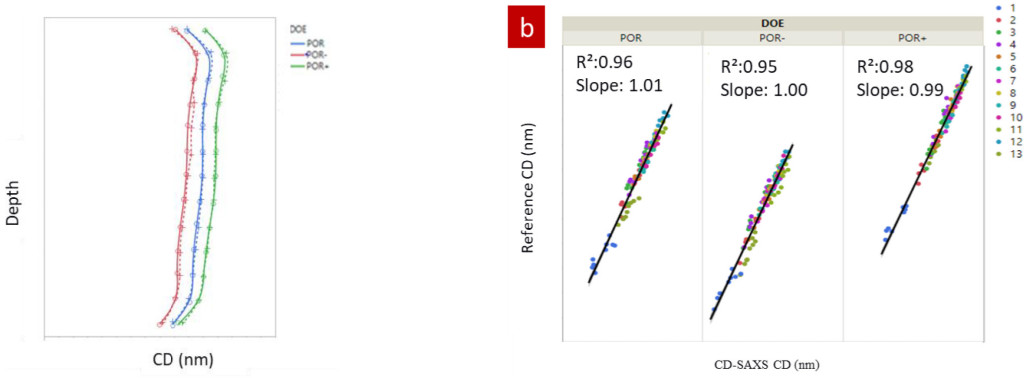

FIGURE 3. CD depth profiles measured by KLA's x-ray metrology system and correlation to reference data from a 3D NAND device [5].

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KEYWORDS

Metrology, CD-SAXS, x-ray, memory, 3D NAND, DRAM

Advanced Manufacturing using Virtual Metrology and Equipment Intelligence®

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The semiconductor industry is now confronting a number of metrology and manufacturing challenges due to critical technology requirements at next-node architectures. Advanced patterning techniques, such as EUV, frequency multiplication and selective deposition, are needed to meet cost and variability challenges at smaller line dimensions. Memory technologies, such as NAND, DRAM, and others, are requiring new materials and the transition to 3D topologies that are more challenging to manufacture. Advanced logic (such as GAA architectures) and heterogenous integration are being pursued in order to reduce power, footprint, and speed in next generation devices, but also require new, higher density and more complex manufacturing techniques. These technology requirements are creating additional metrology challenges, such as a need to measure smaller dimensions in complex 3D structures, increased measurement frequencies and additional demands for metrology data integration and analysis.

In this talk, we will discuss innovative concepts to address some of these next node metrology challenges. We will review the concepts of virtual fabrication and virtual metrology, and how they can be used in conjunction with conventional metrology to better support defect analysis and yield optimization at the latest technology nodes. We will also discuss how physical metrology can be used to calibrate a virtual process model, along with how a virtual process model can be used to validate physical metrology measurements made on a 3D NAND device.

In addition, our presentation will review the concept of Equipment Intelligence®, and how sensor-based metrology is being used to improve chamber and fleet variability. We will discuss how data from in-situ and standalone metrology, using machine learning/artificial intelligence, calibrated models, and advanced analytics, can drive real-time feed-forward and feedback optimization. We will show a specific example of next-generation metrology-based optimization, by presenting an advanced, in-situ etch-depth metrology system that uses spectral analysis and machine learning to deliver significant improvements in wafer-to-wafer etch depth control.

In our conclusion, we will summarize the challenges of next node architectures, and discuss how the concepts discussed in this presentation can be used by all participants in the semiconductor technology space to measure, characterize and address these upcoming challenges.

KEYWORDS

Next node metrology, virtual metrology, process modeling, sensor-based metrology, in-situ metrology, process modeling, machine learning, artificial intelligence, spectral analysis, mass metrology, hybrid metrology, integrated metrology, reflectometry, endpoint detection

mass metrology, hybrid metrology, integrated metrology, reflectometry, endpoint detection

Latest Developments in X-ray Metrology for Semiconductor Structures

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INTRODUCTION

The semiconductor industry continuously develops new materials, architectures and processes aiming to increase the performance of a wide variety of devices including silicon logic and memory devices for computing applications, compound semiconductors for opto- and power-electronics and many others including various sensor and actuator technologies. The advanced silicon devices use many three-dimensional (3D) architectures, which notably include Fin and Gate-All-Around-FET transistors for logic as well as 3D-NAND flash and DRAM memory. The new architectures are characterized by complex structures and, in some cases, high aspect ratios (HAR), which poses challenges on state-of-the-art inline metrology techniques. At the back-end of the line, leading manufacturers adopt more-than-Moore schemes to increase yields and functionality with complex hetero-integration technologies that increase the challenges in monitoring and controlling precise, fine-pitch bonding processes and 2.5D and 3D packaging schemes. X-ray techniques offer many unique advantages and capabilities to measure key parameters of advanced semiconductor devices and to inspect complex packaged structures in a non-destructive way. Thanks to advances in X-ray source and detector hardware, smart tool hardware and powerful analytics software, X-ray metrology and inspection techniques gained significantly in speed and are increasingly adopted for inline use in semiconductor manufacturing facilities.

X-RAY METROLOGY AND INSPECTION

A wide range of X-ray techniques is available to characterize chemical, physical and structural characteristics of a variety of materials, using diffraction, scattering and fluorescence of X-rays after interaction with the sampled matter. X-rays have been used to measure semiconductor structures for many years, especially in the R&D phase of new materials and processes. X-rays sample the material in a non-destructive way but are slower than optical techniques as the sample interactions are weaker and fewer source options available. However, recent developments in X-ray technology, in terms of hardware and software, have led to enhanced detected flux and analysis capabilities, enabling new applications and production worthy throughputs relevant for the trends that will shape semiconductor technology in the coming years [1].

Here we will highlight multiple X-ray techniques with applications in advanced logic and memory technologies, and advanced packaging. High Resolution X-ray Diffraction (HRXRD), alone or in combination with X-ray Reflectivity (XRR) is used to determine accurately and precisely the -individual- thickness and Ge concentration in engineered substrates consisting of multiple SiGe/Si layers critical for GAA-FETs including nano- and forksheet devices. Germanium can also be detected with micron X-ray Fluorescence (µXRF) with a high level of precision and with model-free quantification. This technique can be used to measure the average Ge recess in etched SiGe/Si GAA-structures. Tilt and shape of high aspect ratio (HAR) structures in 3D-NAND and DRAM devices are non-destructively measured with XCD®, also known as Small Angle X-ray Scattering for Critical Dimensions (CD-SAXS). Crystalline defects in high value SiC substrates can cause device failure both during the process and with subsequent usage of the device. Early detection with X-ray Diffraction Imaging (XRDI) can identify the root cause of such flaws and allow for corrections, to maintain yield and avoid waste. High resolution automated X-ray inspection (XRI) provides the ability to monitor processes in-line and enables fab-wide process control feedback for advanced packaging technologies and provides capabilities for inspection of the interior of packages not possible with automated optical inspection (AOI) tools.

High Resolution X-ray Diffraction for Nanosheet Metrology

Advanced logic makes use of Gate-All-Around transistors that consist of SiGe/Si pairs. The Ge concentration affects the etching rate in the formation of the recess, a critical step in the nanosheet process. It is therefore crucial to measure and control the individual layer thickness and Ge concentration per SiGe layer. HRXRD gives these parameters in a single measurement [2,3]. It is applied on the blanket engineered substrates using a millimeter sized X-ray spot. Optionally, the thickness analysis can be enhanced by additional XRR measurements. With a new high power rotating anode and large area detectors, this is done more than six times faster than with a traditional sealed tube. The novel setup with the significantly increased flux improves the measurement sensitivity compared to the state-of-the-art tool and reveals weak signals that went previously undetected, resulting in a better precision and better accuracy.

X-ray Fluorescence for SiGe Recess Metrology

µXRF is an established technique for inline measurement of thickness and composition of metal and alloy stacks both at the front and back-end of line. A new application on etched front-end of line (FEOL) structures has been explored and is presented here. A critical process step in the GAA process flow is the so-called cavity etch whereby the pattered SiGe/Si stacks are selectively etched to partially remove some of the SiGe and the depth of the etch is a key parameter that affects the device performance. Measuring the Ge concentration after is a way to monitor and control the average etch depth with high speed and precision and simple analysis [4]. We used µXRF with a polychromatic Mo excitation to measure the Ge-Kα signal of SiGe/Si etched forksheets. XRF samples the full stack; there are no absorption effects. We found a high correlation between the etch rate and Ge-Kα XRF signal. As absorption of Ge-Kα in Si and C is negligible in this thickness range, the measured signals only correlate with the SiGe volume and not the rest of the stack, such that this linear behavior is expected for stacks even with a hard mask or dummy gate on top. Furthermore, this linear correlation allows model-free quantitative analysis, provided that at least one reference standard is available (e.g. solid pad or forksheet prior to cavity etch). The typical µXRF beam has a FWHM of 25 µm and is therefore suitable to measure small test pads or directly on the device.

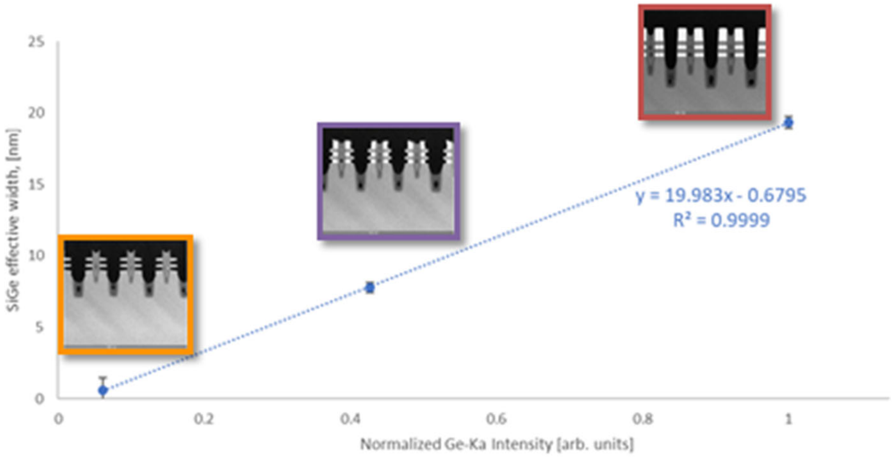

FIGURE 1. Nominal SiGe width vs. Ge Kα intensity. The measured Ge-Kα intensity shows a strong linear relationship to the SiGe fin widths after various rates of Ge-etching.

Profile and Tilt of HAR Structures with Small Angle X-ray Scattering

XCD is a scatterometry-based technique in which short wavelength ($\lambda < 0.1\ nm$) X-rays are scattered from a periodic array of nominally identical objects. Since X-rays interact with the core electrons, rather than valence electrons, XCD is much less sensitive to material properties than optical scattering where variations in the refractive index (n & k) can correlate strongly with the structural properties of interest in OCD.

Here we present an application that is used for the metrology of high aspect ratio holes critical in both 3D-NAND and DRAM technologies [5,6]. We demonstrate the capability of the technique by measuring the cross-section profile and tilt of the holes in a test wafer. A vertical XCD setup was used, which allows the wafer to remain in a horizontal position and reduces the tool footprint. The analysis was done with a novel software jointly developed with Onto Innovation. This software includes a 3D CAD-based region editor and parameter/constraint table for creating sophisticated structure models. Complex unit cells including all the layers and layouts with both the holes and spacers for trenches in 3D NAND can be modelled. The structure model includes a new and flexible approach for describing complex hole profiles. This new approach is easy-to-use, describes a range of realistic profiles and provides more stable regression with reduced parameter correlations than earlier approaches such as stacked cones. Tapering, bowing, ellipticity, tilting and twisting hole characteristics can all be modelled.

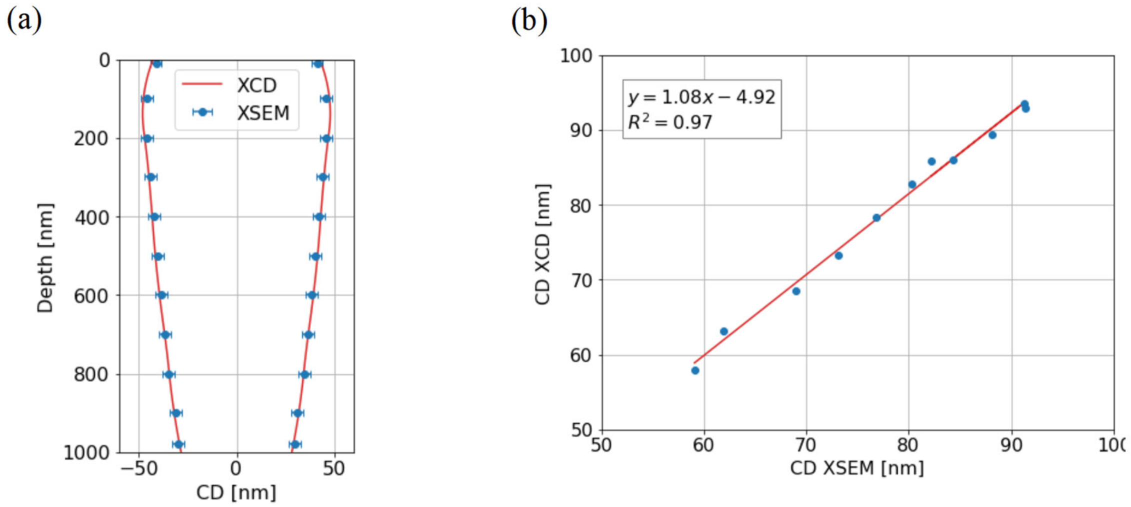

FIGURE 2. (a) Cross-section profile obtained by XCD (red line) compared to the profile obtained from the XSEM images (blue points) near the center of the wafer and (b) correlation plot between the CD values obtained by the two techniques.

High-Resolution, High Speed Crystalline Defect Characterization

XRDI is a technique to detect deviations in the crystal planes in single crystal samples using X-ray diffraction and can detect crystalline defects, cracks or damages in semiconductor wafers. It can be applied to full substrates of a variety of materials whether on pristine, processed or reclaimed Si, SiC or III-V wafers [2]. The XRDI defect map can be used to identify key defects or induced damage within multiple process steps, for example it can be used to help to predict which wafers may break and which should be scrapped to avoid larger damage further in the process, or to identify key defects within a process which can impact the device performance or long-term stability. Latest advances comprise the use of a high-power X-ray source and advanced algorithms enhance the automated detection, classification and quantification of defects.

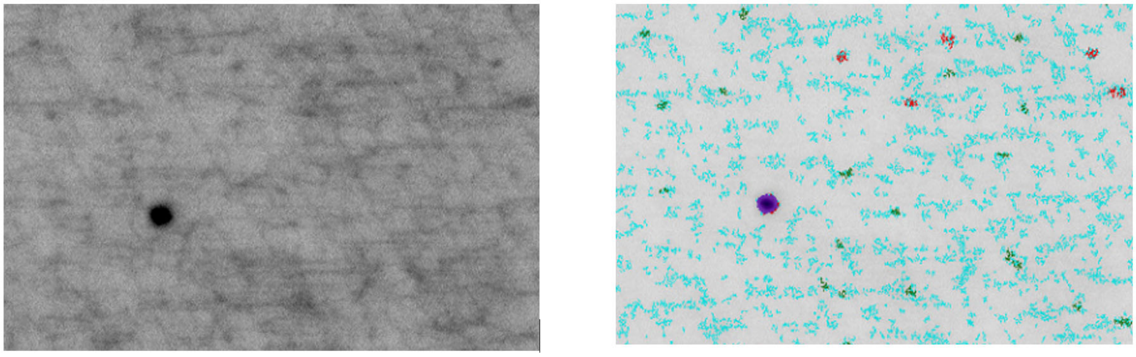

FIGURE 3. XRDI image (~11 mm x 7 mm) of a SiC substrate, with determination of threading edge dislocations (TED, green), threading screw dislocations (TSD, red) and basal plane dislocations (BPD, turquoise) densities.

High-speed Inspection for Advanced Packaging

Automated, high-speed X-ray imaging (XRI) provides manufacturers the ability for in-line inspection of chips, advanced packages [7] and wafers without a significant impact to high-volume throughput. The unique approach of the XRI system presented here achieves its simultaneous high resolution and large field of view by placing the sample close to a high-resolution, high NA detector [8]. Unlike traditional 3D-CT X-ray systems, this geometry removes the limitation on source spot size which enables the use of a high-powered source of ~1 kW for high-speed imaging while maintaining a high resolution. A high bit-depth sensor in the XRI detector provides data rich images for machine interpretation. Besides hardware imaging, XRI also utilizes advanced algorithms to quickly and reliably analyze images containing tens of thousands of solder joints to summarize relevant features, identify outliers, and classify defects.

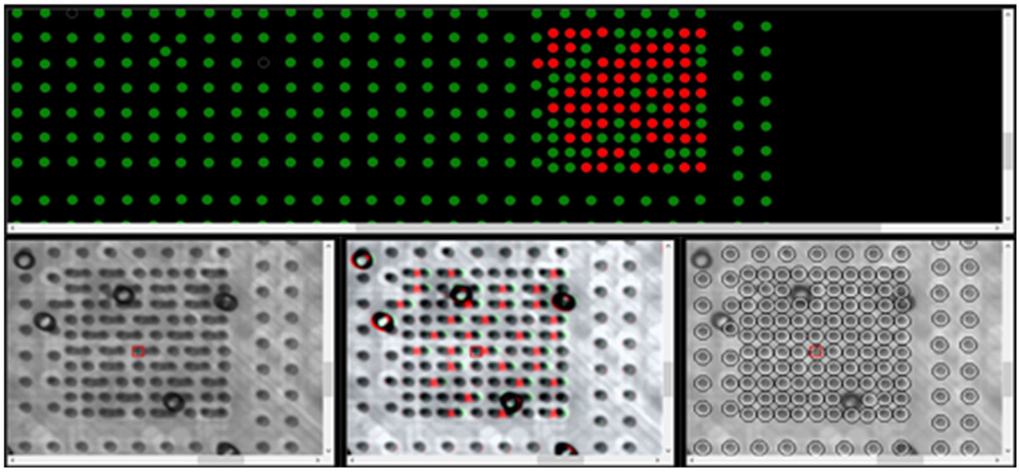

FIGURE 4. Successful deployment of automatic bridge detection in high-volume manufacturing. Data visualization highlights defective areas for review. (top) Threshold image with red indicating failed bumps, (left) raw image, (middle) colorized image indicating the defects, (right) map of circled features of interest.

CONCLUSION

Using a variety of X-ray techniques, it is possible to characterize physical, chemical and structural parameters of complex semiconductor stacks in a non-destructive way. X-ray metrology for the front-end and X-ray inspection for the back-end of the semiconductor process gained significantly in speed over the past years, thanks to the implementation of high-power X-ray sources and novel setups and smart analysis.

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KEYWORDS

X-ray Metrology, X-ray Inspection, 3D Structures, Advanced Logic, GAAFET, 3D-NAND, DRAM

The Reverse-Tip-Sample SPM approach: A Paradigm Shift in Data Collection

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INTRODUCTION

Scanning probe microscopy (SPM) techniques have become a workhorse for semiconductor device characterization because they can measure a wide variety of properties with nanometer spatial resolution such as dimensions (topography/roughness), electric and magnetic fields, voltages, currents, capacitance, and temperature. The key SPM component is a small nanometric sharp tip which is subjected to wear during scanning and must therefore be regularly changed which is a major drawback of all SPM methods. In-line SPM tools deal with this issue by using an automated motorized approach whereby a worn-out tip module is exchanged with a new one from a tip-module cassette. Nonetheless, the single-tip limitation and the need for regular tip replacements still represents a fundamental limitation and major obstacle for SPM for addressing important characterization in nanoelectronics technology. Alternative concepts such as cantilever-tip arrays, switchable scan heads, tips and probes have been proposed but the ‘single-tip’ barrier has not been overcome in practice yet. Therefore, we have developed an SPM concept called reverse-tip-sample (RTS) SPM which can switch tips seamlessly while remaining scanning at the region of interest. This presentation describes the concept, discusses new scan possibilities, and shows first application examples.

RTS SPM CONCEPT

In RTS SPM (Fig. 1a), the sample is fixed to the cantilever end (where the tip is located in conventional SPM) and scans over a tip fixed to a tip substrate (where the sample is located in common SPM). Due to this reverse positioning of tip vs. sample, this approach is referred to as reverse-tip-sample (RTS) SPM. Its most obvious advantage is that it allows to position a high number of sharp tips in close proximity to each other on a tip substrate as shown in Fig. 1b (in practice an area of 1 mm^2 can contain more than 1000 tips). When a worn-out tip needs to be changed, the sample is simply positioned over a new tip without an interruption of the ongoing experiment. Tip replacement is a matter of seconds as compared to typically ~10 min for ambient and ~1 hour for vacuum SPM. The typical sample size of ~10x10x2 μm^3 in this approach is a good match with the requirements for nanoelectronics device analysis and adequate sample preparation procedures based on focused ion beam (FIB) (Fig. 1c) are directly applicable (even fully automated ones from in-line transmission electron microscopy (TEM) workflows look feasible). As the number of tips in RTS SPM is nearly unlimited from the point of view of an SPM user, it opens new analysis opportunities where the impact of high tip wear on the analysis result is overcome by changing the tip more often (e.g. after each scan). This is especially attractive for SPM modes which need high forces as for example in scanning spreading resistance microscopy (SSRM) and 3D nanotomography. Furthermore, new modes become feasible such as multiple-tip scanning where a device is scanned by several tips in the same scan line which improves the measurement statistics and helps to overcome typical SPM artifacts. It is also possible to scan multiple samples at once with the same tip or with several tips at quasi the same time. The RTS SPM approach offers also the possibility to apply different SPM techniques at the same time by connecting different tips to different types of application modules/amplifiers (e.g. SSRM and scanning capacitance microscopy). Nanoelectronics analysis would strongly benefit from these advanced application possibilities because of its ultimate resolution needs and its quest for precise quantitative measurements.

APPLICATION EXAMPLES

Fig. 1d illustrates the effect of rapid tip switching in RTS SPM on the example of a boron doping staircase structure which was FIB lifted-out from the substrate and fixed to the end of a metal cantilever beam. This sample was scanned in SSRM mode using inhouse fabricated doped diamond pyramidal tips which were arranged in close distance to each other. Six SSRM images were consecutively scanned in contact mode using 6 different tips whereby performing an instant tip switching after each SSRM image was recorded. In this way, a sample can be electrically probed by several/many tips in RTS SPM which can highly benefit the data quality (e.g. preselection of super sharp tips for ultra-high resolution) and image interpretation (e.g. higher statistical data relevancy, imaging artifacts as often occurring in electrical SPM are better recognized). Better quantitative measurements are achieved by allowing calibration and device sample to be positioned in close (micrometer) proximity to each other on the metal cantilever and by scanning the tip in each scan line across both calibration and device structure. Note that the conventional method needs separate calibration and device sample engage/disengage steps which significantly contributes to quantification errors. This principle can further be extended by positioning several device samples on the cantilever next to each other and to scan them with the same tip in each scan line which improves the data quality (in practice when aiming for ≤1-nm resolution basically every electrical diamond tip is slightly unique in terms of spatial resolution and electrical conductivity). In still another RTS SPM implementation the same sample can be scanned in each scan line with several tips which significantly improves the measurement data interpretation (Fig. 1e).

CONCLUSIONS

RTS SPM overcomes the single-tip barrier of conventional SPM and looks especially promising for nanoelectronics device characterization because of improved statistical data, a faster way to data (no time consuming physical tip exchanges anymore), and the possibility to perform completely new types of measurements like multiple-tip and/or multiple-technique measurements.

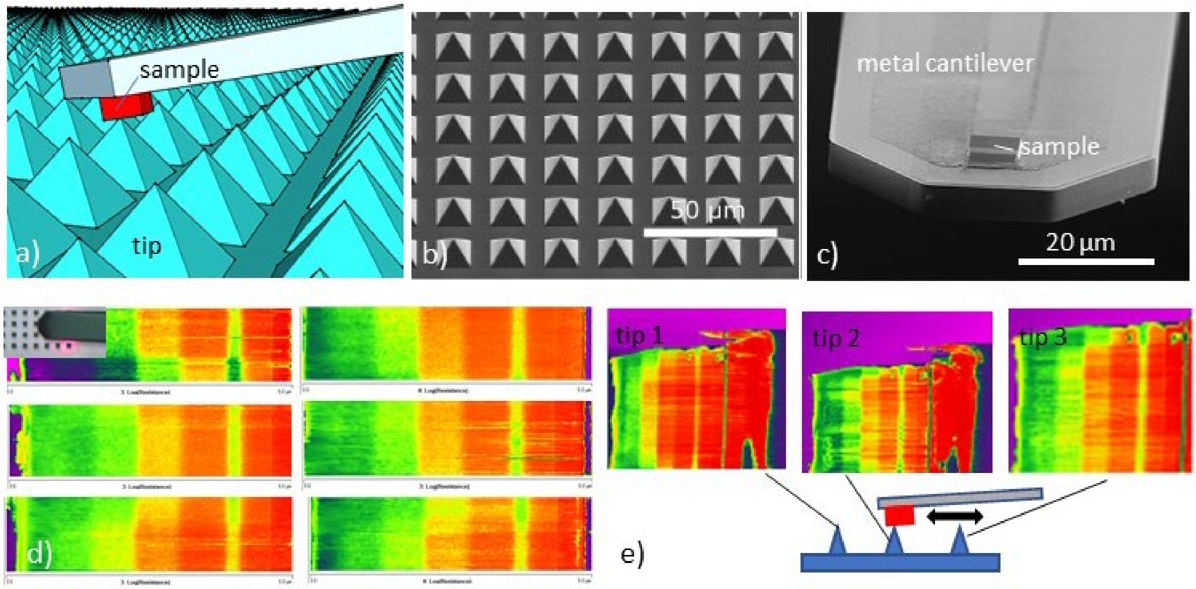

Figure 1: a) Schematic representation of the RTS SPM concept; b) prototype of diamond tip array for RTS SPM application; c) Si sample fixed to metal cantilever by FIB and ready for RTS SPM analysis; d) cantilever with fixed 5 microns wide Si doping staircase structure which is scanned in SSRM mode by a doped diamond tip and whereby the tip is instantly switched six-times after each image (zoom-in); e) Example for sample analysis in RTS SSRM whereby 3 different diamond tips scan the doping staircase structure in each scan line.

Acknowledgements: We acknowledge the contribution of A. Kanniainen, L. Wouters, P. Lagrain, C. Drijbooms, N. Bosman, H. Bender, S. Folkersma, K. Paredis, and W. Vandervorst.

KEYWORDS: Scanning probe microscopy, SPM, RTS SPM, tip.

Time-Resolved Transmission Electron Microscopy From 1 Hz To 10 GHz In Stroboscopic Mode

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In the previous two decades, important technological advancements have expanded the range of temporal resolution in transmission electron microscopes (TEM). Commercial direct-counting and single-electron detectors have revealed dynamics in the ms-timescale. Laser-actuated photoemission microscopes [1, 2] combined with beam scanning, spatially-parsed large area detectors [3], and sparse-sensing algorithms [4], can now unlock phenomena at the μs to sub-ps timescales. Further optimization of the photoemission stage [5] and beam bunching technologies could potentially extend the temporal resolution into the deep fs-regime.

Following our earlier concept paper [6], we now present the modifications to a pair of commercial instruments – one Schottky (200 keV) [7] and one thermionic (300 keV) [8] that can confer temporal information spanning the ns and ps range with repetition rates from 1 Hz to 10 GHz, in the stroboscopic mode without an excitation laser, thereby preserving the native beam brightness of the thermionic filament or field emitter tip. The key enabling technology is a pair of broadband phase-matched modulating and demodulating RF pulsers. We have demonstrated 11 ps and 30 ps on the 200 keV and 300 keV microscopes respectively. The placement of the pulsers, mounted immediately below the gun, allows for the preservation of all optical configurations otherwise available to the unmodified instrument, and therefore makes these instruments dual-mode, both stroboscopic time-resolved (strobe) mode and conventional continuous waveform (CW) mode.

Original imaging and diffraction functionalities are preserved post-modification. We will demonstrate the time-resolved capabilities via images of RF waves moving through an interdigitated MEMS device, and how these observations can now be made coupled with other techniques such as off-axis electron holography or STEM/EELS. Finally, we will discuss the applicability for such this type of modified pulsed-beam system for nanoelectronics through our ongoing work in ferroelectric systems.

FIGURE 1. Modified 300 keV TEM at NIST. The modified section, including the beam pulser is within the blue circle.

FIGURE 2. From ref [9]. High-resolution imaging of gold nanoparticles using continuous and pulsed electron beams. (a, d) Bright field images of gold nanoparticles using continuous (a) and pulsed (d) electron beams without an objective aperture. Images were acquired with a 3 GHz sweeping frequency and pulse duration of 60 ps. (b, e) Magnified images from the regions-of-interest in (a) and (d). Pulsed beam images were acquired longer to achieve similar total doses to ensure that fringe visibility was not affected by signal reduction. (c) Intensity line profiles taken from (b) and (e) along the respective ROIs. (f) Quantitative comparison of the contrast, lattice spacing and accumulated dose using the continuous (maroon) and pulsed (blue) electron

beams measured from the line profiles in (c). Error bars is the standard error of values extracted from the line profiles in (c).

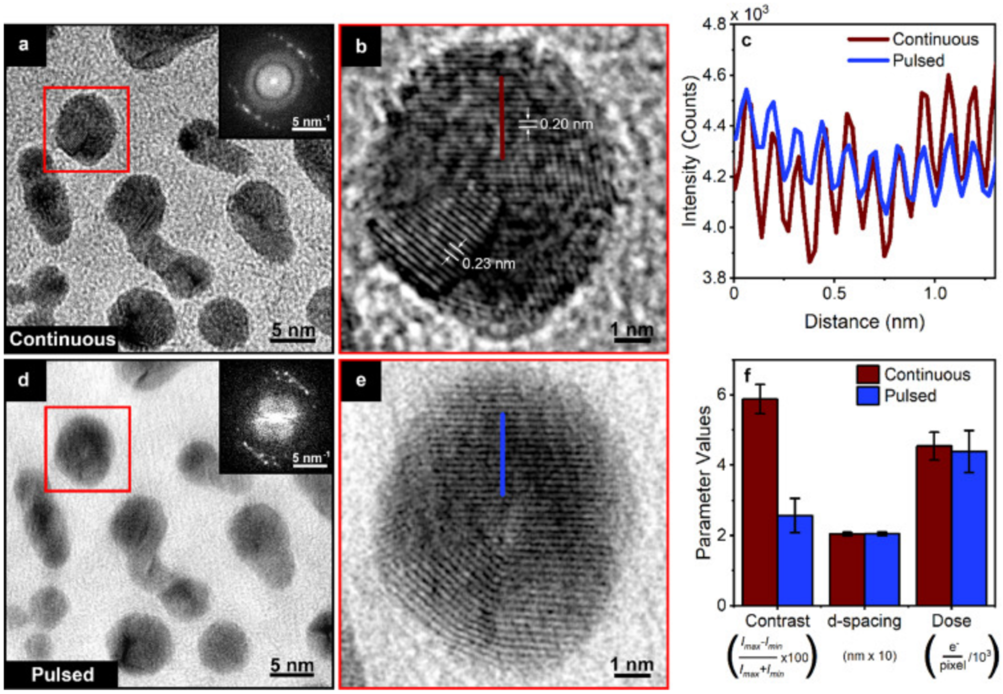
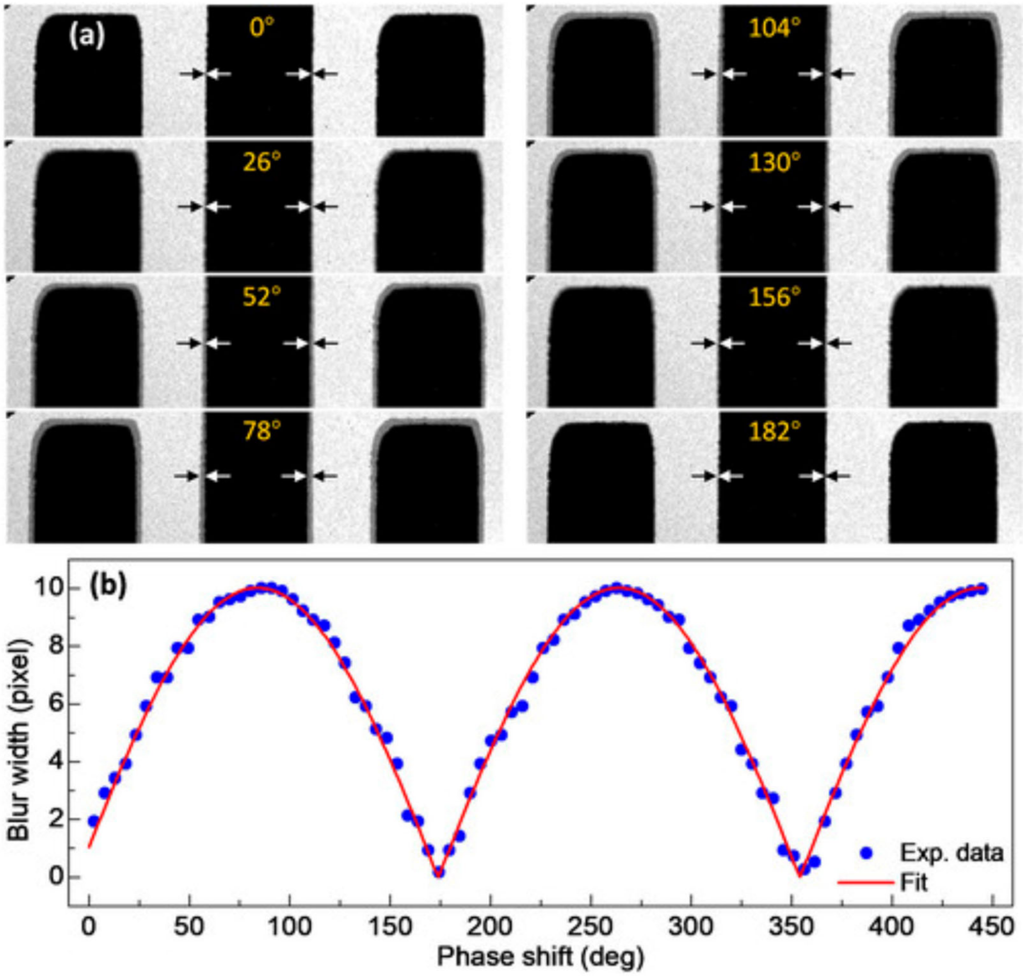


FIGURE 3. From Ref [8]. Stroboscopic pump–probe imaging experimental results. (a) Stroboscopic pump–probe image series of a comb tine with f_0 = 2.6 GHz at various values of phase shift, $\Delta\phi$. Small black and white arrows indicate the blur width. (b) The blur width (W) variation as a function of $\Delta\phi$. The blue dots are experimental data, and the red curve is the fitted result.



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KEYWORDS

Time-resolved; GHz, stroboscopic imaging, TEM, device characterization

New Developments in Atom Probe Tomography

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INTRODUCTION

While the atom probe tomography (APT) technique has been around for more than 50 years, only recently has there been substantial success in its application in the semiconductor industry (for some recent reviews see[1–3]). This continued application targeting tomographic compositional analysis of nanometer scale state-of-the-art device structures relies on continued advances in the areas of hardware (and software) related to APT. The field-of-view (FOV) / mass-spectral-quality tradeoff [4] along with laser wavelength[5,6] (both resulting in improved atom probe performance) are two such areas of advancement.

Historically it has been highly desirable for an atom probe to have a combination of a wide field of view and high mass resolving power (MRP). However, these two metrics are inherently at odds with each other, from a design perspective, due to higher flight time variations (for different flight paths) across the FOV for large APT detectors. Some efforts to overcome this difficulty employ reflectron energy compensating based solutions[7], while others use a straight flight path design[8,9]. In the current work, we present the two new atom probes which comprise CAMECA's 6000 product line and briefly introduce the benefits of each on a variety of materials.

THE CAMECA INVIZO 6000

The goal of the Invizo 6000™ design is to provide substantially increased data volumes while improving data quality and specimen yield. The Invizo 6000 uses a patented design[9] based on Einzel lenses and laser beam delivery optics which enable dual sided specimen illumination with a deep UV (257.5 nm) wavelength (spot size of <2 µm.) The results of these technological advancements include: 1) an ultra-wide FOV (in some cases capturing the entire specimen volume) while maintaining high MRP, 2) more uniform heat diffusion resulting in more uniform field evaporation, and 3) more uniform heat deposition and reduced evaporation field (stress) differences between different phases which produce more uniform specimen shapes. The benefits of the Invizo 6000 include simplified specimen preparation with a higher chance to capture the region of the interest (due to the wide FOV), Improved concentration statistics (due to the wide FOV yielding larger datasets), improved yield for some materials systems (due to the wide FOV and DUV), improved MRP uniformity (due to dual beam illumination), and more accurate data reconstruction (due to dual beam illumination and DUV).

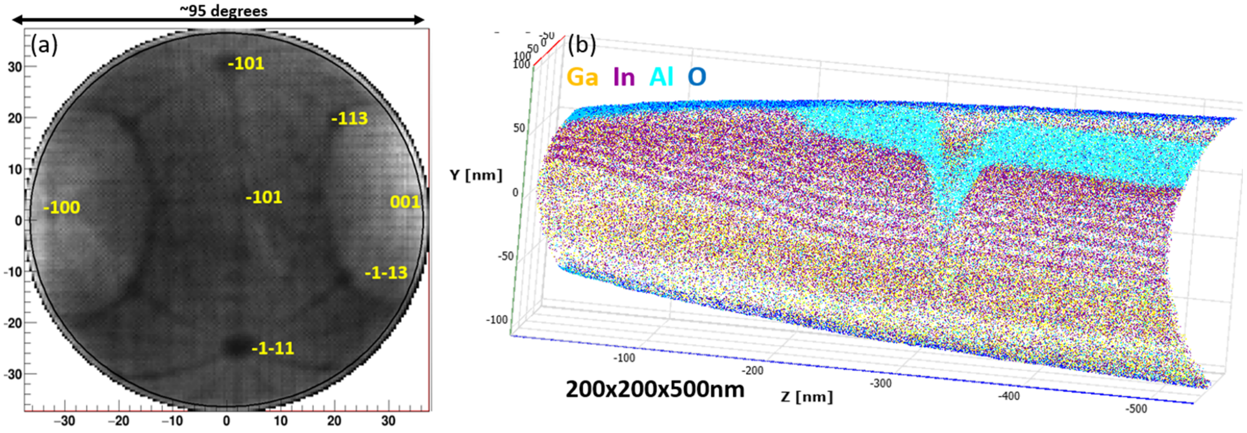

FIGURE 1. (a) Invizo 6000 field desorption map of an aluminum specimen with an angular field of view >90º (units are detector dimensions in mm) and (b) full field of view of a V-defect in a GaN-based quantum well structure.

The wide FOV of the Invizo 6000 is illustrated in Figure 1a, which shows a field desorption map of an aluminum specimen with a FOV >90º (typical LEAP 5000 FOV ~60º). In addition to just providing more data and the associated benefits, this type of field of view enables the ability to caption larger features in their entirety, as illustrated in Figure 1b, which shows a V-defect in a GaN-based quantum well structure. Due to the presence of significant oxygen atoms detected near the edges of the specimen (in XY), it appears that the entire specimen volume is being collected.

While exposure to a single focused-laser-beam is known to lead to non-hemispherical (asymmetrical) shape (especially when very high laser energy is utilized), the Invizo 6000 irradiates the specimen from two sides in a thermally coincident manner[4]. A comparison of a representative silicon specimen shape from one-beam and two-beam laser conditions is shown in Figure 2ab. The local curvature (tip radius) at different points along the tip surface for each of the specimens are quantified in Fig. 2c. showing a decrease of ~5X in the standard deviation as a percentage of the mean tip radius.

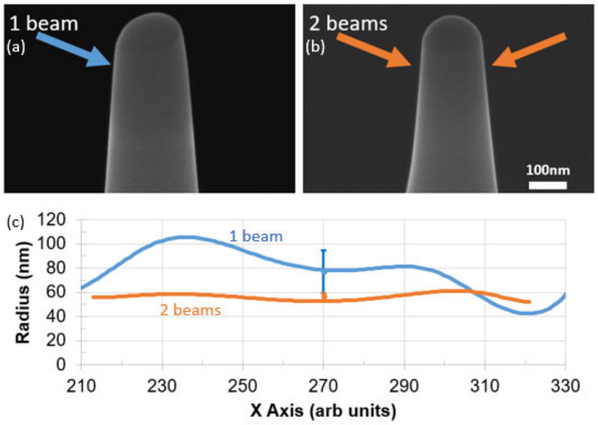

FIGURE 2. Invizo 6000 representative specimen shapes for (a) one-beam and (b) two-beam laser conditions. In (c) the single point average radii are (77±18) nm and (56±2.6) nm for the one- and two-beam conditions, respectively.

THE CAMECA LEAP 6000 XR

The goal of the LEAP 6000™ design builds on the effectiveness of the local electrode compatible LEAP platform in research and near-FAB applications by improving the throughput and ease-of-use through fully automated laser-specimen-electrode alignment. In addition, a goal is to improve detection sensitivity, yield, and data quality. The LEAP 6000 uses a redesigned optical system with the same DUV laser as the Invizo 6000 and includes a multi-mode pulsing operation with simultaneous voltage plus laser pulsing. The results of these technology advancements include: 1) increased automation with complete laser-specimen-electrode alignments and no manual operation required after inserting the specimen and local electrode, 2) more uniform heat deposition and reduced evaporation field (stress) differences between different phases which produce more uniform specimen shapes, and 3) improved signal to noise in the mass spectra. The benefits of the LEAP 6000 include reduced training requirements (due to enhanced ease of use), improved yield for some materials systems (due to DUV), more accurate data reconstruction (due to DUV), and higher sensitivity (due to decreased background noise).

An example of how the DUV leads to improved yield (for both the Invizo and LEAP 6000) is shown for the Si-SiO system in Figure 3. The specimen consists of a 12-nm silicon oxide layer between regions of silicon[10]. Figure 3 shows the effective evaporation field (relative to silicon) for the UV (LEAP 5000) and DUV (LEAP 6000) cases as the specimen is field evaporated. These data are calculated directly from the specimen voltage. As the stress on the specimen is proportional to the square of the electric field[11], a specimen containing Si/SiO illuminated with a DUV laser is under less stress and thus provides a higher probability to yield successful data. Sufficient observations have been made to make this observation statistically significant for the silicon / silicon oxide system.

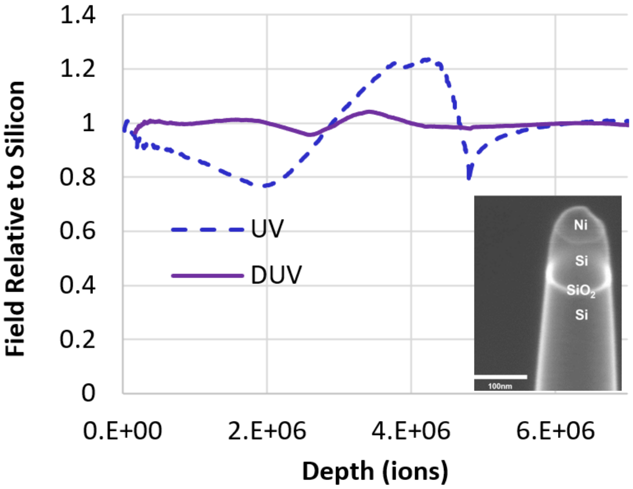

FIGURE 3. The effective evaporation field (relative to silicon) for the UV and DUV cases when field evaporating through a silicon / silicon oxide / silicon structure.[6] The DUV laser provides improved yield in this system by reducing the effective stress on the specimen.

The mass spectral background noise reduction through a combined voltage plus laser pulsing mode[12] is presented in Figure 4. For silicon, a background reduction of ~15x is illustrated in Figure 4. This effect has been shown for a variety of materials, (with varying level of reduction) including silicon, silicon dioxide, aluminum, and a stainless steel (as shown in Figure 4b) and, for the preliminary data, generally improves with voltage pulse magnitude.

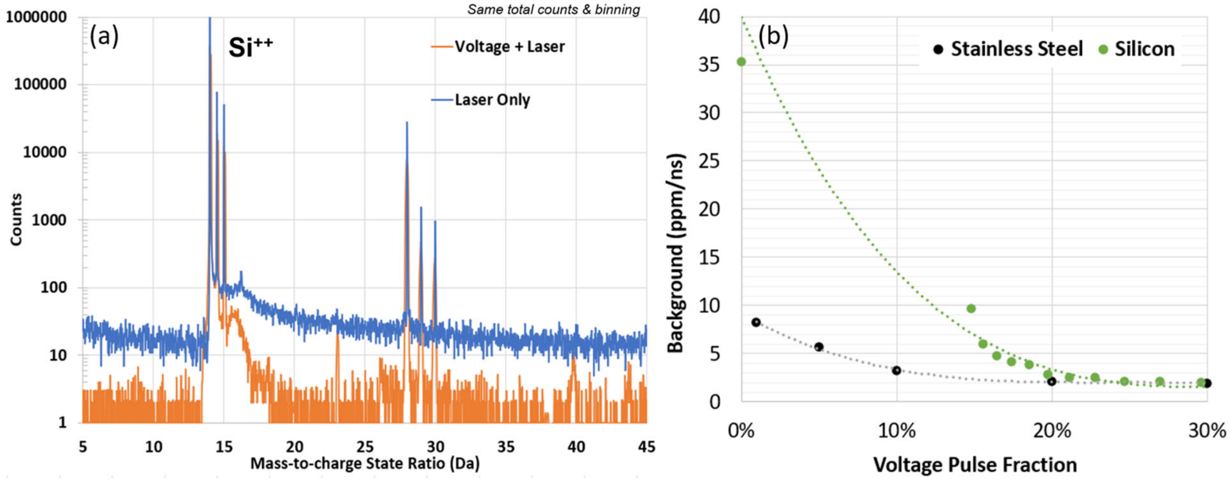

FIGURE 4. (a) Mass spectral background noise reduction through a combined voltage plus laser pulsing mode for silicon and (b) noise reduction as a function of voltage pulse fraction for silicon and a stainless steel.

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KEYWORDS

Atom probe tomography, wide field of view, deep UV laser, background noise, mass spectral quality

Recent Advances in Electron Tomography and Applications in the Semiconductor Industry

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INTRODUCTION

As device architectures become increasingly complex and heterogeneous, advanced three-dimensional (3D) characterization tools are needed to elucidate structure-property relationships and optimize process conditions. At the nanoscale, high-angle annular dark-field scanning transmission electron microscope (STEM-HAADF) tomography is widely used for 3D morphological analysis of semiconductor devices [1]. This technique consists in acquiring a series of 2D STEM-HAADF projections at different viewing angles, and applying a dedicated algorithm to retrieve the 3D morphology of the object.

3D chemical imaging of nanodevices is nowadays possible by energy-dispersive x-ray spectroscopy STEM (STEM-EDX) tomography, which has benefited greatly from recent developments in electron sources such as the 'X'-FEG (Field Emission Gun), and multiple X-ray detector systems such as the Super-X, incorporating four SSD (Silicon Drift Detectors) detectors [2]. The technique remains however very time-consuming, and limitations in X-ray count rates and number or projections are necessary to minimize the total acquisition time and avoid beam damage during the experiment. In addition, tomographic series of STEM-EDX datacubes are too large to be analyzed by commercial software packages in an optimal way. In order to make STEM-EDX tomography accessible to the semiconductor industry, it is necessary to automate the data processing and employ sophisticated methods capable of producing high quality reconstructions from a limited number of noisy projections.

In this presentation, we will give an overview of the recent advances in electron tomography, with an emphasis on STEM-EDX tomography and the processing tools necessary for accessing reliable 3D information. We will show that multivariate statistical analysis methods [3] can be used for unsupervised identification of chemical phases, while automated elemental analysis of very noisy EDX-STEM datasets can be achieved by principal component analysis (PCA) followed by Gaussian curve-fitting methods.

We will also illustrate the superior performance of compressed sensing (CS) approaches [4,5] compared to classical tomographic algorithms, for 3D reconstructions from highly under-sampled datasets.

As an example, we show below the 3D chemical analysis of an arsenic-doped silicon structure for fin field-effect transistor (FinFET) technology [6]. Other applications of electron tomography for the 3D analysis of semiconductor devices and materials will be presented, ranging from phase-change materials [5] to DNA origami nanostructures for silicon patterning. Prospects of deep learning approaches for spectral analysis and tomographic reconstruction will be also discussed.

3D CHEMICAL ANALYSIS OF AN ARSENIC-DOPED SILICON STRUCTURE

The investigated sample is a Si fin-shaped structure doped with As as an n-type dopant. The structures were fabricated on a 300 mm Si-on-insulator substrate with top Si and buried oxide thicknesses of 14 nm and 25 nm. A Si epitaxy process was then performed to obtain the targeted total Si layer of 60 nm. This top-Si layer was patterned using e-beam lithography and dry etching to obtain fin-like structures with 45 nm width. Samples were then doped by plasma immersion ion implantation using AsH3 gas as As precursor and encapsulated in SiOx. A needle-shaped sample was prepared by focused ion beam, and inserted in a Thermo Fisher Scientific Titan Themis operating at 200 kV and equipped with a probe corrector and a Super-X EDX system. 21 STEM-EDX projections were acquired between -90° and +90°, mainly every 10°.

Hyperspy [7], a Python-based software for hyperspectral data processing, was used to batch-process the STEM-EDX tomographic dataset. Non-negative matrix factorization (NMF) was applied to decompose the dataset into spectral signatures and loading maps, both of which are constrained to be non-negative. The number of components to use for the factorization was determined following the scree-plot inflexion point of the principal component analysis (PCA), leading to the identification of three chemical phases in the sample: Si, SiOx and As (Figure 1).

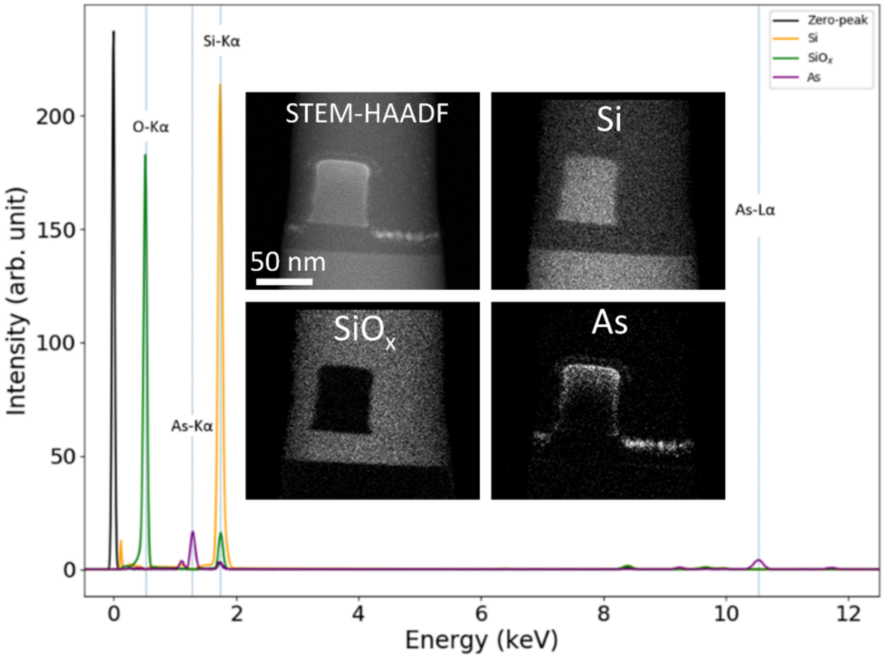

FIGURE 1. Spectral components (Si, SiO_x and As) obtained from NMF decomposition of the STEM-EDX dataset composed of 21 datacubes. The insets correspond to the STEM-HAADF projection and Si, SiO_x and As maps at 5° tilt angle. Adapted from [6].

The tomographic reconstructions were performed using Pysap-etomo [5,8], an in-house Python library dedicated to CS approaches for electron tomography. In the present example, total variation minimization (TV) [4] was employed to reduce the artefacts due to the limited number of projections and the noisy signal. Figure 2(a) shows the volume rendering of the tomographic reconstructions of Si (orange), SiO_x (green) and As (purple) chemical phases. Figure 2(b)–(d) are xz slices through the reconstruction of Si, SiO_x and As volumes. A line profile through the central xz slice (arrow in figure 2(e)) indicates implantation of ~20 nm inside the Si structure.

Note that TV promotes piecewise constant structures even when there is a gradual change in intensities. As a result, stair-case and patchy artefacts may appear in the non-piecewise constant regions. We will show that these artefacts can be reduced using higher-order derivative methods or wavelet-based CS algorithms implemented in Pysap-etomo [5,8].

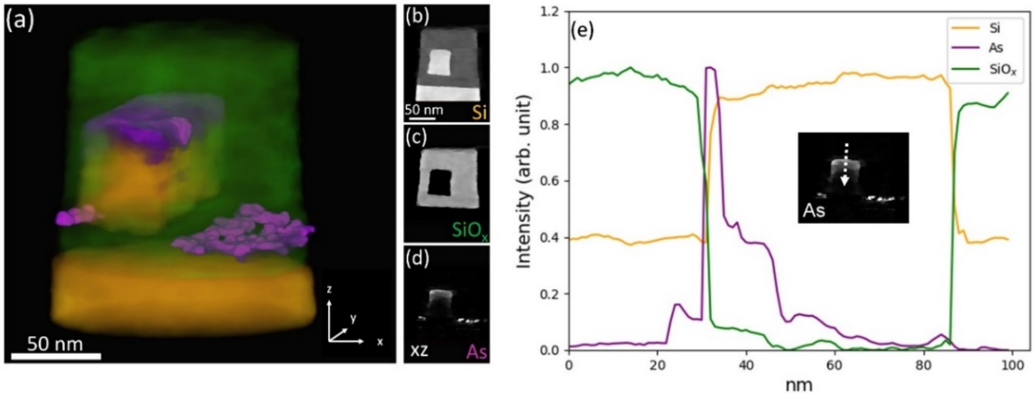

FIGURE 2. (a) Volume rendering of the tomographic reconstructions of Si (orange), SiO_x (green) and As (purple) chemical phases; (b)–(d) *xz* slices through the reconstruction of Si, SiO_x and As volumes; (e) a depth profile through the fin-shaped structure on a selected section (dotted arrow in the insert), after normalization of the three volumes. Adapted from [6].

The tools presented are also applicable to other spectroscopic modes such as electron energy loss spectroscopy STEM (STEM-EELS) [5] or simultaneous STEM-EELS/EDX, and recent studies have shown that correlative approaches combining analytical electron tomography with other techniques (e.g. STEM-HAADF tomography or atom probe tomography (APT) [9]) have the potential to provide a more complete knowledge about the nanostructures [10].

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KEYWORDS

3D analysis, electron tomography, morphology, chemical composition, compressed sensing, machine learning.

High Volume 3D SEM Metrology on Advanced Memory

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INTRODUCTION

Channel/Memory hole etch and cell film deposition processes are critical to 3D NAND manufacturing. Fabs struggle with understanding the behavior and performance of these tall, high aspect ratio (HAR) structures. HAR etch is plagued with issues like bowing, twist, and tilt[1]. These issues can result in columns touching and corresponding bit failure. Memory cell deposition is challenging to measure as the individual cells are covered by many layers of material. Fabs lack the ability to resolve these characteristics easily as the critical dimensions (CDs) are buried within many layers of opaque or semi-opaque materials.

Conventional in-line metrology solutions, especially optical and e-beam systems, are deficient in their penetration and signal extraction capabilities to accurately analyze 3D NAND structures[2]. The inability to directly analyze these characteristics slows down 3D NAND product ramps and can force the relaxing of design rules to accommodate larger process variation. These effects are undesirable as they add additional cost and reduce profitability.

Some efforts have been made to bridge these gaps recently including large investments in Artificial Intelligence (AI) based analytical solutions as well as Small Angle X-ray Scattering (SAXS)[3]. AI or Machine Learning (ML) based solutions help extract all possible learning from extracted data[4,5], but cannot create information from nothing. If in-stack data is unavailable, these solutions can't provide the answers. CD-SAXS has the potential to provide critical in-stack CD's, but suffers from a number of limitations including Z resolution and local channel-hole-to-channel-hole variation[6].

Xenon plasma FIB delayering solves this problem by iteratively removing layer material while acquiring metrology images. This, when combined with novel alignment and processing solutions, provides a full set of CD measurements for the entire stack. These CD's accurately reflect the complex internal structure of the 3D NAND device. Having access to this data provides the missing insights needed to improve process performance.

In this work we demonstrate a Xenon plasma FIB delayering process with correlated SEM metrology for acquiring complete channel/memory hole etch characteristics, as well as memory cell deposition characteristics. The proposed technique provides object-level discretization of the volumetric data. Application of machine learning techniques such as super resolution reconstruction, sharpness restoration, etc., makes it possible to calculate multiple shape and size features in several spatial orientations with high precision and accuracy.

The possibility of high-throughput and high-content information extraction in the proposed method optimally defines the 3D-NAND CDs variation in the 3D-space. This solution also provides nearest-neighbor and hole center in global coordinates to identify difficult issues such as twist and tilt. This methodology provides clear and complete understanding of in-stack parameters to inform process trend and distribution analyses. By minimizing these issues, 3D NAND manufacturers can accelerate their yield ramp for their new products.

For this work, a commercial 128L RG 3D NAND device was acquired and de-packaged. A 30um wide by 30um long region of the array was targeted and the structure was delayered via automated Xenon FIB milling processes. The delayering processes used a proprietary gas chemistry injected at the region of interest to maintain milling performance for flatness and smoothness as the milling progressed. This was continued until the targeted region was delayered to the bottom of the memory stack. At each layer, a high-resolution SEM image was automatically acquired providing metrology source images for the entire volume. These SEM images were analyzed via Thermo Fisher Metrology and Avizo software to extract profile and global registration information. This data was then correlated to create the volumetric data used in this work. Individual memory holes were characterized from the data set to extract orientation, shape, positional shift, and tilt as a function of column position and word line number. Arrays of 162 memory holes were collectively analyzed to extract etch trend information as a function of column and row position, as well as word line number.

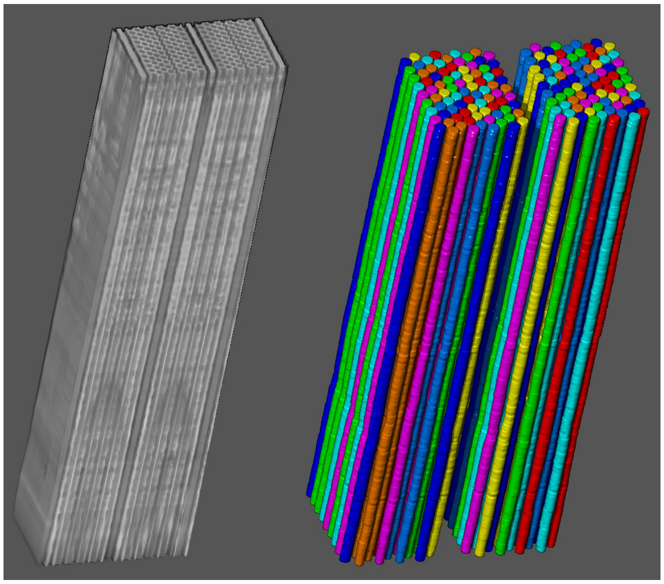

FIGURE 1. 3D NAND memory holes from 128L SSD showing shift, profile, and orientation by word line number

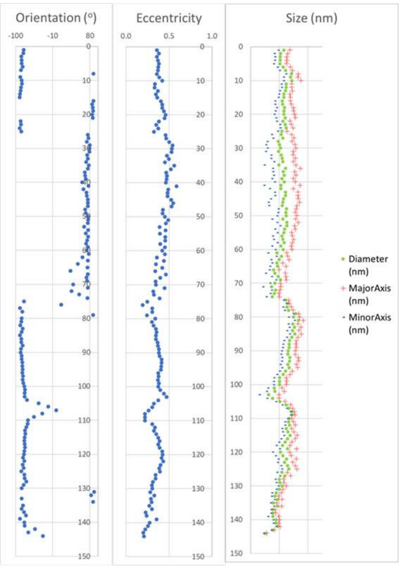

FIGURE 2. Memory hole orientation, eccentricity and critical dimensions versus word line number

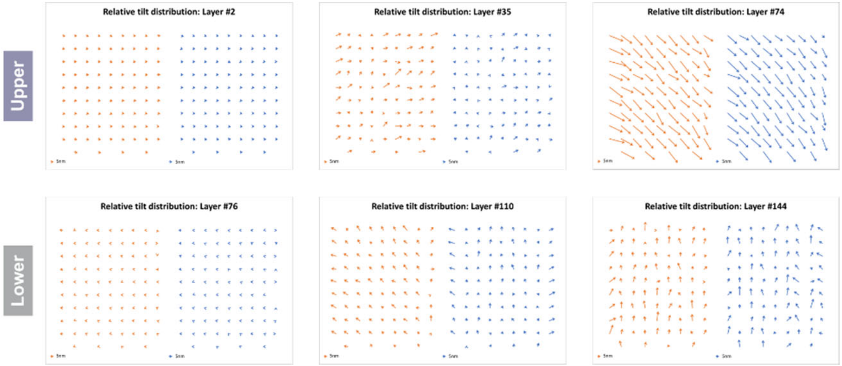

FIGURE 3. Memory hole array etch tilt vector vs word line number examples

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KEYWORDS

NAND, 3D profiling, memory hole, tilt, HAR etch, HAR etching

Methods for Achieving Atomic-Scale Analytical Tomography

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INTRODUCTION

Atomic-Scale Analytical Tomography (ASAT) has been recently defined as the ability to identify every atom in its place [1], [2]. Specifically, ASAT is the ability to determine the isotopic identity and sub-Angstrom position of 100% of the atoms in a specific volume. Taking this a step further, ASAT should also be able to determine the local electronic structure of these atoms, thus giving rise to true 3-D atomic structure / electronic property relationships. ASAT datasets of semiconductor nanostructures will reveal the 3-D position of individual dopant atoms with pm spatial resolution, the 3-D position of nuclear spin isotopes, nanometer scale changes in strain due to structural defects and lattice mismatch, the 3-D position of point defects such as vacancies, and any electronic band structure changes at all these atomic-scale features.

How Can ASAT be achieved?

Undoubtedly, ASAT is a lofty metrology goal but is nearly within reach. Contemporary metrology techniques such as (Scanning) Transmission Electron Microscopy ((S)TEM) are not currently capable of ASAT. (S)TEM can image atomic positions with better than 0.01 nm resolution in some specimens and tilt-series tomographic imaging can give 3-D information, sometimes at atomic resolution [3], [4]. Analytical STEM can be performed at atomic resolution in some cases, although identifying a single atom in 3-D is only possible in limited specimens and with poor depth resolution. Atom Probe Tomography (APT) can provide mass spectral information on individual atoms, however, 3-D image reconstruction methods are constrained by multiple empirical assumptions and lack of information about the specimen that limit the spatial resolution.

Recently, it was demonstrated that correlative TEM and APT on the same specimen can approach ASAT [5]. The authors used TEM imaging of the specimen before and after APT to define the analyzed 3-D volume. TEM diffraction was used to define atom positions within that volume (a dataset known as the specimen function) using information about the crystal space group, orientation, and lattice parameters. More work needs to be done using correlative TEM and APT to achieve ASAT, including demonstrating the ability to capture structural features such as interfaces and defects as well as 100% efficiency ion detectors [6].

Towards ASAT for Nanoelectronics

Capturing structural features such as heterojunctions and dislocations requires detection of small changes in lattice parameter with high spatial resolution. Using 4-D STEM, strain can be quantified with better than 5 pm changes in lattice parameters at sub-nm real space length scales. Figure 1 is a demonstration of 4-D STEM strain mapping in a SiGe nanowire device within a cylindrical APT specimen. Si quantum dots embedded within the 75 nm wide nanowire channel induce anisotropic strain fields as evidenced by changes in lattice parameters in the horizontal direction versus the vertical. Knowledge of the crystallographic orientation, space group, and lattice parameters enables 3-D atom positions to be determined before the APT experiment. Following APT, isotopic information can be assigned to the atom positions using ion trajectory aberration correction methods.

In the near future, ASAT will be achieved through integration of 100% efficiency ion detectors, improved data handling algorithms, and integration of TEM and APT into a single instrument.

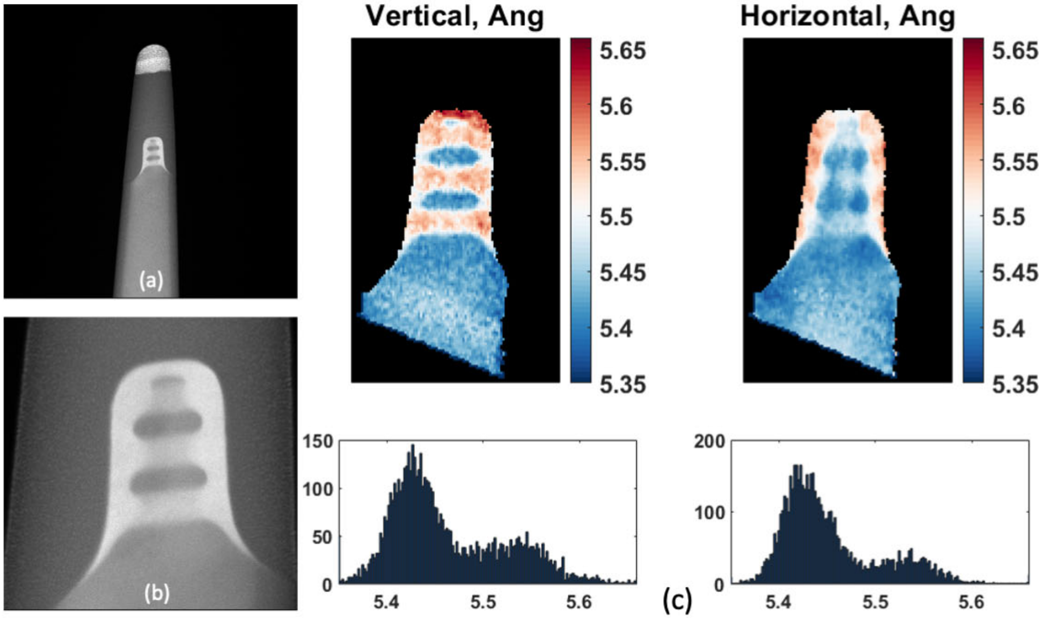

FIGURE 1. Example data collection for ASAT on a vertically stacked Si quantum dot embedded within a SiGe nanowire. (a) and (b) are STEM-HAADF micrographs of the 75 nm wide nanowire present within a FIB-processed cylindrical specimen. (c) Using 4-D STEM diffraction mapping and Exit-Wave Power Cepstrum (EWPC) analyses [7], lattice parameters can be measured in the vertical (left) and horizontal (right) directions. The color maps and lattice parameter histograms (bottom) illustrate the ability of EWPC to quantify lattice parameters to better than 0.05 Angstroms. Sample courtesy of Dr. Emily Turner and Prof. Kevin Jones (Univ. of Florida).

KEYWORDS

3-D, Atomic-Scale Characterization, TEM, APT, Tomography, 4-D STEM, ASAT

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Ultra Low Energy SIMS Depth Profiling of 2D Materials

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INTRODUCTION

Secondary Ion Mass Spectrometry (SIMS) is a very precise surface-sensitive analytical technique. A sample is bombarded with a primary ion beam which leads to the sputtering of the matter from its surface. A small part of the sputtered particles are charged (secondary ions). They are collected and undergo spectral analysis which provides information about their mass to charge ratio. A proper interpretation allows determining the elemental and/or isotopic composition of the sample. Subsequent layers of the sample are removed during the analysis and thus it is possible to determine how the composition changes as a function of depth, creating so-called depth profiles. The lateral analysis of the signal allows the creation of 3D images and cross-section views of the sample.

Application of ultra-low impact energy (90-150eV) in SIMS techniques practically eliminates the mixing effect and allows to reach sub-nanometer depth resolution. However, the typical ion yield for such experiments is very low and an average intensity of signals is in a range of a few hundred counts per second at best. To overcome this problem dedicated measurement procedures have been proposed and established: primary beam and extraction parameters are optimized for the detection of a single type of element in a specific material system. In this way, ion yield is significantly increased (up to three orders of magnitude) and detailed characterization of a material maintaining the sub-nanometer depth resolution becomes possible. This approach, while certainly time-consuming, is invaluable for the characterization of 2D materials.

GRAPHENE

Integration of graphene with the existing fabrication lines may be possible only if the growth process fulfills the high purity requirements of the front-end-of-line integration approaches. While many analytical techniques may provide information about the concentration of contaminants, their dimensional sensitivity is usually poor and thus it is not possible to assess which contaminants are located above/below graphene and which are incorporated into its structure.

Due to the measurement artifacts (transition layer, ion mixing, and preferential sputtering), SIMS measurements performed in standard conditions do not reach the desired depth resolution, as shown in Figure 1A. However, the optimized measurement procedure, as shown in Figure 1B, combines excellent detection limits (0.8 - 2.9 ppm) and subnanometer depth resolution. It confirms the presence of sodium and sulfur at the surface of the graphene layer, the formation of graphene-copper composite, and allows the detection of molybdenum and tungsten at the interface between graphene and the germanium substrate. [1]

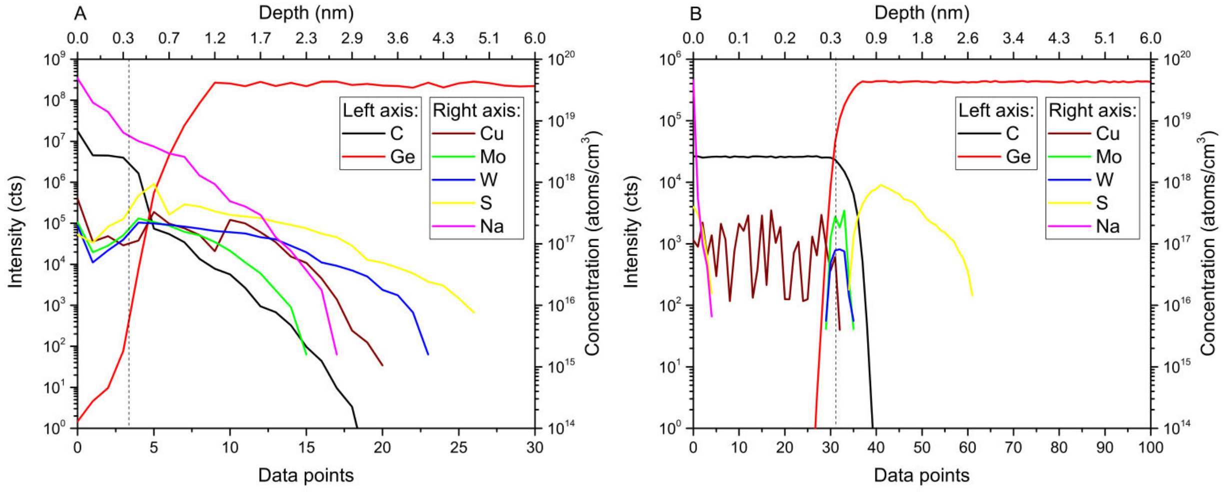

FIGURE 1. SIMS depth profiles of a graphene/germanium sample. A dashed line indicates an interface between graphene and the germanium substrate at the point where the carbon signal drops to 50%. Depth calibration has been performed separately for both regions. Part A: standard measurement conditions, the presence of various contaminants can be confirmed but their exact location cannot be precisely determined due to measurement artifacts. Part B: optimized measurement conditions, the location of each contaminant can be precisely determined.

Such precision is also valuable for failure analysis. Noise-based evaluation of the quality of Al_2O_3-passivated graphene on 4H-SiC(0001) Hall effect sensors has revealed an asymmetrical aging process which suggested a possible degradation of graphene properties due to unintentional and uncontrolled contamination. SIMS analysis has shown that selective removal of the passivation layer at metal contacts has allowed lateral migration of contaminants between graphene and the passivation layer.

MOLYBDENUM DISULFIDE

Complementary use of a position-sensitive detector allows elemental mapping and phase identification of 2D materials. SIMS analysis of MoS_2 layers grown on SiO_2, Al_2O_3, BN, and graphene/SiC system reveals oxygen out-diffusion from the substrates containing oxygen and formation of an amorphous MoOS layer in addition to MoS_2 Total area of MoS_2 domains covering substrate is directly related to a type of substrate. For SiO_2 small triangular domains of MoS_2 separated by amorphous MoOS material are observed. For Al_2O_3 the size of MoS_2 domains is drastically improved due to the higher stability of sapphire. For BN substrates SIMS measurements reveal a uniform MoS_2 coverage over a whole 2-inch wafer. [2] The most surprising effect is observed for the graphene/SiC system, where MoS_2 film is grown between graphene and silicon carbide. Further SIMS experiments reveal that the intercalation process occurs via the atomic step edges of SiC and Mo and S atoms gradually diffuse along SiC atomic terraces leading to the creation of the highly oriented MoS_2 layer. [3]

MXENES

Application of the SIMS technique for MAX and MXene characterization yields important direct information about their structure: for some samples, oxygen atoms are incorporated in the carbon (X) sites. Thus, MAX and MXenes should be considered as early transition metal oxycarbides and not carbides as it is commonly assumed; the composition of surface termination layers can be precisely monitored; for some out-of-plane ordered MAX and MXenes, the transition metal layers are not fully separated. Measurements reveal that for Mo_2TiC_2 a perfect separation exists: Mo atoms occupy the outer layers, whereas Ti atoms occupy the inner layer only. In the case of Cr_2TiC_2 partial mixing exists: Cr atoms occupy the outer layers, whereas Ti atoms occupy the inner layer in addition to some Cr atoms, thereby forming a solid solution on the M site.

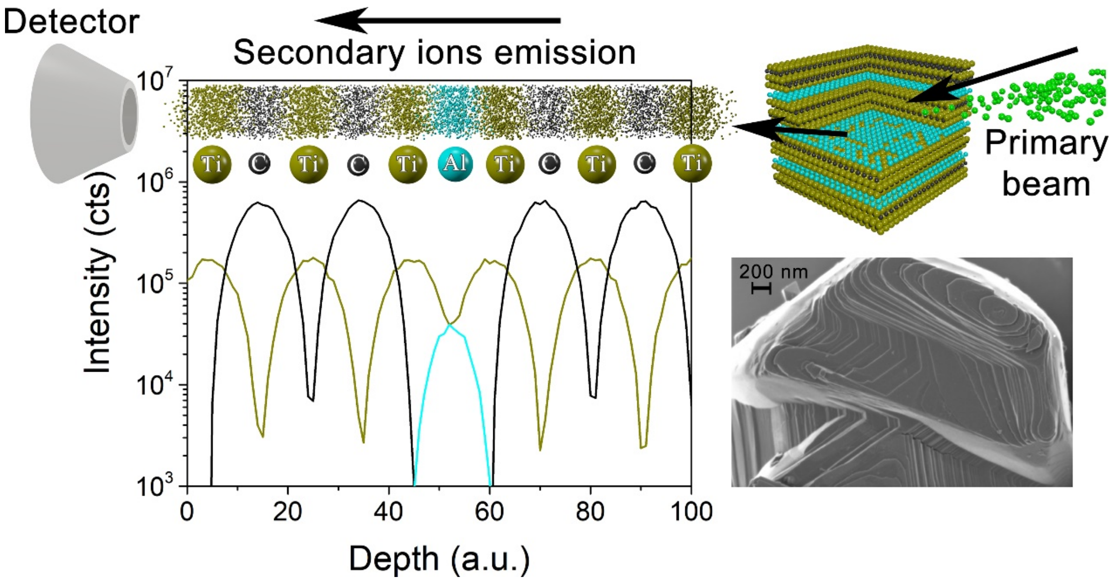

FIGURE 2. An example of SIMS experiment with atomic depth resolution performed on Ti_3AlC_2 MAX sample.

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KEYWORDS

Secondary ion mass spectrometry, SIMS, 2D materials, graphene, molybdenum disulfide, MXenes

Photoelectron Spectroscopy in Device Technology: from XPS to HAXPES

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INTRODUCTION

Device technology encompasses nowadays a wide variety of devices fabricated on integrated circuits (ICs), from Complementary Oxide-Metal-Semiconductor (CMOS) devices for logic and power applications and non-volatile memories to various sensors and optical components. Prior to high-volume manufacturing, research and development (R&D) is necessary in order to qualify the integration of new materials and related processes. As down-scaling proceeds further towards the limits of Moore's law, the characteristic device dimensions drastically decrease down to a level where the role of interfaces in the final performances of ICs is getting more and more important[1] and requires more reliability in their control. Photoelectron spectroscopy such as XPS plays a key role in the metrology of ultra-thin layers as well as at characterization facilities of R&D labs. The recent advent of Hard X-ray Photoelectron Spectroscopy (HAXPES) at the laboratory scale is a huge step forward for the reliable qualification of materials and critical interfaces in the R&D phase of device production, and may also play a key role at the metrology level in the future. Here, we present some recent examples of the use of HAXPES in the field of characterization of technologically-relevant systems.

HAXPES FOR DEVICE TECHNOLOGY

XPS played a key role in the early days of microelectronics, enabling the detailed study and understanding of the critical Si/SiO_2 interface in CMOS devices[2]. The interfaces of interest for characterization or metrology are most of the time deeply buried underneath metal electrodes or oxide layers and/or localized in small areas, which has been an increasing challenge for XPS. Also, the diversification in logic device architectures and types is involving a large variety of materials and is driving the need for innovative ways of analyzing. For some years, the challenge of characterizing deeply buried interfaces was addressed at Leti by implementing synchrotron radiation[3,4], offering excellent energy resolution but poor analytical throughput due a poor accessibility. The recent advent of HAXPES with lab-scale instruments enables answer to practical analytical needs at the R&D level in nanoelelectronics. The instruments are nowadays proposed from different manufacturers with a broad range of photon energies enabled by different X-ray technologies: conventional X-ray sources from solid-state anode for Silver Lα (2984 eV photon energy) and Chromium Kα (5415 eV)-based excitations and liquid-jet technology for Gallium Kα excitation (9250 eV). The application of Cr Kα HAXPES to nanoelectronics was demonstrated some years ago[5], and its implementation in analytical laboratories is now quickly increasing.

There are several key advantages of HAXPES over XPS, the first one being the larger probing depth enabled by the increased inelastic mean-free path of more energetic photoelectrons excited by harder X-rays. Typically the gain is a factor of 3 larger with Cr Kα photons, making possible to probe buried layers and interfaces at depths larger than 10-15 nm, without the need of potentially invasive sputtering. As a result of a more pronounced bulk sensitivity, the proportion of the signal arising from the outermost surface becomes negligible, and therefore in case of sputtering the damaged zone of the material is not dominating anymore the collected signal. Another advantage is regarding the larger number of photoelectric lines being available, as illustrated in Fig. 1 in the case of a multilayer stack of thin nitride layers frequently used in logic or power devices. In XPS, the low binding energy part of the spectrum is characterized by multiple photoelectric lines much difficult to disentangle, particularly for measuring the composition of the buried GaN interface. Moving to HAXPES, we obtain well isolated photoelectric lines (Si 1s, Al 1s, Ga 2p) allowing further analysis, with minimal interferences with Auger lines.

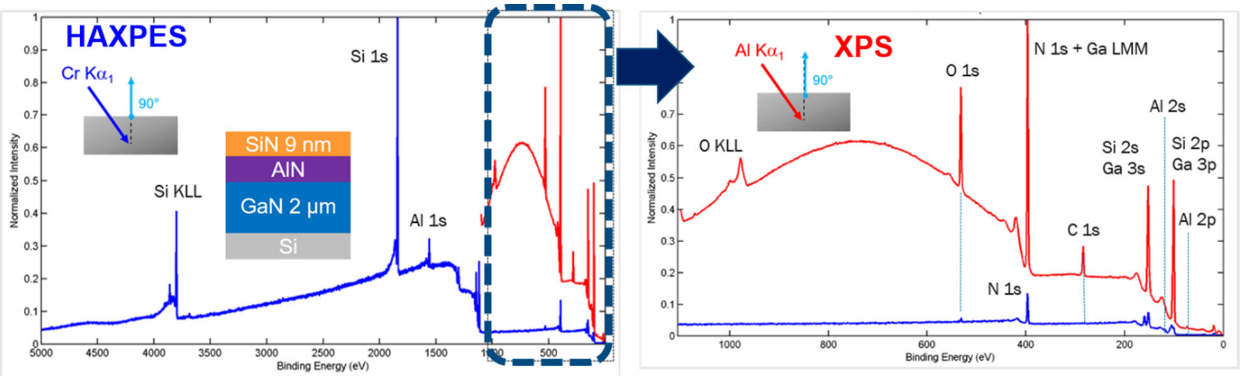

Figure 1. Comparison between XPS and HAXPES survey spectra of a stack of nitride layers. The thickness of the AlN layer is 4 nm.

Moreover, accessible transitions over a large range of kinetic energies, and therefore, characteristic probing depth, allows for variable depth analysis and quick qualitative diagnostics regarding the spatial organization of layers within a sample. This was demonstrated previously for Ti[5], using the two extreme Ti2p (*~4950* eV kinetic energy) and Ti1s (*~444* eV kinetic energy) lines. Quantitative in depth analytical methods are getting more and more accurate, either using core line intensities in angle-resolved HAXPES, or exploiting the inelastic background which allows up to 50 nm probing depths, an interesting method which will be further discussed. Finally, important aspects of HAXPES for R&D in nanoelectronics are energy resolution on the one hand and sensitivity on the other hand. Routine energy resolution in HAXPES remains below 1 eV, thereby still allowing chemical state fingerprinting. Sensitivity mainly derives from photoionization cross-sections, which are known to decrease drastically at higher excitation energies. In Table 1, cross-section values are shown in XPS and Cr Kα-HAXPES for some key elements in nanoelectronics : it is shown that the cross-sections are similar between low-energy and high-energy transitions. This means that the sensitivity of the HAXPES analysis is maintained compared to XPS. Other examples will be considered and further discussed.

TABLE 1. Photoionization cross-sections (kb) in XPS and Cr Kα-HAXPES of some key elements in nanoelectronics, after Ref. [6].

Transition	Si2p	Si1s	Ga3d	Ga 2p	Al2p	Al1s
XPS cross-section	6.25		7.26		4.05	
HAXPES cross-section		8.13		6.62		6.24

APPLICATION TO ADVANCED FERROELECTRIC DEVICES

Recently, ferroelectric HfO_2-based devices have attracted much attention with potential breakthrough in low-power logic and memory applications[7]. In ferroelectric random access memory (FeRAM) devices, the active HfO_2 layer is used in a metal-insulator-metal (MIM) structure where the performances are deeply linked to the defects within the dielectric HfO_2 layer. Indeed, the ferroelectric phase has to be stabilized either by the addition of dopants such as Si[8] or La[9] or by the creation of oxygen vacancies[10]. It is therefore of primary importance to be able to probe these defects in order to tune the device properties. In this regard, HAXPES is a relevant technique to help understanding the chemistry and electronic properties of the interfaces in MIM structures. Fig. 2 shows the example of a TiN/Ti/Si:HfO_2 stack investigated by HAXPES. It is seen on the survey spectrum that using Cr Kα radiation, a very broad and intense Ti KLL Auger peak gives rise to an extended inelastic background overlapping the region of the Hf3d$_{5/2}$ core line, the most intense Hf core-level. However, despite this interference, it is still possible to record an exploitable Hf3d$_{5/2}$ signal as seen on the high-resolution spectrum shown on Fig. 2. The analysis of this spectrum allows evidencing the presence of different valence states of Hf in the top interface, related to the formation of oxygen vacancies

Other applications cases will be considered and further discussed.

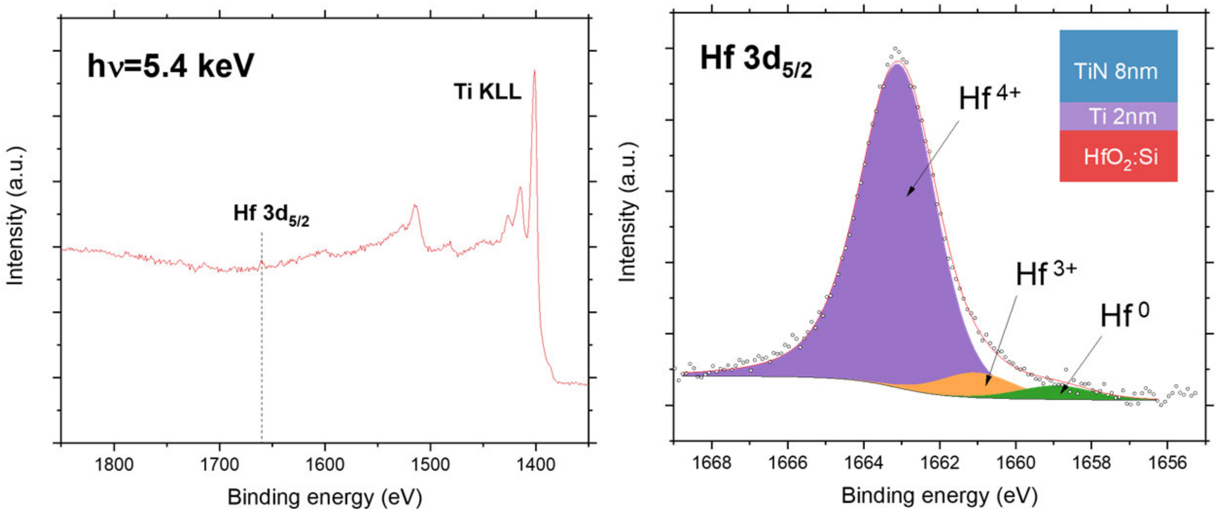

Figure 2. HAXPES spectra of a TiN/Ti/Si:HfO$_2$ stack: Ti Auger region of the surver spectrum (left) and high-resolution Hf $3d_{5/2}$ spectrum. The initial TiN thickness (18 nm) was reduced down to 8 nm using controlled Ar$^+$ sputtering, without influencing the interface chemistry (as checked with a bulk HfO$_2$ sample).

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KEYWORDS

XPS, HAXPES, nitrides, memories, hafnia

Advanced Electron Microscopy Techniques to Investigate New Semiconductor-Related Materials and Devices

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INTRODUCTION

With the critical dimensions of key integrated circuit components, especially in field effect transistors (FET) shrinking from the nanometer to the atomic scale comes the increasing need to image and characterize the device structures at atomic resolution and with sub-picometer precision. Aberration-corrected (scanning) transmission electron microscopy (S/TEM) offers imaging with a sub-Å lateral resolution, but with a precision of only a few pm, and the depth resolution being >50× worse. To better understand and improve the properties of these devices, it is important to have a robust imaging method for precisely determining the strain fields as well as the 3D structural information for both light and heavy elements. Additional functional information is needed for proposed nanodevices based on quantum materials to complement or augment CMOS, especially for low energy operation and non-volatility [1]. The physical properties in quantum materials that encode information are often associated with a collective state characterized by a corresponding order parameter, e.g., magnetization (polarization) in a ferromagnetic (ferroelectric) material. Thus, developing a robust method for visualizing and characterizing these order parameters is a critical step to help understand the physics and improve nanodevices.

In this talk, I will show how quantitative physical information can be obtained using four-dimensional STEM (4D-STEM) diffraction imaging that would not otherwise be possible, including strain, 3D positions of dopant atoms, polarization, electric and magnetic fields.

Robust Imaging of Strain and Single Dopant Atoms

In semiconductor technologies, strain is introduced to boost the performance of transistors by tuning the electronic band structure. Recent developments in four-dimensional STEM (4D-STEM) diffraction imaging have demonstrated the strain measurement precision of <0.1% with spatial resolution of ~1 nm in FET devices [2,3]. 4D-STEM works by using an electron microscopy pixel array detector (EMPAD) [4] to record the 2D electron diffraction pattern over a 2D grid of probe positions, resulting in 4D datasets. Here, we demonstrate the potential of the exit-wave power-cepstral (EWPC) transform as a fast and dose-efficient technique to extract strain information in 4D-STEM datasets [5]. The EWPC transform deconvolves low frequency noise and exploits the periodicity in the diffraction patterns, which is less sensitive to crystal mis-tilt or thickness artifacts. These factors combined with a very fast run time (1-10 ms/pixel) makes this technique potentially well suited for high-throughput applications.

Three-dimensional atomic structures and crystal defects govern the electronic, magnetic and optical properties in nanomaterials, such as point or line defects in semiconductor devices. To image internal structures and composition variations, tilt-series electron tomography has been a reliable way to provide 3D information at the nm- and atomic scales, but it has constraints from dose limitations of the sample, electron channeling artifacts, tilting range and field of view, and number of projection images. Recent advances in 4D-STEM multislice electron ptychography have demonstrated a lateral resolution of <20 pm on a crystalline specimen [6]. More importantly, multislice electron ptychography also allows for 3D structure determination for both light and heavy elements, because it iteratively retrieves the sample's structure at different layers and recovers a linear phase response versus thickness. Here, using 4D-STEM multislice ptychography at a single projection, we demonstrate the 3D imaging of a single Tm dopant atom at depth z=4 nm in a 31-nm thick $Gd_3Ga_5O_{12}$ sample with ~3 nm depth resolution while maintaining a sub-Å lateral resolution [7].

Beyond-CMOS: Characterization of Quantum Materials and Their Order Parameters

Quantum materials offer the promise of additional functionality not accessible with the current set of CMOS-oriented technologies, especially from an energy efficiency perspective. Specifically in multiferroics, the interplay between order parameters such as spin, lattice strain, polarization, orbital, charge degrees of freedom often can be used to encode bits of information. More interestingly, topological textures such as skyrmions consisting of real-space arrangements of order parameters can emerge as manipulable particle-like objects in ferroic materials, which have potential applications in next generation memory devices [8]. As those ferroic textures are intrinsically nm-scale and dynamic, developing methods for visualizing and characterizing their detailed 3D structure is a critical step in understanding their properties and exploring possible phase transitions. Here, we show how robust imaging of those order parameters is enabled by 4D-STEM, which further allows us to study the detailed structures of topological textures and explore their possible phase transitions. First, I report the emergence of achiral polar meron lattice (topological charge of +1/2) from disordered but chiral skyrmion (topological charge of +1) phase transition driven by elastic boundary conditions [9]. Second, I report the observation of room temperature Néel-type skyrmion in a van der Waals ferromagnet accompanied by a change in crystallographic symmetry and chemical order [10]. These results may offer a promising way to control their functionalities in ferroic nanodevices using the local and spatial distribution of chirality and order.

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KEYWORDS

Strain, ferroelectric, ferromagnetic, skyrmions, 4D-STEM

Xray Metrology Challenges for the Semiconductor Industry

Joseph Kline

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Characterization and Metrology for Silicon Photonic Quantum Computing

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ABSTRACT

PsiQuantum's approach to building a general-purpose quantum computer is underpinned by three focus areas (i) a fault tolerant architecture, (ii) manufacturable qubits, and (iii) a scalable technology. A fault tolerant computer can be realized by fusion-based quantum computing (FBQC) using photonic qubits [1]. A manufacturable integrated photonics platform is capable of on-chip generation, manipulation, and detection of photonic qubits. The technology is intrinsically scalable as it is assembled leveraging an integrated silicon photonic chip, standard CMOS electronics for qubit control and chip-to-chip photonic qubit interconnectivity with optical fibers for modularity. The on-chip single photon detection is achieved using superconducting nanowires, which operate at cryogenic temperatures. It is important to note that these superconducting detectors operate at a few Kelvin temperature with high internal detection efficiency and do not require milli-Kelvin temperatures in dilution refrigerators like superconducting qubits.

This manufacturable photonics technology is being jointly developed with our semiconductor foundry partner. The development efforts include the addition of new materials and process integration modules in an integrated stack which meet the performance requirements of our photonic components. The development of these new materials for cryogenic operation, drives the need to corelate device performance to metrology measurements at room temperature or alternatively the material properties are characterized at cryogenic temperatures. In this talk, the characterization and metrology efforts on some of our materials is presented.

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KEYWORDS

Silicon photonics, quantum computing, qubit, superconducting, cryogenic

Using Deep UV Wavelength Broadband Plasma Optical Inspection for EUV Print Check and High NA EUV Development

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INTRODUCTION

Extreme Ultra Violet (EUV) lithography is now in the high volume manufacturing (HVM) phase enabling advanced device scaling and simplification of patterning schemes. Two top issues the EUV community is focused on in 2022 are meeting thin resist resolution with minimal stochastic defectivity and keeping reticles defect free [1]. Process control has a critical role to play in meeting these objectives. KLA has developed process control solutions using a Deep UV (DUV) wavelength broadband plasma optical wafer inspector for 1) EUV reticle contamination monitoring 2) Stochastic defect detection, and 3) EUVL process window qualification. We will provide an overview of these methods and deeper insight into the EUV print check product developed for reticle qualification. We will also provide an outlook on the challenges associated with high NA EUV development and KLA's roadmap to address those challenges.

EUV RETICLE CONTAMINATION MONITORING

IC manufacturers are intensely focused on EUV reticle yield and are adopting comprehensive reticle qualifications strategies to mitigate contamination risks. In addition to the standard optical reticle inspection method, alternative methodologies based on inspection of printed wafers are being adopted to reduce the yield risk caused by particle adders on the reticle. KLA has developed unique methods for high sensitivity repeater detection using broadband plasma (BBP) optical wafer inspection.

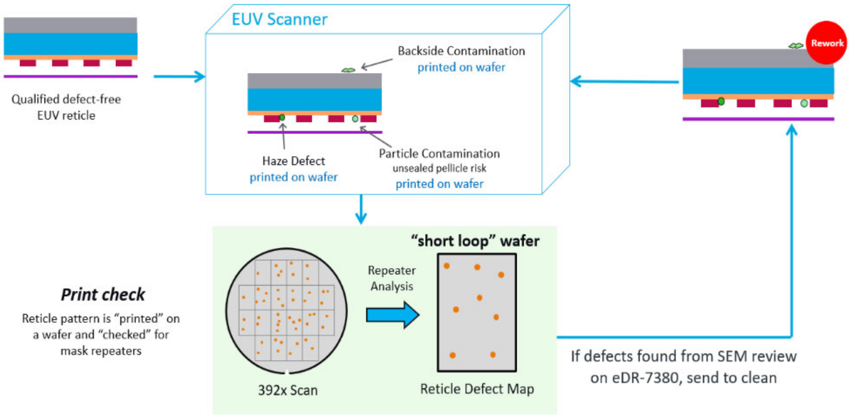

FIGURE 1. EUV Print Check Methodology

The EUV reticle print check inspection methodology (Figure 1) has been developed over the past few years. Used to help find critical reticle defects that can seriously impact yield, the print check method leverages monitor wafers, broadband plasma optical inspectors and e-beam defect review systems. To minimize noise from previous patterning layers, short loop wafers are used in this print check workflow to maximize sensitivity. Print check takes place at the ADI (after-develop inspection) process step to minimize the cycle time for reticle re-qualification.

To meet the high sensitivity requirements for reticle re-qualification in high volume manufacturing (HVM), KLA has developed a combination of optical and algorithmic techniques using KLA's broadband plasma (BBP) wafer inspection systems. BBP wafer inspection leverages illumination in the 190-260nm wavelength range and provides high sensitivity to a variety of critical defects at ADI with acceptable throughput for HVM. New capabilities have been developed to improve the signal to noise ratio through systematic and random noise reduction. KLA's EUV print check solution works on large optical image data sets across the entire reticle row, ensuring sensitivity to repeater defects and reduction in the number of false repeaters reported. In addition, the litho stack used for the short loop wafer inspection is a critical factor for inspection sensitivity. KLA has collaborated with IC manufacturers to develop optimal short loop stacks to be used on monitor wafers, which has demonstrated a significant sensitivity benefit for print check.

The EUV print check solution using BBP has shown unique sensitivity at high throughput and has been adopted by IC manufacturers in both the logic/foundry and DRAM segments. The print check method is complementary to KLA's optical reticle inspection systems, with both techniques playing a role in minimizing escape risk for reticle defects during chip production.

PROCESS WINDOW QUALIFICATION

With continuous technological advancements in the semiconductor industry, there is constant drive to attain smaller dimensions for IC fabrication. With semiconductor chips being at the forefront of many new applications, there are many layouts needed to enable this. In advanced nodes the overlapping process window for any layout is getting smaller and smaller. Therefore, it becomes very critical to comprehend the boundaries of that overall process window. IC manufacturers use the Process Window Qualification (PWQ) methodology, which utilizes DUV broadband plasma optical wafer inspection and state-of-the-art design algorithms, to help understand the process window. PWQ serves as an HVM monitoring solution by effectively detecting systematic design and lithographic weak spots, and tracking different layouts and structures.

STOCHASTICS QUALIFICATION

EUV lithography is more prone to stochastics effects – events that have random variables. Random local variations that occur between structures cause unwanted defects, impacting the performance of the chip, including the possibility of causing the device to fail [3]. To accurately quantify the stochastics failure rate, the entire area of a wafer needs to be inspected at high sensitivity driven by the advanced design pitch. Broadband plasma optical wafer inspection captures critical defects of interest at high throughput with full wafer coverage, which is requirement for stochastics monitoring in high volume manufacturing.

HIGH NA EUV DEVELOPMENT

As EUV moves into the next phase of development with high NA optics, it requires further improvement of resist performance, such as resolution and sensitivity. Both photon and material stochastics monitoring is gaining more traction in this regard as IC manufacturers qualify various thin resist materials. Anamorphic optics on the high NA scanner impact the max field size for the reticle by 50% and could lead to 2x reticle exposures on the 0.55NA platform versus the 0.33NA platform. This increases yield risk further for any particle contamination that occurs on EUV reticles [4]. The smaller device pattern pitch and higher pattern density at the design nodes targeted with high NA EUV necessitates the need to extend the EUV print check roadmap to address the critical reticle qualification needs. BBP has roadmap to address the sensitivity requirements needed to support high NA EUV stochastics monitoring and print check. These enhancements include optical and algorithmic approaches for signal to noise improvement for both ADI and after-etch inspection (AEI) monitoring steps.

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Observing Invisible Electrical Fails with e-Beam DirectScan

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INTRODUCTION

Critical dimensions in most advanced generations of silicon technology are reaching 10-15nm. At such small geometries optical defect inspection is running out of steam. Moreover, it is also not capable of detecting defects which are hidden below the surface. Especially at 7nm and below, many yield and reliability killer defects are the result of interactions between lithography, etch, and fill [1]. Detection of surface and subsurface defects with high sensitivity and low nuisance rate is becoming a challenge in technology development and mass production. Conventional e-beam tools can detect the defects [2], but lack the throughput to scan silicon chips for defects at very low, parts-per-billion fail rate levels. A solution is required with several orders of magnitude higher throughput than conventional e-beam tools without sacrificing the ability to measure sub-20nm feature sizes. PDF has developed the DirectScan technology to scan billions of patterns of interest per hour. This DirectScan technology is an e-beam inspection technology that is designed and optimized to scan random product layout patterns. Voltage Contrast (VC) signal is collected from selected patterns suitable for inspection, and electrically active defects are detected based on the response to the e-beam stimulus. Using sophisticated product layout analyses, scanning recipes are created to drive the e-beam tool time of DirectScan technology to focus upon measuring relevant, VC observable layout shapes.

NEW E-BEAM BASED INSPECTION PLATFORM

PDF Solutions has developed a new e-beam-based inspection system which focuses upon detecting electrically active defects, including such buried defects as shown in Fig.1. Defect detection is based on identification of unintended shorts or opens, using the modeled VC response. The tool can detect defects at the physical layer that is exposed when the inspection is performed as well as detect the defects already present at the lower levels, provided that connectivity allows unconfounded identification of the VC response.

Multiple components had to be developed to build the system for efficient detection of defects. A new type of e-beam tool was developed to scan and test selected locations of interest on the wafer. A proprietary layout profiling tool (FIRE^{TM}) was adapted to extract layout attributes, identify locations that would be relevant to a given type of yield issue, and to export location coordinates for inspection. Finally, a dedicated data collection and analysis flow were built (based on PDF Exensio analytic platform) to support fast defect identification and statistical analysis.

The eProbe®250 e-beam system is designed, produced, and offered by PDF Solutions. The system is tuned to perform VC measurements using vector scanning mode. By operating in vector scanning mode, the system is able to dedicate all the e-beam measurement time to measuring locations on the wafer that actually matter (Fig. 2). The software embedded in the eProbe system performs real-time registration during measurement and employs an artificial intelligence-based system for learning the relationship between the IC layout and the measured VC gray level signals, used to identify defective sites on the wafer.

The throughput of the eProbe®250 is dictated by the field of view (FOV) and the stage speed. In most cases it operates with a FOV of 45 um x 45 um and can travel at a stage speed up to 100 mm/sec. The resulting throughput enables full wafer scans within 2-4 hours, making the tool suitable for high volume production mode where queue time limitations impose stringent time constraints.

Design For Inspection (DFI) Characterization Applications

Multiple applications which we refer to as Design For Inspection (DFI) applications have been developed based on the eProbe inspection platform [3]. In this paper, we focus upon the DirectScan application which consists of inspecting the actual layout patterns that are present in an IC design. Additional applications include embedding specially designed test structures in product layout, scribe line area, or test chips, that are sensitive to critical defects and failure modes, detectable by Voltage Contrast. These test structures can be implemented as DFI Filler cells to replace conventional filler cells in IC designs. Test structures placed in scribelines or test chips enable overlay and process window monitoring using eProbe [4].

DirectScan

The goal of the DirectScan application is to inspect a given layer of a product to detect yield and reliability relevant defects [5]. The eProbe®250 has successfully measured layers with feature sizes as small as 1x metal layers in 4nm technology. The DirectScan work flow consists of four stages as depicted in Figure 3. The first step is to identify a fail mode or set of fail modes of interest. This step dictates the layer at which the given wafer will be scanned. The second step consists of analyzing the product layout and generating the measurement recipe. PDF's proprietary FIRE software is used to analyze the product layout. This software identifies electrically relevant layout patterns for the selected fail modes. The next step is the actual measurement of the wafer on the eProbe tool. The final step is the analysis of the resultant data.

An important characteristic of the DirectScan technology is the ability of focusing the inspection on particular failure modes and optimizing the inspection for throughput and speed. Fig 4. Illustrates this approach, showing a portion of a layout at a metal layer. First, the layout profiling software tool FIRE is used to identify metal line segments which can provide useful information (conventional tool would scan whole area, with all patterns included).

Once the metal patterns are identified and determined to be relevant to a possible failure mode (opens or shorts associated with various layout configurations), the recipe can be built to target only the subset of metal polygons relevant to the Failure mode of interest. This enables high observability at parts-per-billion level and supports fast defect learning and improvement using DirectScan.

DirectScan has been applied to detect buried defects in multiple advanced node technologies. In one example, it was used to identify the layout patterns that were responsible for the yield fallout at a metal layer in 7nm technology. This entailed scanning over 20 billion instances of layout patterns per wafer. Dark defects were identified and classified into layout pattern families, thereby establishing a fail rate per pattern family. These failrates were measured across numerous wafers spanning multiple process grades and split conditions. This approach enabled detecting and correcting part per billion level defects that were causing several yield points of fallout in mass production.

Conclusion

DirectScan and additional DFI applications are revolutionizing the best in class practices for inspecting sub-surface defects at PPB levels of statistical significance. These capabilities are enabled by the eProbe hardware. The resulting system provides faster yield learning loops which are critical for the types of defects that are limiting yields at advanced nodes. The DirectScan and the broader set of DFI applications presented in this paper have the opportunity to advance the state of the art of the in-line process control, diagnostics, and Failure Analysis.

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KEYWORDS

Defect Inspection, e-beam, Design For Inspection, Voltage Contrast, Direct Scan, New Product Introduction

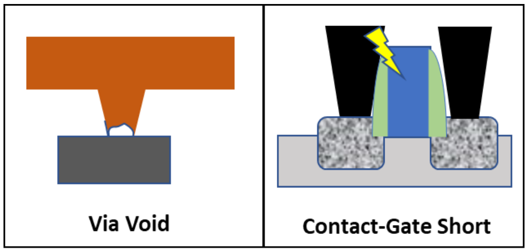

Fig. 1. Example of buried defects detectable by DirectScan. Such defects cannot be detected by optical inspection, and conventional e-beam inspection cannot not provide enough observability to capture defects on product wafers.

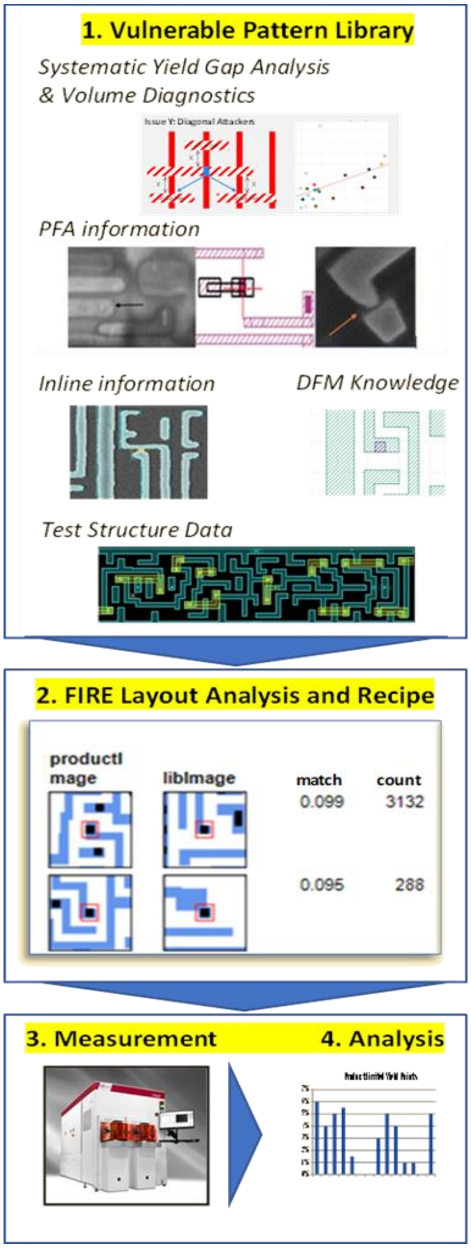

Fig. 3. Direct Scan work diagram, from identifiction of failure types and possible locations to failure mode pareto.

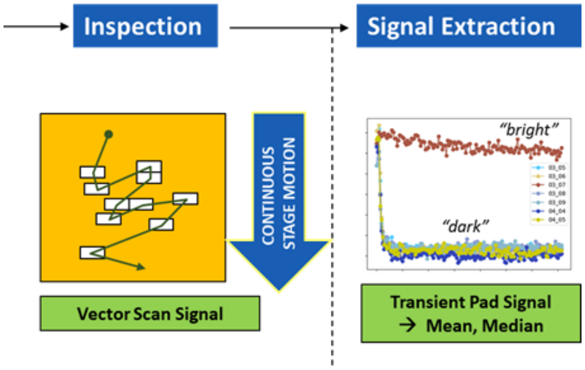

Fig. 2. eProbe tool principle of operation – Vector scan enables high throughput

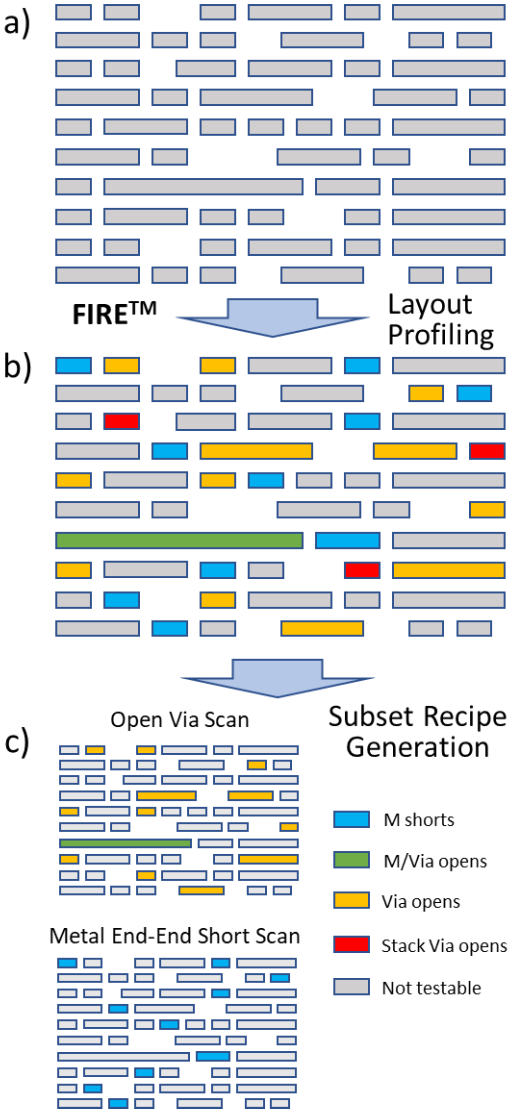

Fig. 4. DirectScan recipe generation – out of all metal patterns (a) only some are suitable for VC inspection (b), and once such instances are identified, the subset recipies can be generated to target particular failure modes (c).

The Status of Actinic Patterned Mask Inspection for EUV Lithography

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INTRODUCTION

Patterned mask inspection is necessarily process step for mask making. Different inspection and metrology tools are used for EUV mask after pattern writing. Optical inspection that utilizes longer wavelength at DUV 193nm, Actinic Patterned Mask Inspection (APMI) using EUV 13.5nm and Electron beam (EB) inspection are the typical patterned mask inspection technologies.

Along with enhancement of semiconductor device performance, resolution limitation of critical dimensional feature printing with all available resolution enhancement techniques forced the industry to move to low exposure wavelength. To accommodate these needs, lithography entered high volume manufacturing at EUV wavelength operating at 13.5 nm, and the semiconductor industry considered lithography-wavelength-matched actinic patterned mask inspection (APMI) tool to be a crucial infrastructure for EUV mask qualification.

Blank manufacturing is the initial step of mask making process. Nanometer-scale bumps and pits on substrate, uniformity of multilayer stack and particles that can translate as defects in wafer printing must be controlled during blank making process. Optical and actinic blank inspection (ABI) are widely used as effective qualification method to detect defect of interest after multilayer coating for defect size and location management during blank manufacturing process.

INSPECTION PERFORMANCE

ACTIS, high sensitivity actinic patterned mask inspection system accommodated the industry demand for lithography-wavelength-matched actinic patterned mask inspection (APMI) tool[1,2]. ACTIS introduces a high brightness EUV source and high-numerical aperture EUV optics to achieve high throughput and high-resolution EUV imaging. It is targeted to accommodate needs for pattern inspections at least up to 3 nm technology node. ACTIS have a superior capability to capture lithographically impacting defects that cannot be seen with the existing DUV inspection tools. The actual results of production mask inspection show that only an actinic EUV inspection system can visualize small surface topology and phase changes that propagate through multilayer stacks. Particle at pattern edge and phase defects are typical defects that cannot be seen with a DUV system.

Early detections of defects within multilayer stack on EUV blanks is a necessary before patterning the mask during expensive EUV mask manufacturing process. In the past, optical blank inspection tool has been used for both EUV and optical blank qualification process. However, utilization of tools that operating at the EUV wavelength produce more reliable detectability of phase defects in multi-layer. Thus, after the multilayer stack is coated on the EUV mask substrate, it is necessary to use an actinic blank inspection (ABI) tool to detect printable defects not detectable with DUV inspection. ABICS is an ABI tool using 13.5nm actinic EUV light for EUV blank inspections that has been introduced by Lasertec filled this requirement[3]. EUV blank manufactures already using it for their qualification process.

FIGURE 1. ACTIS A150: Actanic Pattern Mask Inspection (APMI) System

FIGURE 2. ABICS E120 Actanic Blank Mask Inspection (ABI) System

One of the key features of ACTIS is its high resolution. It is essential for ACTIS to have high resolution to achieve high inspection sensitivity. The results of mask imaging by ACTIS A150 are shown in Figure 3. These line and space patterns have a half pitch of 35nm and 60nm, respectively, on the mask. EUV masks mainly use patterns larger than 60nm, and the current resolution of ACTIS A150 is good enough to make even the 35nm hp mask pattern clearly visible. It has a capability to resolve OPC patterns smaller than the main features. The image in Figure 4 shows a pattern of 80nm contact holes. There is an absorber intrusion of less than 20nm, which is equivalent to 10% CD deviation on a 80nm contact hole, at the center. The signal intensity of this defect is more than 25% larger than that of the other contact holes. ACTIS has demonstrated the capability to visualize and detect 10% wafer CD deviation on 80nm contact holes.

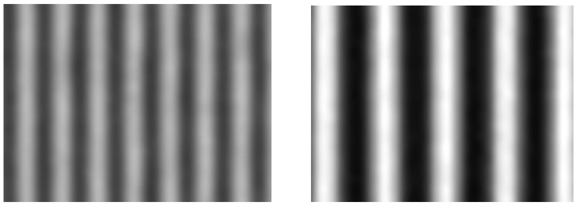

FIGURE 3. Half-pitch 35nm (left) and 60nm (right) line-and-space pattern

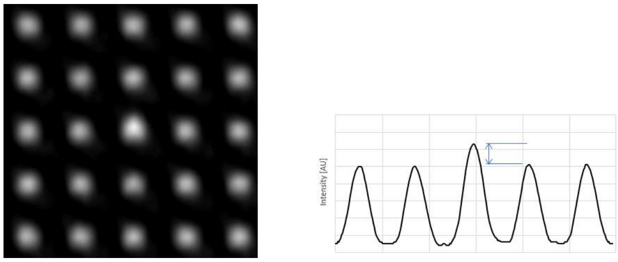

FIGURE 4. Defect review image of ACTIS A150 of a defect on contact hole layer

Inspection Modes of Operation

ACTIS has two inspection modes, die-to-die (DD) and die-to-database (DDB). Die-to-die inspection is for full mask multi-die or partial multi-die area configuration only whereas die-to-database inspection is applicable to single-die or multi-die masks. Initial development of the ACTIS was focus on DD mode only where multi-area inspections within two or more dies in scan direction. Recent advances were made to incorporate the DDB inspection mode capability on ACTIS tool. Currently high-end mask shops are utilizing both die-to-die and die-to-database modes of inspections during EUV mask manufacturing.

EUV pellicle are now utilized on EUV mask. The pellicle material has a characteristic to transmit light only at EUV wavelength. This is the other reason that actinic solution is considered as adequate inspection method for patterned mask qualification. Through-pellicle inspection is another application of ACTIS and in use for printable defect management after pellicle mounting mask shops and multi exposure at wafer fabs in both die-to-die and die-to-database modes.

Figure 5 shows sample images from N5 node. These images contain OPC features in the pattern. The die-to-database image rendering system converts design data to database reference images, which are then compared with image data from the inspection tool to create difference images. In these examples, the algorithm of die-to-database inspection detected a break in the lines, a corner defect, and a particle (from top to bottom).

Figure 6 is a comparison of signal-to-noise ratio (SNR) between DD inspection and DDB inspection. We conducted a test using an EUV programmed defect mask with simple defects of pinhole, intrusion, protrusion, miss size, and pattern shift. Because the reference images rendered by the die-to-database inspection algorithm contain no roughness information of the actual mask pattern, die-to-database inspection has better SNR than die-to-die inspection for all types of defects. In this test result, die-to-database inspection shows about 10 to 20% improvement in SNR. Die-to-database inspection is expected to bring better results to EUV mask inspection. As expected, various layers of production mask inspections performed at mask shops show promising results so far.

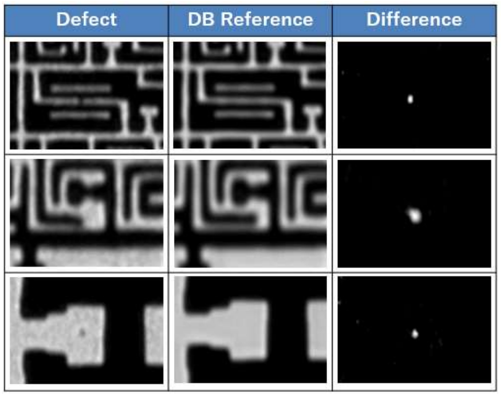

FIGURE 5. Die to database inspection result

FIGURE 6. Comparison between die to die and die to database

For technology nodes beyond N3, a high-NA EUV anamorphic lithography system will be used. The mask structure in the high-NA era will be different from the current configuration[4]. For inspection tool design, a different magnification of mask-to-wafer projection in the vertical and horizontal directions needs to be considered. ACTIS has extendibility to a high-NA system. This will be the next level of development requirement for ACTIS, and any other actinic pattern inspection tools emerges in the industry.

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KEYWORDS

EUV, actinic, patterned mask, blank mask, APMI, ABI, phase defect, inspection, pellicle, high-NA

Soft X-Ray Scatterometry: At-Resolution, 3D Metrology for the EUV Era

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INTRODUCTION

In the EUV era, nanoscale devices have increasingly complex 3D geometries and require revolutionary metrology techniques. Whereas in lithography, the wavelength used to print devices has shrunk—now to 13.5nm EUV light—to keep up with Moore's law, optical metrology instruments have not yet done the same. In the area of overlay metrology, as devices shrink, processing differences between large pitch metrology markers suitable for visible wavelengths of light and real device areas increase, leading to mark-to-device (MTD) offsets. These can be difficult to correct, particularly if they drift in time. Visible light can be used to measure device pitches on thin stacks (i.e. <50nm separation between overlaid gratings), for example using ASML's Yieldstar In-Device Metrology (YS1375) platform. There is an un-met need in the semiconductor industry for a fast, accurate metrology technique suitable for high volume manufacturing (HVM) settings that can measure overlay on device-pitch stacks that also have significant layer separation, as is the case after develop and after intermediate etch steps.

Furthermore, upcoming gate all around (GAA) devices (i.e. nanosheets, forksheets, and CFETs) pose new profile metrology challenges for which there is not yet any established HVM metrology solution due to their complex 3D profiles. Traditional inline metrology techniques such as optical critical dimension (OCD) metrology face significant challenges characterizing these devices, suffering from low sensitivity and increasingly difficult parameter correlations. Transmission electron microscopy can provide accurate and useful information, but it is destructive and slow, making it too expensive in HVM. Thus, a variety of emerging technologies and hybrid combinations of multiple techniques such as OCD, AFM, CD/HV-SEM, XRD, and Raman spectroscopy are under investigation in the semiconductor industry [1].

In this presentation, we share a possible metrology solution well suited to meet these challenges, under investigation at ASML research: soft x-ray (SXR) scatterometry. SXR scatterometry using 10-20 nm wavelength light is a promising next-generation metrology technique with potential for overlay (OVL) and edge placement error (EPE) control, as well as 3D profile metrology applications and the outlook to have sufficient throughput for HVM. As EUV is to DUV lithography, we foresee SXR could relate similarly to optical scatterometry. This wavelength regime offers unique benefits over existing optical metrology tools today:

[1] It enables measurement of device pitch structures, decreasing mark to device offsets observed when large-pitch targets are used as a proxy for device overlay.
[2] SXR provides optimal material contrast, with enough scattering to detect small features in devices.
[3] SXR provides 3D capability, with stack heights of up to several hundred nanometers supported and depth information collected in a single shot due to the use of a broadband source and sensor.
[4] SXR gives strong decorrelation between parameters, allowing many parameters of interest to be extracted accurately and simultaneously (such as overlay, CD, layer thicknesses, and grating tilts).

In this work, we explore SXR metrology in simulation as well as on an experimental testbench. We present measurement results showing both at resolution, after develop overlay capability as well as strong sensitivity to lateral etch time on forksheet devices fabricated by imec.

AFTER DEVELOP OVERLAY

In Figure 1, we present experimental ADI OVL measurements using SXR metrology on device-pitch structures. We demonstrate as low as 0.3nm 3σ set get performance on an after develop litho-etch-litho-etch stack that cannot be measured with visible light because it is *both* at device pitch and has 130nm layer separation. In Fig. 1c, we show shot-noise limited performance scaling with SXR dose. Here, each dot corresponds to measurements of a different field from the same wafer. Furthermore, we see no systematic effects of resist shrink in our overlay measurements. This shows the capability of SXR to measure device pitch overlay directly after litho.

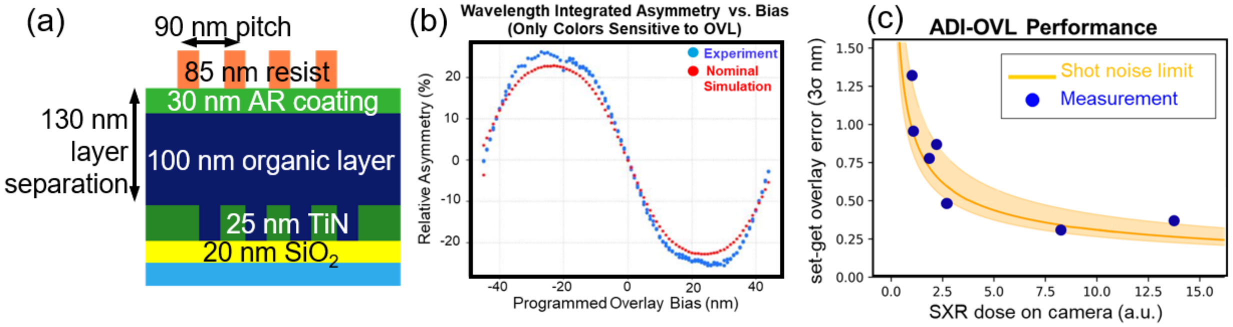

FIGURE 1. (a): ADI Overlay stack measured with SXR. (b): Wavelength integrated asymmetry vs. programmed overlay bias on measured targets spread over a several mm area on one field, as well as simulated response for the *nominal* stack shown in (a) (with no parameter tuning in the model to attempt to match the experimental curve). Here we demonstrate the sinusoidal asymmetric response of the SXR diffraction signal as a function of OVL bias, just as in Yieldstar. (c): Measured set-get overlay error (3σ nm) as a function of SXR dose, with each measurement set from a different field on the same wafer.

3D PROFILE METROLOGY ON GAA DEVICES

A unique benefit of SXR metrology is excellent parameter decorrelation as compared to visible light. In a simulation including a realistic SXR source, illuminator and sensor with shot noise and ideal parameter inference, we find 3σ <0.1nm static reproducibility for individual nanosheet CDs and 3σ <0.05nm for all layer heights (see Fig. 2). This is achievable due to the excellent decorrelation in the signal, visible in the correlation matrix in the right panel of Fig. 2. Note that here a diagonal matrix is ideal, and pale colors off diagonal indicate low correlation between parameters. In particular, the low correlation between the individual SiGe sheet CDs (top left 3x3 elements in the matrix) is very promising, as each of these dimensions separately is of interest, while many techniques can measure only the average. This matrix compares very favorably to metrology using visible wavelengths, where many elements would be expected to take on values much closer to ±1.

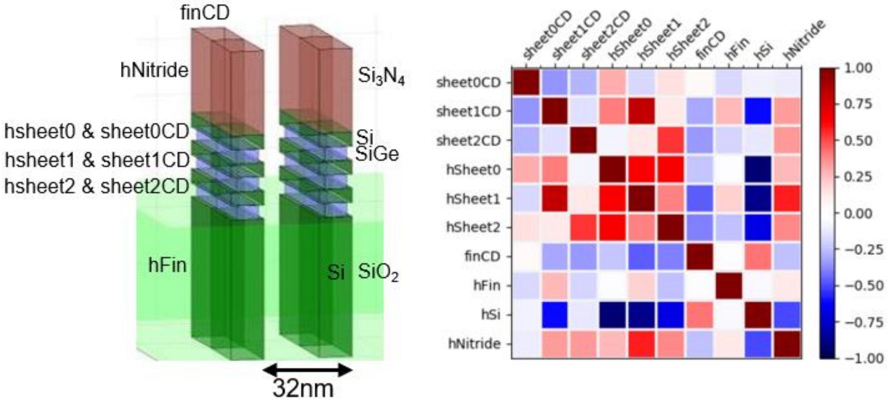

FIGURE 2. Simulated SXR performance on nanosheets, as shown in left panel. Right: Parameter correlation matrix showing good decorrelation between the nanosheet parameters.

In Figure 3, we show experimental results on our SXR testbench of 90nm pitch forksheet devices made by imec. We measured 9 fields: 3 coupons each from 3 wafers with different lateral recess etch times. TEM cross sections are shown for each wafer in panel (d) next to the measurements to which they correspond. We see in both simulation and experiment that there is a large enough difference in the measured first order diffraction efficiency between samples with different etch times to visually discriminate the different etch depths in the raw data (Fig. 3 b-c). Clustering can also be straightforwardly achieved using principal component analysis (PCA). Principal components are first calculated from only the non-sub-segmented targets from each wafer on one of the three measured coupons. Subsequently, all measurements are projected onto these components. Again, clustering is obvious by eye, and can also be achieved with 100% accuracy by applying k-means to the PCA output, yielding the coloring in Fig. 3d. It is promising that this method can generalize to the full set of measurements after being trained on only a subset. Notably, the difference in the signal is larger between wafers with different etch time than between fields or between micro-scale structure variation (i.e. sub-segmented vs. non-sub-segmented forksheets). We note that this is only a preliminary profile sensitivity experiment: With only 3 etch depths we cannot yet infer lateral recess etch depth, but this data in combination with our simulations suggests that we have excellent sensitivity to so.

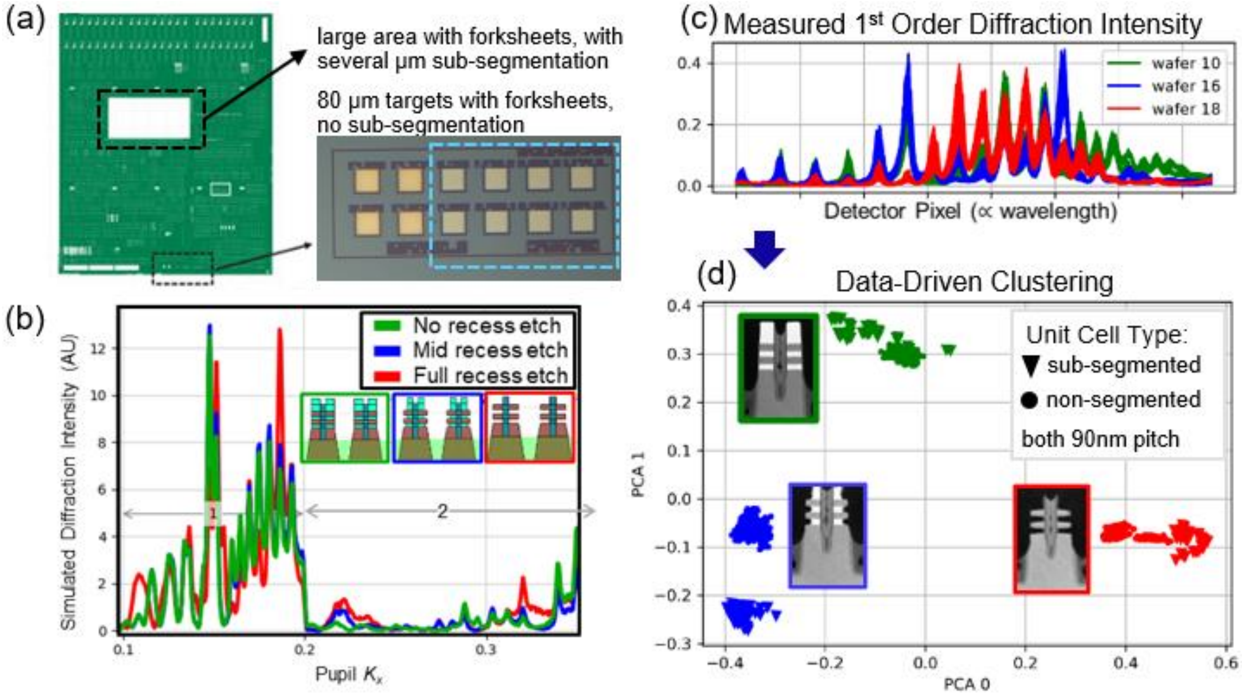

FIGURE 3. Experimental (c-d) and simulated (b) results of SXR scatterometry on forksheets. (a) Field layout, showing measured areas. All forksheets have 90nm pitch. (b) Simulated 1st and 2nd order diffraction intensity, with differences due to etch time visible by eye. (c) Measured 1st order diffraction efficiency, with all 1800 measurements overlaid including measurements on three neighboring fields from each wafer. (c) Natural clustering by etch time can be seen when principal component analysis is calculated from only the non-sub-segmented targets from a single field per wafer, then all measurements are projected on these components.

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KEYWORDS

Metrology, Scatterometry, EUV, OCD, Overlay, Profilometry

Extending Optical Critical Dimension Metrology into the Mid-Infrared Range

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INTRODUCTION

A significant component of the advancement in the capability of optical critical dimension (OCD) metrology to new semiconductor fabrication problems can be associated with the extension of the operating wavelength range of the hardware [1,2]. This growth has been largely accretive from the visible into the deep ultraviolet (DUV) and near infrared, 0.8-3 um, (NIR) and due to the introduction and refinement of laser driven light sources (LDLS) capable of integration into existing OCD systems [3]. Just as the LDLS was a boon to UV-visible-NIR OCD, new source and detector technologies as well as novel analysis algorithms have allowed expansion of the OCD method into the mid-infrared, 3-30 um, range (IRCD) [4-7].

Semiconductor metrology in the mid-infrared is not a new area. Fourier transform infrared spectrometers (FTIR), which are unpolarized mid-infrared reflectometers, are ubiquitous in semiconductor development. The fully automated wafer systems like the Element™ from Onto Innovation have a probe size between 1-5 mm (although smaller is possible) and are used for compositional analysis of blanket thin films deposited on silicon wafers or the wafers themselves through transmission or reflection measurements.

An FTIR instrument can be modified to create an ellipsometer by introducing polarization state generators at appropriate points in the optical system. There is a significant body of academic literature describing this configuration [8], and the Woollam IR-VASE® is a commercially available realization [9]. However, mid-infrared ellipsometers need not be based on an FTIR [10]. This alternative configuration has historically had a simple optical layout but low signal to noise ratio due to the weakness of the light source. The Aspect M1™ technology developed by Onto Innovation falls into this second category [7]. It uses an infrared high brightness light source (IR-HBLS) with an operating range of about 5 to 11 um and a monolithic cryogen-free detector. Wire grid polarizers are used in the system as well as one or more electro-optic or acousto-optic phase modulators. The currently available system has a probe size of <150 um, measurement time < 10 s, and a single phase modulator allowing operation in a psi-delta (M33-M34) mode, but a partial Mueller, 8 element, capability has been demonstrated with no change in probe size or measurement time.

RESULTS & DISCUSSION

IRCD offers a unique solution for the measurement of high aspect ratio structures found in 3D NAND memory devices [11]. Figure 1 contains three specific uses cases. The parameters of interest in Figure 1a describe the profile of the channel holes after they have been etched into the SiO_2/Si_3N_4 superlattice or ON tier stack, Figure 1b the profile of the holes etched into an amorphous carbon hard mask used for the etch in Figure 1a, and Figure 1c the recess of the Si_3N_4 after a further etch and clean following the etch in Figure 1a.

As shown in Figure 2, there is negligible absorption for any wavelength for SiO_2 and Si_3N_4 in the visible-NIR range; however, in the mid-infrared, there are regions of negligible and strong absorptions associated with the fundamental Si-O and Si-N bonds whose positions are well understood. Figure 3 is a finite difference time domain (FTTD) simulation of intensity of the electric field for a set of wavelengths in the mid-infrared range for 192 pair

ON tier stack with 100 nm CD holes illustrated in Figure 1a [6]. This figure demonstrates that light at some wavelengths completely penetrates the whole structure while others are strongly absorbed near the surface. This variation in optical absorption implies that different portions of the structure are sampled by different wavelengths enabling the extraction of the critical dimension of the holes as a function of depth. Figure 3 contains a finite number of absorption snapshots, but the absorption coefficient is continuous as would be the extracted profile. This variation in absorption is central to the differentiation in operating principle of IRCD.

Figure 4a shows typical etch profiles of a specific etch process at the center and edge of a 300 mm wafer [4]. The data has been extracted at specific depths based on customer requirement; however, the curve can be defined at arbitrary resolution in depth. Figure 4b shows the correlation of IRCD measured values plotted against a destructive reference for an etch process skew [4]. The data in this plot is grouped by channel hole diameter for a given depth. The correlation is better than Angstrom-level with typical CD values of 100 nm. Figure 5 is a typical measured profile of a channel hole etched in an amorphous carbon hardmask film, and the correlation of the bottom CD with a destructive reference [4]. The operating principle here is the same as in the channel hole etch application. The amorphous carbon films used as hardmasks in these process flows tend to be thick at >4 um and highly graphitic thus strongly absorbing. The longer absorption length afforded by operating in the mid-infrared makes these measurements possible.

The lateral silicon nitride recess in the channel hole occurs because of the etch bias between SiO_2 and Si_3N_4. Traditional OCD metrology operating in the visible-NIR range and even x-ray methods are unable to uniquely measure the recess relative to the channel hole due to correlation, however, IRCD can take advantage of the unique absorption peaks in the mid-infrared (Figure 2) to differentiate the channel hole surface from the recessed silicon nitride surface. Figure 6 shows the results of IRCD correlation to a destructive reference metrology along with DOE discrimination at the wafer-level with radial dependence plots [5].

CONCLUSION

Technological advances in light source and detector technologies have allowed for a true OCD solution in the MIR region that surpasses classical FTIR in terms of SNR. This coincides with an industry gap in 3D NAND, namely the characterization of high aspect ratio structures constructed in dielectrics. Traditional OCD metrology operating in the visible-NIR range are insensitive to HAR structure profile due to lack of optical contrast in dielectrics, but IRCD can take advantage of strong and unique dielectric absorption bands in MIR to measure the Z-profile of the channel hole, amorphous carbon hardmask and even the lateral silicon nitride recess in the channel hole.

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KEYWORDS

Optics, Metrology, Infrared, Ellipsometry, Scatterometry, Semiconductor

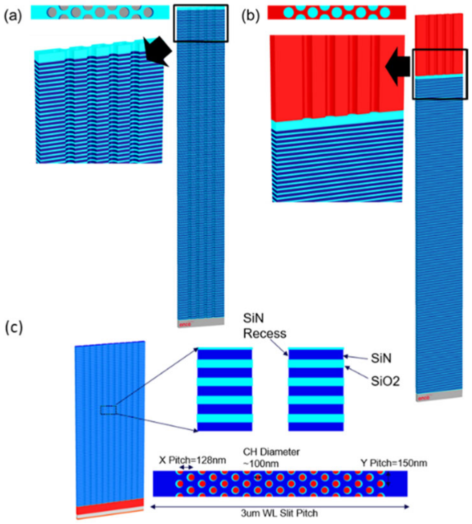

FIGURE 1. Representative structures under investigation for the (a) channel hole etch, (b) hardmask etch, and (c) Si_3N_4 recess applications in 3D NAND memory.

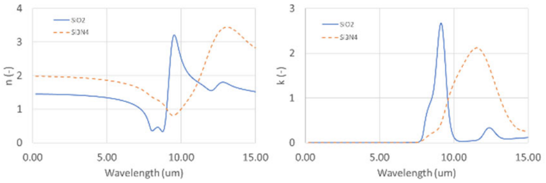

FIGURE 2. Representative optical dispersion curves for SiO_2 and Si_3N_4.

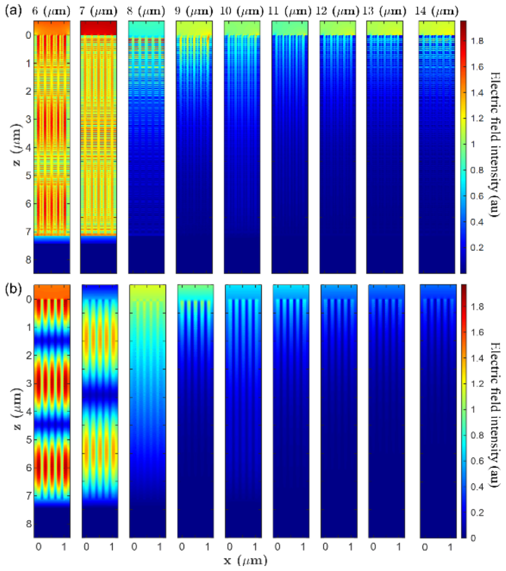

FIGURE 3. Electric field intensity for a representative channel hole structures as a function of optical wavelength for TM (a) and TE (b) polarization.

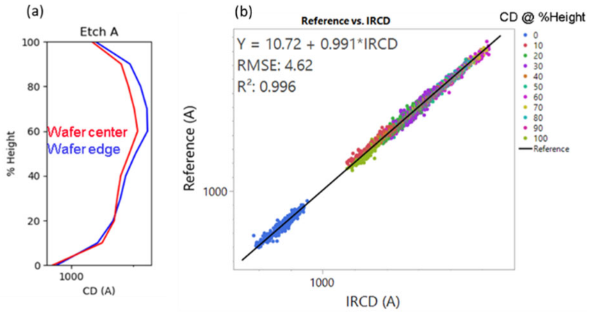

FIGURE 4. Channel hole CD correlation through the tier stack between IRCD and reference metrology for five different wafers each produced from a different etch recipe (a) example of the profile for one etch recipe and (b) colored by CD at various heights, where 0% indicates the bottom and 100% indicates the top.

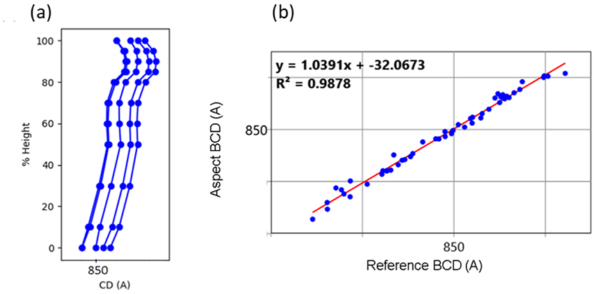

FIGURE 5. Examples of IRCD fitted amorphous carbon etch profiles (a) and BCD correlation between IRCD with reference metrology (b).

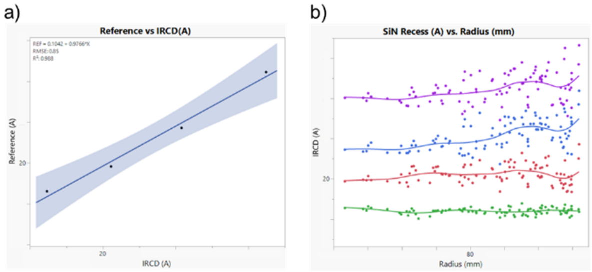

FIGURE 6. Si_3N_4 recess correlation between IRCD and reference metrology for four different wafers (a) and radial dependence of Si_3N_4 recess for all DOE wafers (b).

Ebeam Technology for CD and Overlay Addresses 2D Scaling Challenges and 3D Edge Placement Errors

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INTRODUCTION

To continue the 2D scaling roadmap, we need to ensure three things. First, we need to make sure the intended patterns on the EUV photomask are precisely replicated on the photoresist, with proper features, centering and uniformity across the entire wafer. We perform after-development inspection -- or ADI -- to find serious errors before etching the wafer. Second, we need to make sure the patterns we etch into the wafer are just as uniform. We use after etch inspection -- or AEI -- looking for very high correlation between the ADI and AEI measurements. Any inconsistencies introduce irregularities that can propagate as we continue to process the wafer. Third, we need to align the edges of the critical features on each layer of the chip with their opposite features on the layers above and below. Edge placement errors can ruin entire wafers, or they can crop up in particular areas and negatively impact chip yield, power and performance. This talk will demonstrate how 3D eBeam technologies are deployed in each of these three areas.

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THIN EUV RESIST CD CONTROL

Let’s begin with after-development inspection or ADI. Tthe EUV photoresist is much thinner than DUV resists. If we used conventional eBeam systems and energies to look for stochastic defects and measure the critical dimensions and overlay, we could distort the patterns on the delicate resist. To help chipmakers inspect more during ADI, The Industry needs lower energy to minimize interaction with the resist. And we provide a unique technology that improves EUV pattern image resolution, giving us sharp dark and light contrasts at low energy. Chipmakers are already using this technology to ensure CD uniformity at emerging EUV nodes, and to center the mean of pattern variation across the wafer prior to etching.

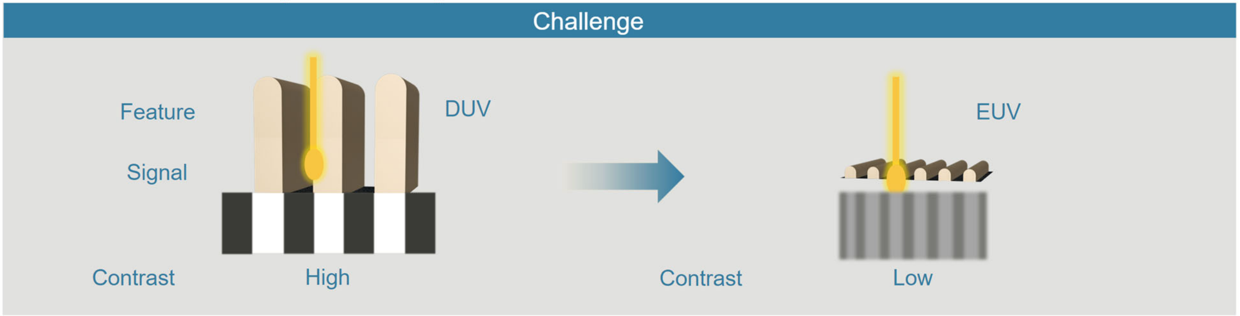

FIGURE 1. EUV ADI Needs Lower eBeam Energy, Higher Pattern Resolution.

2D PATTERN FIDELITY, FROM DEVELOPMENT TO ETCH

In easier times, if engineers properly centered the photoresist pattern over the wafer, they could usually count on good etch results as well. EUV patterning introduces a number of intermediate steps. The photoresist pattern is etched into a transfer layer, then the transfer layer pattern is etched into a hardmask, and finally the hardmask pattern is etched into the wafer. Each of these intermediate steps is a potential source of variation that can reduce pattern fidelity on the wafer. And this can cause serious ADI to AEI correlation issues. To help with EUV scaling, engineers are now adding metrology steps using our PROVision eBeam metrology system which is 10 times faster than SEM metrology. PROVision can generate data for each of these intermediate steps, giving process engineers bias signature data that they can use to holistically center the entire patterning flow. Engineers can quickly improve ADI-to-AEI correlation, identifying and correcting the issues before they result in scrapped wafers. This data can also be used with our AIx platform, creating feedback loops that can help customers tune their process technologies.

EDGE PLACEMENT

Prior to EUV, edge placement was much easier. Features were larger, and if we aligned the optical scribe lines in the resist with the corresponding optical targets on the wafer, we could predict that the edges of the new features would be properly aligned with their opposite features on the previous layer. We could proceed one 2D layer at a time and make optical corrections along the way, producing uniform features from top to bottom. It’s actually amazing that optical techniques have worked for so long. The optical proxy targets are at least 10 times larger than the features we are creating with EUV. Also, iterative process steps like multipatterning introduce variations, and 3D designs create stresses and interlayer distortions. Optical metrology and target-based approximation struggle to detect and diagnose these issues. As we continue to scale with EUV, engineers are encountering more situations where they are using all of the optical techniques properly and still having edge placement errors. They are hitting blind spots that bring scaling to a halt. Today, most equipment manufacturers agree that we need to use eBeam metrology to complement optical metrology. But many of their efforts are still focused on diagnosing patterning failures one layer at a time and using the eBeam data to make optical corrections rather than solve the underlying process issues.

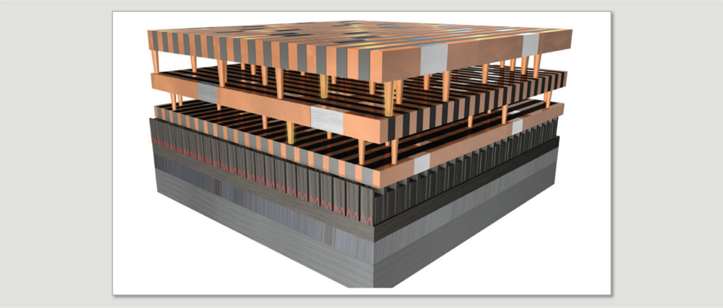

FIGURE 2. 3D Metrology needed to overcome stochastic errors and process variability

3D patterning control

Applied Materials is driving a different approach we call 3D patterning control. The approach is designed to overcome the blind spots by measuring and addressing all of the sources of edge placement error. The new 3D patterning control playbook has three elements. One, we supplement optical target approximation of patterns with actual, on device metrology using eBeam. Two, we supplement statistical sampling of a small number of locations with massive across-wafer metrology. And three, we go beyond 2D, one-layer at a time approaches to a 3D integrative approach that measures and addresses all of the critical layers as an integrated system.

Applied's PROVision eBeam is specially designed for 3D patterning control. We use higher eBeam landing energies to penetrate the many layers of an advanced chip. Using our Elluminator technology [1],

we capture the back-scattered electrons and produce high-contrast images of the many interdependent features. The clear, resulting images allow engineers to see and measure edge placement through all of the critical layers at the same time. PROVision measures all of the sources of edge placement errors, including overlay, CD uniformity, and line width roughness. It also gives engineers the data they need to refine process recipes for a wide range of equipment -- from litho to etch, deposition, anneals and CMP.

3D pattering control can be used at different times for different purposes. In early R&D, there are cases where eBeam metrology is the only way to develop a new process with correct edge placement. Later, eBeam data can help in the transition from R&D to tool matching and high-volume ramp. While customers will continue to use optical methods to keep their processes in spec during high-volume production, eBeam can help in quickly diagnosing and solving yield issues in HVM. If a manufacturer's optical control scheme has an excursion, it can take weeks to produce new masks with new proxy targets. Using actual, on-device measurement with eBeam, customers can continue to process wafers in the meantime.

Finally, Chipmakers have collaborated with us to publish papers, Showing how the new patterning control playbook can be used to achieve higher yields, faster. In Reference [2], Samsung and Applied demonstrated the use of eBeam SEM overlay and CD uniformity techniques to improve 3D edge placement and yield in logic devices. In reference [3] Hynix and Applied demonstrated similar edge placement and yield improvements in DRAM. In Reference [4], IBM and Applied presented a paper on the new VeritySEM technology for EUV photoresist metrology. In Reference [5] IMEC and Applied show how PROVision can be used to control the Silicon Germanium recess step, which helps speed Gate All Around and ForkSheet FET process development.

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KEYWORDS

CD, Patterning Control, Pattern Fidelity, Overlay, Edge Placement Error, EPE

Fast and High-resolution Micro-XCT and Nano-XCT Imaging of Advanced Packaging Structures Using New X-ray Sources

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INTRODUCTION

The talk will discuss the different ways to achieve high resolution imaging, and especially 3D imaging using computed tomography, of advanced packaging structures and how new X-ray sources can significantly improve the performance of such imaging. The talk will highlight how different source characteristics are optimal for the different methods of imaging and what the main figures of merits of the sources are.

HIGH RESOLUTION IMAGING – WHAT'S NEEDED FROM THE SOURCE

High resolution X-ray imaging can be achieved in three main ways. The first two are "shadow puppet" style where either an X-ray spot of roughly the same radius as the sought resolution is used in magnification mode, where the detector can have relatively large pixels if sufficiently far away from the sample as illustrated in Figure 1a, or the resolution is achieved by having a detector with pixels of similar size as the sought resolution close to the sample, where the source then can be larger if it is sufficiently far away from the sample as in Figure 1b.

(a) (b)

FIGURE 1. The two conventional ways to achieve high resolution X-ray imaging by (a) geometrical magnification allowing for use of a low-resolution detector or (b) no magnification imaging requiring a high-resolution detector.

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The final way to achieve high resolution is using an X-ray optic, such as, e.g., a Fresnel zone plate, as objective as in Figure 2.

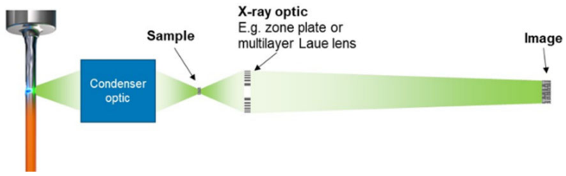

FIGURE 2. High resolution imaging through the use of an X-ray optics objective.

All techniques have in common that they benefit from using the brightest possible X-ray source with an appropriate spot-size within the applicable range for the specific case. But in a practical situation, high brightness is not all you need from a source. It also must have high stability, low maintenance and a form factor that enables the application at hand.

NEW X-RAY SOURCES

The by far most used X-ray sources in the world and the only sources that can be easily integrated into inspection and metrology equipment are based on the principle of bombarding a metal target with high energy electrons. Such sources are commonly referred to as X-ray tubes since their simplest design is a form of vacuum tube. Most X-ray tubes on the market today look very much like the original Coolidge hot cathode tube from 1913 as shown in the timeline of Figure 3. One breakthrough came in 1929 with the introduction of the rotating anode allowing for higher power operation thanks to the distribution of the e-beam energy over a ring on the rotating anode rather than just a point on the stationary anode. Both X-ray tube types have been refined over the years through the hard work of very many engineers and scientists, but no major anode-technology breakthrough came until the liquid-metal-jet anode technology was invented in 1999 [1]. By using a high-speed jet of liquid metal, instead of the traditional solid- or rotating anode, it has been demonstrated that a much higher power density can be applied to the anode. The MetalJet technology achieves at least 10x higher X-ray brightness than conventional microfocus X-ray sources. However, since it is a so-called reflection type X-ray source, the MetalJet sources can typically not reach X-ray spot sizes below 5 µm and thereby not realize better resolution than a few micrometers in the magnification imaging mode mentioned above. For higher resolution one must use so called transmission X-ray tubes where the Excillum NanoTube N3, based on refined electron optics etc. from the MetalJet platform, can reach down-to 150 nm resolution.

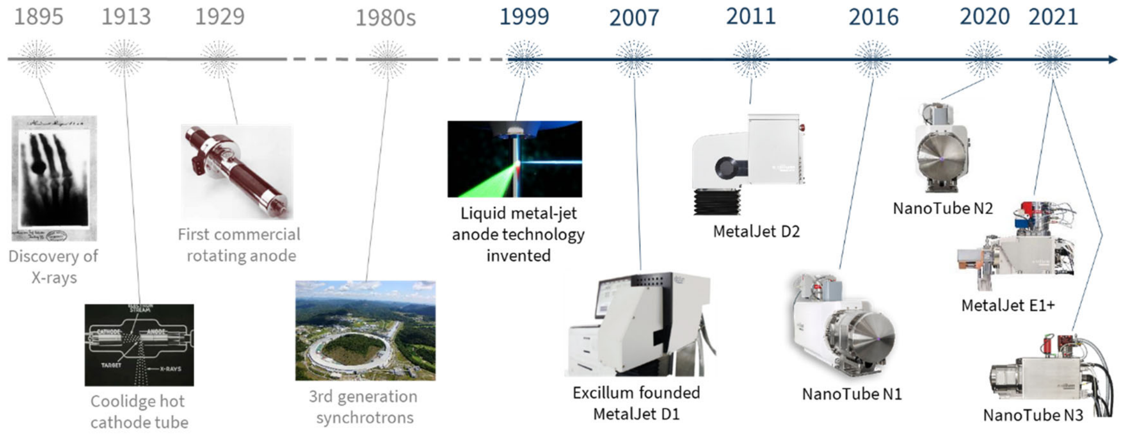

FIGURE 3. A very overview X-ray history timeline with some major X-ray tube developments, especially the different anode types, and release dates of the Excillum products that will mainly be referred to for imaging examples in the talk.

IMAGE EXAMPLES

The talk will show how the new sources drive performance of imaging of advanced packaging structures using the three different imaging modes described above. Several examples will be shown like, e.g., the extreme resolution CT dataset from Müller et. al. [2] in Figure 4 of a commercial micro-SD card imaged with an Excillum NanoTube N2 X-ray source.

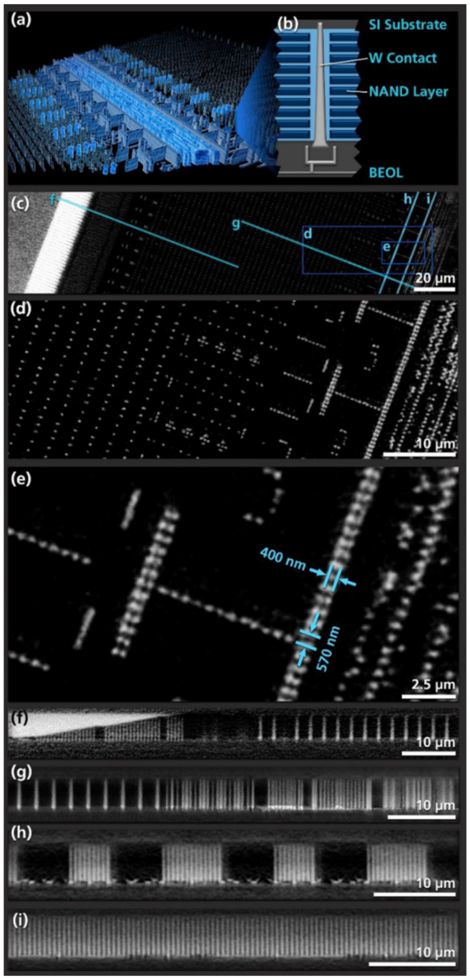

FIGURE 4. Example from Müller et. al [2]: Reconstructed nano CT scan of a semiconductor memory chip from a commercial micro sd card (SanDisk 32 GB microSDHC UHS-I) measured with a sampling of 98 nm. (a) a 3D rendering of the internal metallized structures, where the individual contacts with an expected size between 100 - 200 nm can be clearly identified. (b) schematic of a single contact pillar connecting the multiple wordlines. (c) volume cross-section from the reconstruction with memory array in the center and a section of the peripheral circuits to the right. (d) - (e) enlarged details of the sectional view with dimensions for specific features, (f) – (i) vertical sections through the volume corresponding to the markings in (c). (f) wordline staircase at the edge of the chip. (h) – (i) vertical view of the peripheral circuits

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KEYWORDS

Microfocus, Nanofocus, X-ray, Computed Tomography, Advanced packaging

In-situ Micro-DCB / Nano-XCT Test to Ensure the Robustness of Leading-edge Cu/ULK BEOL Stacks

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[a] Now with Robert Bosch Semiconductor Manufacturing Dresden GmbH

INTRODUCTION

Mechanical failure caused by microcracks that were introduced into a microchip during the manufacturing process, e.g. during dicing of a semiconductor wafer, are a serious reliability concern for microelectronic products [1]. The risk of microcrack growth and eventually fracture in BEoL stacks has been increased since the introduction of low-k and ULK materials – with low dielectric permittivity but also low Young's modulus and cohesive strength, and consequently low fracture toughness - to insulate the on-chip metal interconnects. For the understanding of fracture mechanics at small scales, a specially designed experimental setup is needed to grow microcracks in patterned Cu/low-k and Cu/ULK structures by applying a precisely controlled mechanical load and by monitoring force and displacements in materials at the micro- and nanoscale. A miniaturized mechanical test for 3D-structured systems and materials - a micro double cantilever beam (micro-DCB) test in a laboratory X-ray microscope - provides a unique capability for high-resolution 3D imaging of microcrack evolution while a force is applied [2].

Since in-situ 3D imaging of microcracks and crack propagation kinetics requires a non-destructive technique with high spatial resolution, nano X-ray computed tomography (nano-XCT) is the technique of choice. X-ray imaging is characterized by a sample thickness / resolution value of ~ 10^3, (see Fig. 1), however, conventional micro-XCT does not provide the resolution needed. Electron tomography in the TEM requires small samples in the ~ 100 nm range.

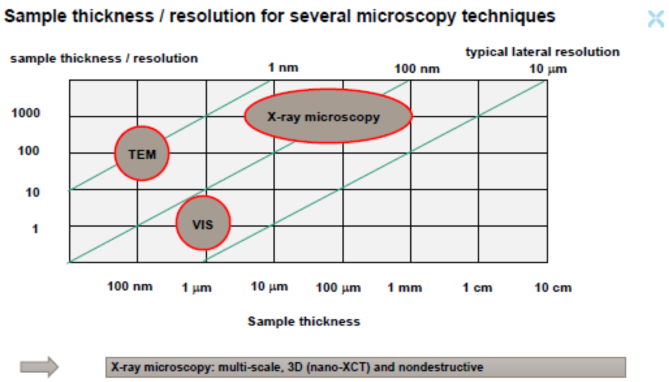
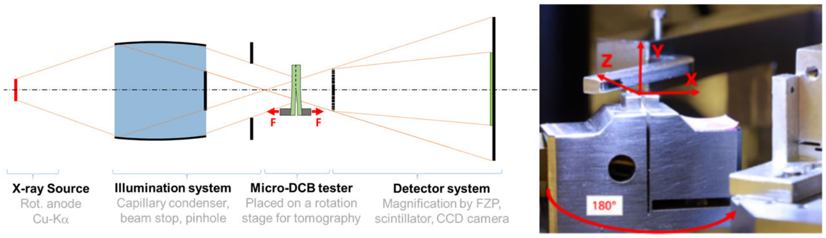


FIGURE 1. Sample thickness / resolution for X-ray microscopy, visual light microscopy and TEM.

The requirement to a mechanically robust on-chip interconnect stack against wafer processing and packaging stress requires that the fracture driving force for pre-existing defects – e.g. microcracks – is smaller than the fracture resistance of the BEoL stack [3]. As a preventive measure to avoid fracture and mechanical chip damage, metallic guard ring (GR) structures that are mechanically robust against local mechanical stress are designed and integrated at the rim of microchips manufactured in leading-edge CMOS technology nodes [3]. Another option to dissipate energy is to steer the microcrack into regions of the BEoL stack with relatively high fracture toughness, with the consequence that the crack propagation is slowed down and eventually stopped [4]. In this study, we present an experimental approach that allows to steer the microcrack in a controlled way by tuning the fracture mode mixity locally at the crack tip and to acquire simultaneously the 3D image information of a region of interest (ROI) that includes the on-chip interconnect stack of an advanced microchip. We discuss the influence of materials properties at micro- and nanoscale and special stress states, with the goal to describe a way to steer the microcrack into a region with relatively high fracture toughness.

MATERIALS AND METHODS

In this study, a miniaturized piezo-driven DCB test positioned in the beam path of a commercial laboratory X-ray transmission microscopy (TXM) tool (Xradia nano-XCT) is used to force a displacement-controlled crack propagation through the BEoL stack of a microchip and at the same time to image the pathways of microcracks in BEoL stacks with sub-100nm resolution [5. For X-ray microscopy at a photon energy of 8 keV (Cu-Kα radiation), the sample size has to be < 100 µm, at least in one direction parallel to the crack front, to enable the transmission of photons [6]. The scheme of the X-ray microscope and the integrated micro-DCB test are shown in Fig. 2.



a

b

FIGURE 2. a) Scheme of the micro-DCB test inside nano-XCT, b) micro-DCB test setup inside the X-ray microscope: Z axis: X-ray beam direction, Y axis: rotation axis of the sample (there fixed on sample holder), X axis: direction of applied load [5].

Sandwich-like micro-DCB samples were prepared in such a way that two beams, the sample of interest and a "dummy" sample, are glued together, with a thin layer of epoxy and the layer stack to be studied (ROI) in the center. A piece of a thinned wafer, containing on top of the silicon the ROI with the BEoL stack, and also a part of scribe line (SL) and guard rings (GRs), was glued to a dummy sample (silicon) of similar dimensions in length and width, but with varying heights. The integrated circuit was manufactured in an advanced CMOS technology node, with a BEoL stack consisting of 12 layers of copper (M1 to M12) with different dimensions, insulated by ULK materials [6], and a post passivation layer on top. The samples were grinded, polished and sawed up to a length of 1 mm and a cross-section of approximately 50 µm x 50 µm, to fulfil the geometrical requirements for a micro-DCB test in a TXM [2,6]. The micro-DCB test samples design includes: (i) "symmetric sample", there are both beams had the same target heights $e = h_1/h_2$ dummy beam (h_1) and chip beam (h_2) is supposed to be $e = 1$; (ii) "asymmetric sample" with dummy to chip beam ratios $e = h_1/h_2$ were 2.0 and 0.5, respectively. The resulting real beam thickness ratios e were calculated from 3D tomography data of the ROI.

RESULTS

The microcrack is either propagating along one level of the BEoL stack, and then moving to a higher level or to a lower level, depending on the mode mixity, or – even more often – the crack front is running in several levels simultaneously. Fig. 3 shows virtual cross-sections through pieces of wafers at the final loading stage of a micro-DCB test, visualizing the microcrack in SL, GR and Cu/ULK BEoL stack, for a mode mixity of $e \sim 2.5$. In this particular case the microcrack is steered from M6 to M4.

The micro-DCB experiment in an X-ray microscope allows to control fracture and to steer crack paths to regions in the BEoL stack with relatively high fracture toughness. The achieved results for different geometries show that steering of the crack path to higher metallization levels, as characteristic for beam thickness rations $e < 1.0$, is the preferred option since the fracture resistance or the critical energy release rate for crack propagation is increased the closer the microcrack will be to M12 (Cu metallization thickness ~ 2 µm). The energy dissipation process that results in the increase of the energy release rate close to thick Cu lines can be explained with the size-dependent plasticity of copper. For Cu structures with a dimension > 1 µm, the dislocation confinement is relaxed, and the plasticity zone is enlarged when the microcrack is approaching the Cu structure, thus dissipating more mechanical energy. Therefore, considering Cu structures with dimensions of 2 µm in the BEoL stack, the crack propagation is expected to be slowed down, and in the best case the microcrack will be stopped. Since the plastic zone size exceeds the Cu layer thickness, this effect occurs also in the dielectrics next to the Cu structure [7].

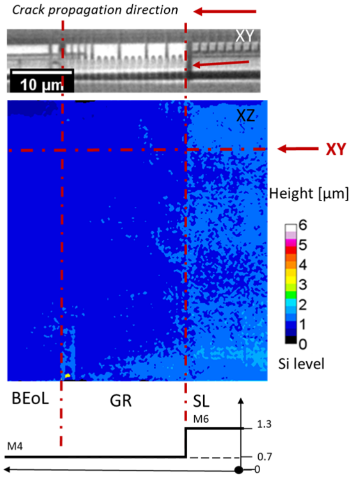


FIGURE 3. Virtual cross-section (XY view) with indicated crack path changes (top); XZ height map of the crack in the Cu/dielectrics stack (SL, GR, BEoL), heights above the Si substrate indicated by colors (middle); Scheme of the cross-section XY at the indicated z location (red line) with crack pathway, showing crack path changes from M6 to M4, heights above the Si substrate in µm (bottom).

The combination of micromechanical testing and high-resolution X-ray imaging opens the way for the development of design concepts for novel engineered materials systems based on their local mechanical properties. Nano X-ray computed tomography (nano-XCT) is the technique of choice to image microcracks in 3D-patterned microchips with sub-100nm resolution and to draw conclusions for their mechanical robustness. A micro double-cantilever beam (micro-DCB) test setup is used to demonstrate the capability to steer microcracks into toughened regions of microchips. The demonstrated approach to steer microcracks into toughened regions of a microchip has significant implications for the design of on-chip interconnects (including guard-ring structures) of leading-edge integrated circuits and for the fundamental understanding of the fracture behavior of materials.

ACKNOWLEDGMENTS

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KEYWORDS

X-ray microscopy, XCT, crack propagation, interconnect stack, fracture toughness

High Throughput (<Minutes) Sub-Micron 3D X-ray For Failure Analysis & Wafer Level Packaging

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INTRODUCTION

The development of advanced packaging architectures are an area of strategic importance for the industry. Packaging is now widely recognized as complementing front end development in delivering on Moore's scaling law for improved functionality. Heterogeneous Integration (HI) has attracted significant interest because it offers the ability to mix and match chiplets from diverse nodes, overcome reticle size limitations and co-locate logic with high-bandwidth memory.

The key driver for physical attributes in System-in-Packages (SiPs) is achieving a bandwidth doubling for each successive generation of device. Bandwidth increases are typically achieved with increased interconnect density, which places stringent limits on the linear and areal interconnect density. This in turn constrains bump pitches and line widths. The HI roadmap calls for bumps with less than 10 micron pitch and 250 nm line widths within five years [1]. The continuing miniaturization of bumps and line widths demand metrology and failure analysis tools with higher spatial resolution than ever before and a roadmap for continued increases over the next decade. Moreover, modern device architecture is predominantly three-dimensional in nature because a 3D architecture offers the shortest connection path between dies which minimizes capacitance for maximum bandwidth.

3D X-ray is widely regarded as a workhorse solution for non-destructive failure analysis of 3D structures. However, the growth of HI and wafer-level packaging have prompted urgent demand for 3D X-ray on larger packages and on wafers, for which even the leading 3D X-ray systems struggle. These large samples also suffer from high dose and beam hardening artifacts in conventional 3D X-ray approaches.

Conventional 3D X-ray is not well suited to wafers and packages for two reasons. First, the throughput is inversely proportional to the square of the package size meaning large packages take far longer to image. Samples up to 10 mm work well but at larger sizes, throughput times exponentially increase and even data with limited image quality may require tens of hours to collect. Second, beam hardening causes significant artifacts in the reconstruction making interpretation of critical defects such as silicon cracks around metal features extremely difficult, if not impossible. In this case, beam hardening artifacts can only be reduced with higher kVp at the cost of significantly reduced contrast and consequently longer exposure times. The net effect of these problems is that most practitioners conclude that 3D X-ray is impractical for samples much larger than half an inch diameter.

Here we present a novel 3D X-ray approach (Sigray Apex XCT) that offers sub-micron resolution (0.5 μm) and throughput times of <15 minutes on large samples, even on samples up to 300 mm in diameter. A patent-pending geometry allows Apex XCT to decouple spatial resolution from sample size, and it can achieve spatial resolutions of 500 nm anywhere (center, edges, etc.) on a large, intact sample. 3D measurements for process control and yield management of wafer level packaging have been demonstrated at throughput times of 15 seconds. Due to the innovative design, beam hardening is negligible, enabling the virtual delayering of packages and wafers with sharp clarity. The performance (spatial resolution, sample size, and image quality) of Apex allows it to address every generation of the bump pitch called in the five year plan of the heterogeneous integration roadmap [1].

We will describe two versions of our Apex tool, each designed separately to address the specific needs of the failure analysis and fab process control markets. The Apex-150 XCT is a lab scale tool capable of handling samples up to 225 mm in diameter with an integrated sample handling robot for unsupervised operation. A fully automated version of the tool, the Apex WaferCT, is designed for semiconductor backend fab process control and yield management and features a two port EFEM to accommodate standard 300 wafer FOUPs, GEM300 compliance and AMH compatibility. Both versions of the tool offer sophisticated defect detection using statistical, image processing and machine learning techniques.

X-ray dose is often an important consideration for backend inspection especially for high bandwidth memory. The Apex utilizes a patented WaferShield™ technology to mitigate potential damage from ionizing radiation. Combined with the extremely rapid data acquisition and highly efficient detection system the Apex is able to offer the highest 3D spatial resolution at the lowest achievable X-ray dose.

EXAMPLE 1 - IMAGING INTACT GPU IN 30 MINUTES

To illustrate the potential of Apex-150 XCT an intact GeForce 1070 was imaged to reveal defects in the interconnect layers. A relatively coarse scan at 8.6 μm was selected to give an overview of the region of interest in about 30 minutes. Failure analysis on a device this size using conventional CT would typically take tens of hours and be riddled with artifacts. The volumetric reconstruction shown here is remarkable for the lack of streaking artifacts which means each bump can be segmented and quantified.

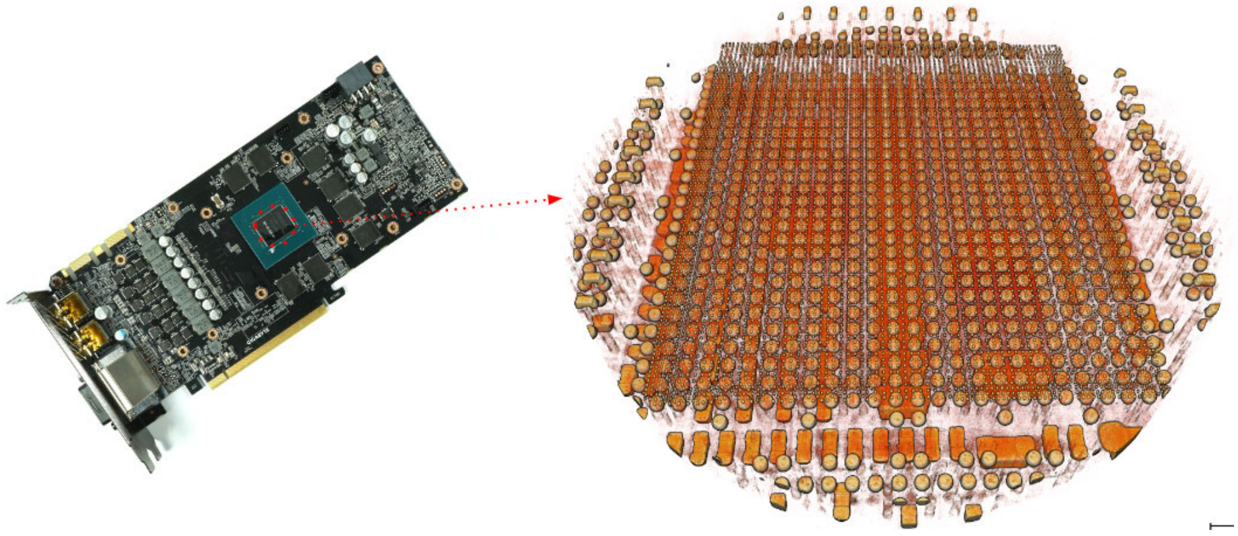

FIGURE 1. An GeForce 1070 GPU imaged in the Apex-150 XCT. Parameters used: 160 kVp, 1201 projections 8.6 μm voxel size, 34 minutes data collection. The reconstructed 3D volume reveals the many interconnect layers of differing pitch and material composition as well as their defects.

EXAMPLE 2 - INSPECTION OF COLD JOINTS FOR WAFER LEVEL PACKAGING

The Apex WaferCT was used to detect cold joints on a 300 mm wafer. In this case the image quality was optimized to achieve the highest throughput while maintaining the ability to detect the characteristic defect shape of the cold joint. The WaferCT works just as well for rapid screening and quantification of defects during process development and then for detailed high resolution investigation of individual defects where that becomes necessary.

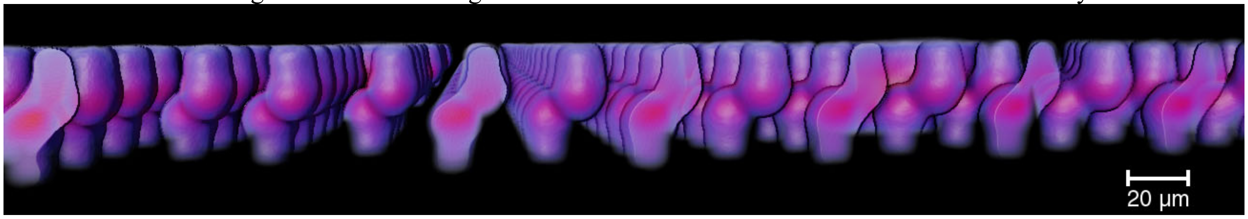

FIGURE 2. Illustrating cold joint defects in a die-to-wafer bonding on a 300 mm wafer . The data was collected with 70 kVp, 1201 projections, 0.3 μm voxels and 3 minutes total data collection time.

CONCLUSION

Apex is a patent-pending novel 3D X-ray approach offering the highest resolution and up to orders of magnitude improvement in throughput. The system has been productized to address two key applications: failure analysis and inline process control

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KEYWORDS

Failure analysis, wafer level packaging, metrology, heterogeneous integration, X-ray, 3D

Raman Spectroscopy For Nanoscale Materials Characterization And Metrology

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INTRODUCTION

In semiconductor manufacturing, Raman spectroscopy is an attractive characterization technique for e.g. mechanical stress and composition, thanks to its versatility, high throughput and non-destructive character, but as an optical spectroscopic method it is inherently diffraction-limited. In order to re-enable the strengths of Raman spectroscopy at the nanometer scale, we exploit polarization-induced enhancement effects and extend the application domain of Raman analysis into dimensional metrology.

NANOFOCUSED RAMAN SCATTERING

In a standard micro-Raman spectroscopic arrangement, the excitation light is focused onto the sample using a microscope objective which limits the spatial resolution to dimensions of the order of the (usually visible) wavelength. Moreover, the penetration depth of the light is typically of the same order, meaning that the total probed volume is very large compared to modern transistor dimensions. However, when aligning the linear polarization of the excitation laser with the structure geometry, the description of the coupling of the light into the structures is dramatically different from that of bulk material. The grating-like structure acts as a photonic crystal which leads to confinement of the available modes for transmission into the material of interest under the right experimental conditions [1]. As a result, the Raman spectrum becomes dominated by the response of just a tiny fraction of the total probed volume, and the Raman scattering originating from the material under study becomes strong enough to enable detailed analysis. As such, characterization of for instance mechanical stress and composition become possible on structures with dimensions far beyond the diffraction limit [2].

RAMAN SPECTROSCOPY WITH DIMENSIONAL SENSITIVITY

With the electric field confined to the small nanostructures under investigation, the penetration depth of the light is still much larger than the typical thickness of the device channels, meaning that the totality of the channel volume is probed, and the intensity of the collected Raman scattering scales with that total volume. Therefore, when normalizing the signal from such channels to another reference signal in the spectrum (like Si-Si scattering from the substrate) we obtain a volumetric measurement of the amount of material present in the probed volume. This opens a completely new application domain for Raman spectroscopy as a dimensional measurement as we will demonstrate in a couple of examples.

First, in nanosheet and forksheet FETs [3] a metrology challenge emerges as the SiGe in the Si/SiGe stack [see inset of Fig. (1) panel (a)] is etched selectively from the sides, revealing the Si transistor channel for further processing. The depth of that cavity is an important parameter to control, but is virtually inaccessible using the standard characterization techniques for profilometric measurements like OCD or AFM. We use the Raman scattering coming from the SiGe layer and normalize that to the Si-Si scattering that is collected from the Si layers in between the SiGe and the Si substrate combined, both of which material volumes remain unchanged. When carrying out this analysis on a variety of etch depths we can see from panel (a) in Fig. (1) that the normalized integrated intensity of the Raman signal decreases uniformly as the cavity depth increases. Moreover, the sensitivity of this parameter equals that of a true volumetric measurement, as the trend follows the ratio of the normalized remaining volume of SiGe (V/V_0, blue dashed line in the plot).

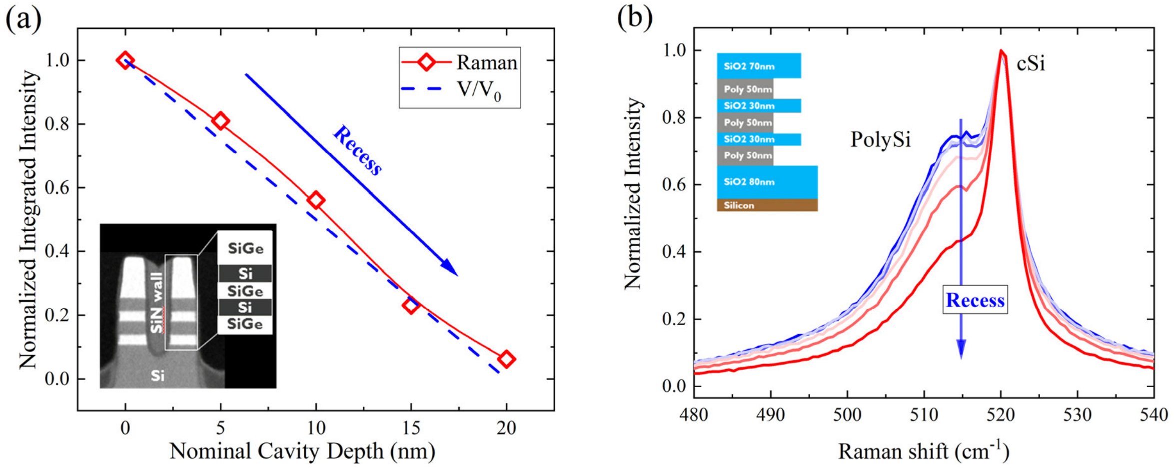

FIGURE 1. (a) Normalized integrated Si-Ge scattering intensity from a forksheet structure as a function of nominal cavity depth as it is etched into the SiGe. The dashed line represents the ratio of the remaining over initial volume of material, while the line through the datapoints is a guide to the eye. The inset shows a forksheet FET structure with the stacked Si and SiGe layers, where the SiGe is etched selectively from the sides. (b) Normalized Raman spectra for a stack of Si/polySi memory structures with a DOE of increasing etch rate from center to edge of the wafer sample, corresponding to the downward arrow in the plot. The inset shows the material stack under investigation.

Second, an example from 3D memory technology demonstrates that this method works as long as the Raman signals from the material of interest can be distinguished from the background, as is the case for PolySi in e.g. 3DNAND stacks. Here, we rely on the slight offset of Si-Si scattering in PolySi with respect to that of crystalline Si (cSi) to measure the etch depth of the cavity that originates as the PolySi is etched between the SiO_2 in the stack [see inset of Fig (1) panel (b)]. Similarly as with the SiGe etch, we have a DOE where the cavity depth progresses in the sample set, and it can be seen in panel (a) of Fig (1) that when we normalize the spectra to the Si background from the substrate, the characteristic PolySi signal at slightly lower wavenumber decreases significantly. The ratio of this intensity to the Si background can be used as a quantitative measure of the remaining volume of PolySi and hence of the depth of the cavity. It was indeed confirmed by TEM measurements that there is a 1-on-1 relationship between the normalized PolySi Raman intensity and the depth of the etched cavity.

In summary, these examples show that Raman spectroscopy has the potential to provide dimensional metrology on industry-relevant structures, which in combination with the extensive set of applications for the technique re-enabled at the nanometer scale, make it an essential toolkit in semiconductor manufacturing environments.

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KEYWORDS

Raman Spectroscopy, CD Metrology, Etch Depth

Measurement Challenges for Scaling Superconductor-based Quantum Computers

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INTRODUCTION

Global investment in the research and development of quantum information systems by industry, government, and academic institutions continues to accelerate and is expected to reach over \$16B by 2027 [1]. Systems based on optical photons, atoms or ions, spins in semiconductors, and superconductor circuits are all being pursued. One of the most challenging technology hurdles for all these paradigms is scaling to the large number of qubits required to make a quantum computer (QC) capable of solving relevant problems that cannot be efficiently solved using a conventional computer. In the case of a QC using superconducting qubits with state-of-the-art gate error rates, it is estimated that greater than 1 million physical qubits will be required [2].

Scaling superconductor-based QCs to this size from the present ~ 10^2 qubits [3] will require designing, implementing, and testing large, cryogenic microwave systems for initialization, control of gate/entanglement operations, and readout of ~10^6 physical qubits using millions of low-power microwave signals. The goal of the NIST research highlighted below is to assist the nascent QC industry with making significant advances in 1) cryogenic microwave reference sources, 2) on-wafer microwave testing, and 3) on-wafer calibration standards that will be required for fabrication process control, design verification, and accurate modeling and simulation in the development of large-scale QCs.

Fabricated lithographically on silicon or sapphire wafers, superconductor-based "transmon" qubits consist of simple, cryogenic, non-linear *L-C* resonator circuits using superconducting tunnel junctions called Josephson junctions (JJs) to provide the nonlinear inductance (L). The resonators have a ground state (0) to first-excited state (1) energy separation E_{10} with a transition frequency $f_{10} = E_{10}/h$, where h is the Planck constant, typically in the 4 GHz - 8 GHz range. Because of the nonlinearity, the higher energy state separations (E_{21}, E_{32}, etc.) decrease, allowing the E_{10} transition to be isolated as a two-level system (TLS), i.e., a qubit. The qubit is cooled to the "quantum regime" in a dilution refrigerator (DR) to a temperature $T < 0.05$ K so that the thermal energy $k_BT << E_{10}$, where k_B is the Boltzmann constant. Low-power (~ -90 dBm =1 pW, as measured at the qubit) modulated microwave control signals are used to 1) initialize ("write") the qubit state, e.g., excite the qubit from the ground state to the first-exited state, and 2) perform gate operations, i.e., control the evolution of the qubit state and interactions with other qubits.

Readout of the qubit is a delicate measurement designed to interrogate but not upset the fragile quantum state. To do so, the qubit can be capacitively-coupled to a low-loss (high quality-factor) superconducting linear resonator with a resonant frequency f_r, typically chosen to be a few GHz higher than f_{10} (dispersively-coupled regime). Extremely low power (< -120 dBm = 1 fW) microwave signals are used to monitor f_r, which shifts depending on the qubit state. In multi-qubit systems fabricated on a single chip, each qubit is coupled to a different linear resonator with a unique f_r. Many resonators can be coupled to a single transmission line, allowing frequency-multiplexed readout [4]. Because the readout signals are so small, extremely sensitive, low-noise, cryogenic parametric amplifiers are located near the qubits and used as the first amplifier stage of the output chain; these "quantum-limited amplifiers," developed at NIST [5,6] and elsewhere, add only the minimum amount of noise dictated by quantum mechanics.

The microwave circuits and the modulated microwave signals they produce to initialize, control, and readout the qubits in a large-scale QC system will need to be fully characterized with calibrated measurements of signal power, phase, distortion, and noise. A programmable, self-calibrated microwave reference source is one tool that NIST is developing to enable these measurements.

REFERENCE SOURCES FOR MICROWAVE SIGNALS

The primary standards developed at NIST for dc and ac voltage used around the world are based on superconductor circuits consisting of series arrays of $N = 10^3$-10^5 JJs [7,8]. When an array of JJs is driven with a current pulse of appropriate amplitude, it will emit a voltage pulse with a quantized time-integrated area exactly equal to $N\Phi_0$, where N is the number of JJs and $\Phi_0 = h/2e$ is the magnetic flux quantum defined by two fundamental constants, h and the unit of elementary charge e. Programmable, arbitrary waveforms can be generated by driving the JJ array with encoded pulse patterns using pulse density modulation [8]. The quantized output pulse areas are identical for every device, traceable to fundamental constants, and immune to variations in operational and environmental parameters. NIST is extending this technology to develop RF waveform synthesizers as reference sources for telecommunications metrology [9,10]. Waveform synthesis at 1 GHz with up to -28 dBm output power [11] and a 4-tone multi-sine signal [12] with programmable amplitudes and phases have been demonstrated.

NIST is also developing these quantum-based synthesizers for quantum information applications [13]. QC laboratory demonstrations typically route signals through coaxial cables from racks of room temperature microwave electronics into the cryostat to perform the initialization, control, and readout of qubits; this “rat’s nest” configuration is not scalable. The scaling of cryogenic QCs will require closer integration of the qubits with compatible cryogenic, energy-efficient, electronics for qubit control and readout [14,15]. Several research groups worldwide are working on cryogenic semiconductor (cryo-CMOS) control solutions [15]. NIST is investigating the use of energy-efficient superconductor pulse generators for in-situ, extremely stable, self-calibrating, reproducible, digital qubit control that is scalable and has potential for standardizing the testing of qubits [16]. These superconducting qubit “drivers” could be combined with cryo-CMOS electronics at the classical-quantum interface of the QC [14].

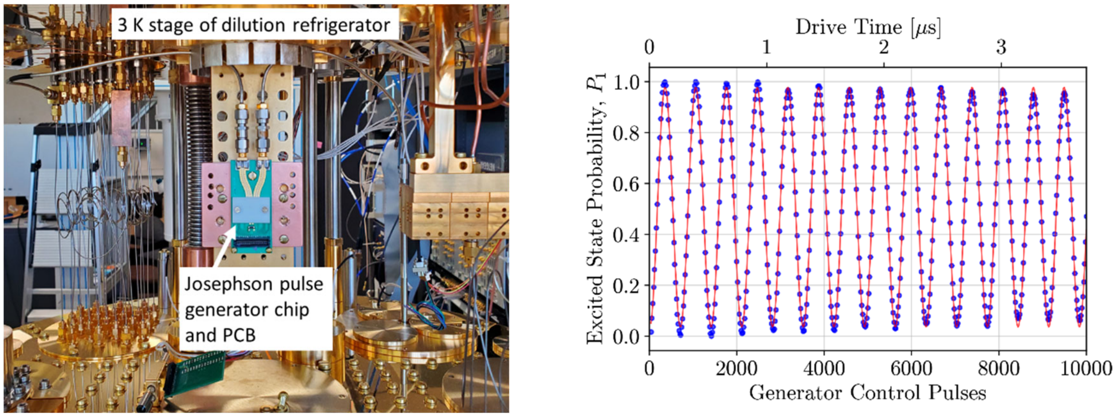

FIGURE 1. Left: A “Josephson pulse generator” located at the 3 K stage of a dilution refrigerator used to digitally control a superconductor qubit at the 10 mK stage (electromagnetic shielding has been removed). Every quantized pulse sent by the generator is identical and causes a discrete change in the qubit state. Right: A Rabi oscillation plot, showing data (blue points) and fit (red line) of the probability that the qubit is observed in the excited state (P1) versus the number of control pulses.

ON-WAFER CRYOGENIC MEASUREMENTS AND STANDARDS

Previously, NIST demonstrated scattering-parameter microwave calibrations at millikelvin temperatures [17] and is now working to combine a commercial room-temperature vector network analyzer with a NIST-developed cryogenic front-end with unprecedented sensitivity to accurately characterize the very low power microwave control and readout signals present at the qubits [18]. Challenges include designing and implementing the front-end to measure modulated microwave signals that are several orders of magnitude weaker than possible with state-of-the-art network analyzers while operating at millikelvin temperatures inside the DR; power, phase and noise-parameter standards are also being developed to reach the lowest power levels. If successful, this instrument will be able to make direct, on-wafer, calibrated measurements of scattering parameters, impedances, voltage and current waveforms, nonlinear distortion, and noise and will be indispensable for design verification and developing the accurate models of microwave systems required for designing large-scale cryogenic, microwave-based QCs.

In related work, NIST has developed a 4 K cryogenic microwave probe station with 3-axis translation for accurately characterizing on-wafer superconductor devices up to 40 GHz. This measurement system is being used to develop the quantum-based waveform sources mentioned above as microwave power standards. The two-tier calibration procedure includes a custom cryogenic through-reflect-line (TRL) microwave calibration kit co-located on-chip with the superconducting devices under test. Loss and dispersion in the input/output signals due to the RF cables and interconnects are de-embedded (subtracted out), enabling accurate measurements of the microwave signals using a vector network analyzer [19].

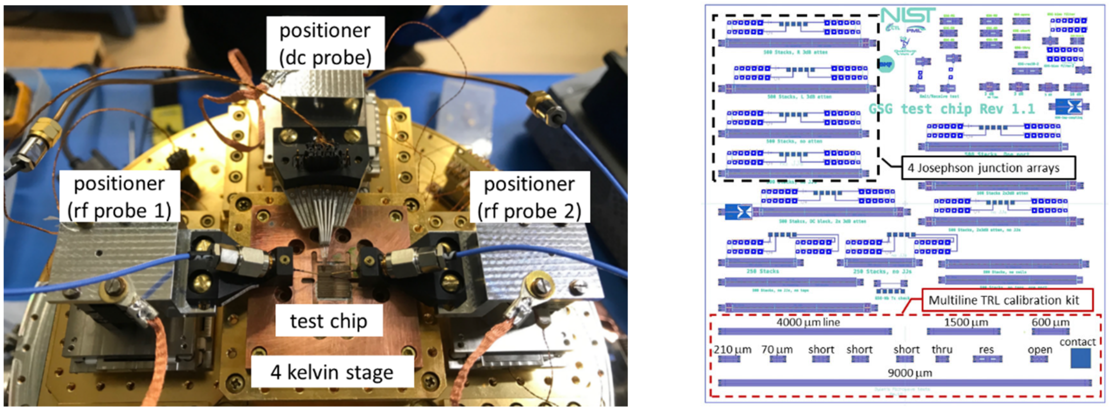

FIGURE 2. Left: Sample stage of NIST's cryogenic microwave probe station. Right: Layout of a 1 cm x 1 cm chip, designed and fabricated at NIST, that includes the cryogenic superconductor-based TRL microwave calibration kit (dashed red box at bottom)) and several superconducting circuits with arrays of Josephson junctions (dashed black box indicates four examples).

Ultrasensitive, calibrated cryogenic microwave measurements and standards for understanding, designing, testing, and scaling the microwave circuits that initialize, control, and readout the qubits are key to enabling the commercialization of large-scale microwave-based cryogenic QCs. NIST's research on cryogenic microwave reference sources, a new cryogenic vector network analyzer with unprecedented capability, and superconducting on-wafer microwave calibration standards should provide assistance towards this challenging endeavor.

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KEYWORDS

Quantum computing, superconductor qubits, qubit control, qubit readout, microwave calibrations

Characterization of 2D materials by ARPES at imec

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The latest generation semiconductor device dimensions are now at a level not thought possible even 10 years ago. And with 3 nm node logic device high volume manufacturing scheduled for 2022-2023 [1], the question asked is: How far can this go on? One of the primary obstacles is: How to control electrical leakage at decreased device dimensions. In this context, a group of materials gaining increased attention are *2D-materials*. Examples of 2D materials include *Graphene*, *Transition Metal Dichalcogenides* (TMDs) and *Topological Insulators* (TIs), of which there are 2D-TIs and 3D-TIs. 3D-TIs have a bulk bandgap along with conductive spin locked surface states. Since these are topologically protected from backscattering and localization, these may pose solutions to electrical leakage with devices based around these requiring less power. Examples of potential applications of TIs for supporting tomorrow's semiconductor roadmap include, Bi_2Se_3 based Field Effect Transistors [2], Spin-Orbit Torque Random Access Memory [3] and even quantum computing [4].

TIs were first theorized in 2005 [5] when it was realized that topology plays a role in defining the electronic structure of 2D materials (the theoretical framework underlying this resulted in the 2016 Nobel prize in physics). In short, the unhindered conduction of spin locked electrons at the 3D-TI surface is a result of the Dirac cone formed close to the Fermi edge (E_F). In 2007, this Dirac cone was empirically confirmed using Angle Resolved Photo Emission Spectroscopy (ARPES) [6]. ARPES is based on the photo-electric effect for probing the electronic structure of solids through the direct and simultaneous measurement of energy and the momentum of the photo-emitted electrons. Supporting this is Photo Electron Emission Microscopy (PEEM) as this employs the same spectrometer and allows for imaging in real space (ARPES maps in k-space, otherwise referred to as reciprocal space). PEEM thus aids in allowing ARPES to be carried out over localized regions of interest.

To support 2D materials research at imec, a dual-purpose initiative was kicked off at the imec Leuven site in 2019 termed the "imec AttoLab". This employs a high powered 5 kHz femto-second Ti-Sapphire laser feeding two High Harmonic Generation (HHG) sources, all of which were installed in 2020. One of these HHG sources produces pulsed coherent photon beams over the 25-120 eV range to support and extend the capabilities of reflectometry, radiometry, Coherent Diffractive Imaging (CDI), mid Infra-red, ARPES and PEEM. Pump-probe ARPES, otherwise referred to as Two Photon Photoelectron Emission (2PPE) will be implemented for mapping of both the Highest Occupied Molecular Orbitals and Lowest Unoccupied Molecular Orbitals as a function of pump-probe delay-time. This will allow for the examination of such features as Floquet-Bloch states. These experiments are planned to start in late 2022, i.e., following the plumbing of the 25-120 eV HHG source to the SPECS spectrometer. The other HHG source provides a pulsed coherent photon beam at 92.5 eV for examining EUV interference lithography possibilities. Figure 1 illustrates the conceptual design.

Henceforth are reported initial ARPES spectra from Graphene, MoS_2 (a TMD) and Bi_2Se_3 (a 3D-TI) acquired using a He discharge source (using the He-1 line at 21.2 eV) within the SPECS spectrometer analysis chamber. Graphene (CVD grown on Cu/Sapphire substrates), MoS_2 (Metal Organic Chemical Vapor Deposition on Sapphire substrates) and Bi_2Se_3 (Molecular Beam Epitaxy grown on Sapphire substrate) were fabricated in-house. Since Bi_2Se_3 is air sensitive, a Se capping layer was also applied in-situ. This layer was subsequently burnt off in the sample preparation chamber attached to the SPECS spectrometer. This preparation chamber contains Low Energy Electron Diffractions (LEED) and Auger Electron Spectroscopy (AES) capabilities to ensure optimal sample preparation.

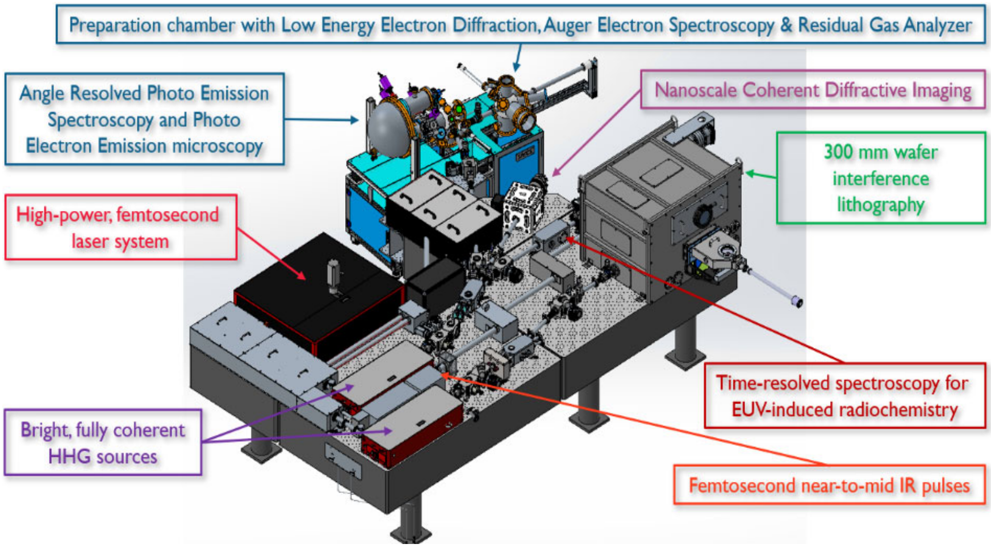

Figure 1: The imec AttoLab

In Figure 2 are shown ARPES spectra collected from single layer graphene and twisted bi-layer Graphene. The latter is of interest since low temperature superconductivity can be realized with a twist angle of 1.05° (a research area called “twistronics”) [7]. The single layer graphene sample exhibited the appearance of 6 Dirac cones, while the twisted bi-layer graphene exhibited 6 additional cones slightly offset from the former. These spectra are in good agreement with published results [8].

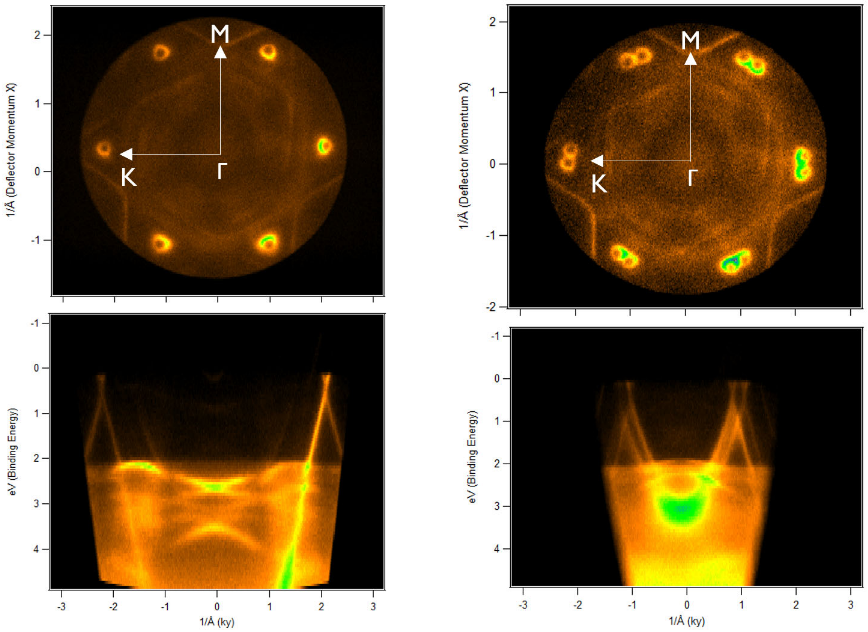

Figure 2: ARPES of Graphene monolayer and twisted bi-layers

In Figure 3 are shown ARPES spectra from 3.5 monolayer (ML) MoS_2 and 1 ML MoS_2 as well as band structure calculations derived elsewhere [9]. These were of interest since an indirect to direct band transition is expected on moving from bulk MoS_2 to 1 ML MoS_2. This is consistent with the observed spectra (see elevation in band at K in the 1 ML case relative to the 3.5 ML case).

In Figure 4 are ARPES spectra from Bi_2Se_3 which are in good agreement with published data [10].

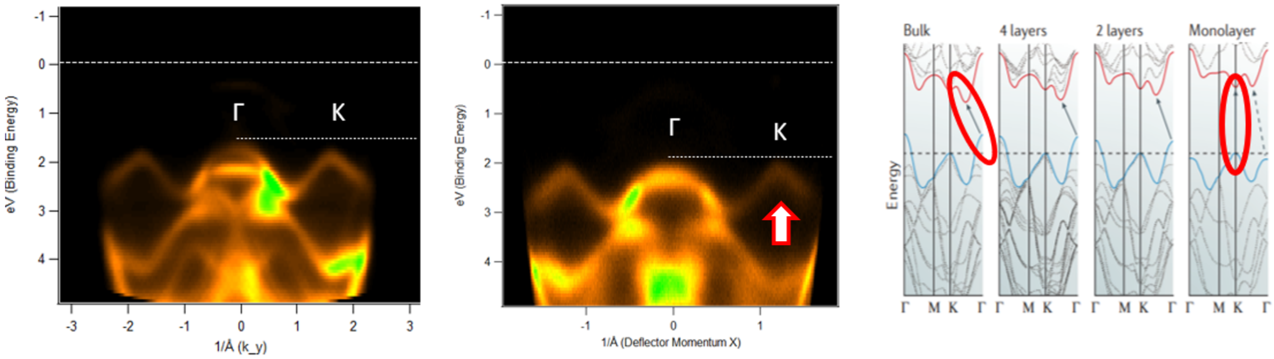

Figure 3: ARPES spectra of the TMD MoS_2 (to the left is shown spectra for 3.5 ML and in the middle is shown spectra for 1 ML) and simulated spectra[9] showing indirect to direct transitions.

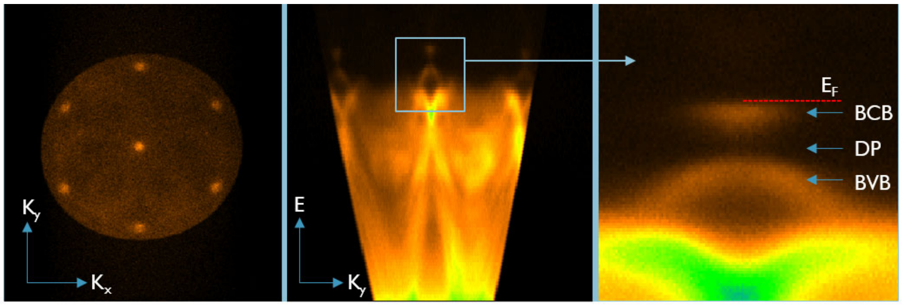

Figure 4: ARPES spectra of the 3D-TI Bi_2Se_3 where BCB refers to the Bulk Conduction Band, DP the Dirac Point, and BVB the Bulk Valence Band.

With the observations of the respective band structures from the various 2D materials realized, the imec-AttoLab is well on course to realize the R&D goals laid out during its inception.

ACKNOWLEDGMENTS

The authors are indebted to Steven Brems, Pierre Morin, and Clement Merckling (all from of imec) for supplying the Graphene, MoS_2 and Se capped Bi_2Se_3 samples respectively. We also recognize the efforts of our joint development partners, SPECs, Berlin, for ARPES support and KMLabs, Boulder Colorado in helping us getting the AttoLab outfitted and operational.

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KEYWORDS

ARPES, 2D materials, AttoLab, Graphene, MoS_2, Bi_2Se_3

DEVELOPMENT OF NV MAGNETOMETRY FOR SPIN MAPPING AT THE ATOMIC SCALE

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INTRODUCTION

The measurement of low-amplitude magnetic signals with nanoscale spatial resolution is essential in many research fields including materials science as well as a major challenge for understanding the properties of emerging magnetic materials that are of interest for the development of new spintronics devices. Although scientists have a wide range of high-sensitivity magnetometry techniques at their disposal, mapping a magnetic field distribution in a quantitative and non-perturbative way with nanometric spatial resolution still remains a major experimental challenge. In this context, the last decade has seen the emergence of a new generation of magnetic sensors exploiting the properties of individual quantum systems. Such quantum sensors, based on experimental methods originally developed for quantum information, promise exceptional performance due to their extreme sensitivity to the environment. Among a large number of elementary quantum systems used as sensors, the NV centre of diamond is of growing interest for magnetic imaging, as it offers an unprecedented combination of spatial resolution and sensitivity, even at room temperature. Such performances have motivated a rapid transfer of these quantum magnetometers to industry, leading to the appearance in 2020 of the first commercial products, barely a decade after the first experimental demonstrations in the laboratory. In this article, we will introduce the operating principle of scanning NV magnetometry (SNVM), illustrate its performances through a few examples and finally present the key steps that led to the release of a first commercial solution by Qnami.

MAGNETIC IMAGING AT THE NANOSCALE WITH SCANNING NV MICROSCOPY

The principle of operation of a SNVM is schematically described in Figure 1. A diamond probe containing a single NV centre is integrated into a scanning probe microscope (SPM), allowing the NV probe to be moved in a controlled manner close to a magnetic structure to be characterised. A confocal optical microscope is coupled to the SPM to optically excite the NV centre positioned at the tip and measure its magnetic resonance spectrum using resonant microwave excitation. The magnetic field mapping is then obtained by measuring the Zeeman shift of the optically detected magnetic resonance (ODMR) at each point of the sample. The detection volume, and thus the intrinsic resolution limit, is here basically fixed by the spatial extension of the electron spin wave function of the NV centre, which is of the order of a few angstroms. In practice, however, the spatial resolution of the magnetic microscope is limited by the distance between the NV probe and the sample, which is typically of the order of a few tens of nanometres. The resulting magnetometer allows quantitative and vector mapping of the magnetic field, with a sensitivity of up to 100 $\mathrm{nT/Hz^{1/2}}$. In addition, the measurement is non-perturbative and can be performed at room temperature without any restrictions on the choice of materials studied. The combination of all these features is currently not offered by any other magnetic microscopy device. After the first proof-of-principle experiments performed about ten years ago [1,2], SNVM has rapidly found numerous applications, including the study of chiral spin textures in ultrathin ferromagnetic layers, current imaging in graphene-based components, or the analysis of magnetic order in two-dimensional magnets down to the monolayer limit.

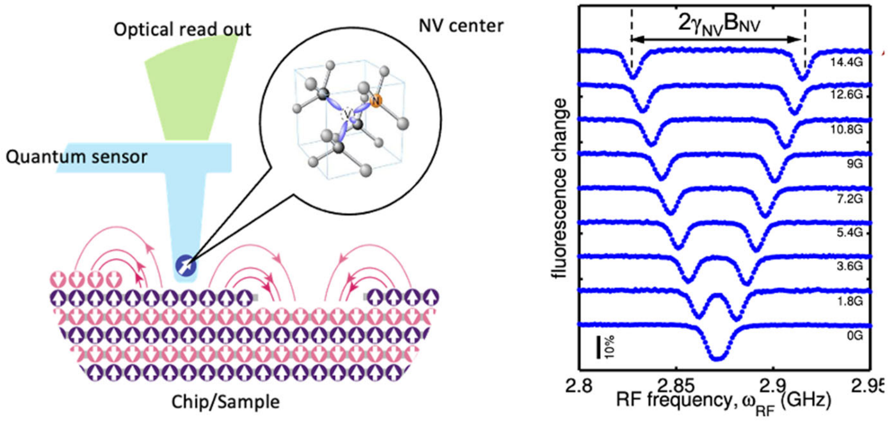

FIGURE 1. Principle of Scanning NV Magnetometry. The quantum sensor is an all-diamond SPM probe containing a single NV center (left). A combination of optical and microwave pulse generates the optically detected magnetic resonance (ODMR) spectra shown on the right. The amplitude of the B field at the NV center position directly translates into a splitting of the two main resonances (Zeeman effect). A full map of the magnetic stray field is obtained by recording such ODMR spectra as the probe is scanned over the sample.

A NEW TOOL FOR THE STUDY OF MAGNETIC SIGNALS

These new capabilities have led to breakthrough in materials science. In this section we illustrate the capabilities of SNVM through a few examples.

First, we show non-perturbative field distribution mapping in ultra-scaled magnetic nanowires with diameters down to 6 nm. The studied sample consists of an array of CoFeB NWs with cross-sectional areas of about 120 nm^2, a wire width of about 6 nm, and mm lengths. Figure 2a reveals the presence of weak magnetic inhomogeneities inside in-plane magnetized nanowires that are largely undetectable with standard metrology. The magnetic defects could be attributed to local nanometer scale inhomogeneities in the NWs (density, compositional, or strain-induced) that led to fluctuations of the in-plane saturation magnetization [3]. More quantitatively, SNVM allowed detection of local variations Ms in the CoFeB NWs on the order of 30% or less with nanoscale spatial resolution and µT magnetic field sensitivity.

SNVM also gives access to characterize local currents with excellent spatial resolution. In such operando measurement a sample is investigated under operation allowing, for example, the examination of a chip for failure analysis purposes, the observation of current flow in 2D materials or microwave-imaging in RF resonators. As an example we show the result obtained by applying a current of 250µA, corresponding to a current density of 2.5×105A/cm2 through a 100nm thick Cr/Au microwire. By flowing through the wire, the current induces a local magnetic field, which we detect using the ODMR signal of the NV center. From the magnetic field, the local current density can be readily calculated. The result is shown on Figure 2b. We recover the applied magnitude current density and note two interesting details. First, some but not all defects in the wire lead to an enhanced current flow in their vicinity and second, the current flow is enhanced in the inner edges of the U-shape and reduced at the outer edges.

In the last example we show the sensitivity of SNVM to atomically thin magnetic layers. In this experiment, performed under cryogenic environment (4K), the Van der Waals material chromium triiodide (CrI3) is studied. Using SNVM, the magnetic field from CrI3 atomic layers is measured quantitatively [4]. Using backwards propagation techniques, the magnetization of CrI3 monolayer is found to be 16 Bohr magnetons per square nanometer. Furthermore, the analysis of odd and even number of layers reveals the antiferromagnetic nature of the CrI3 in the limit of few atomic layers (Figure 2c).

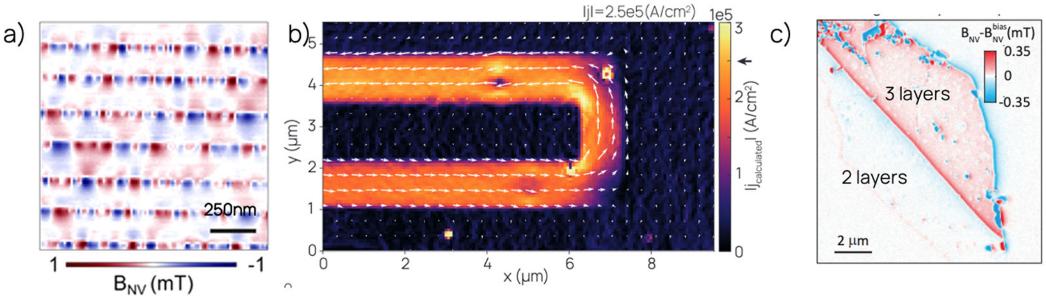

FIGURE 2. Examples of application using SNVM. (a) Non-invasive imaging of the magnetic stray field produced by ultra-scaled nanowires (sample IMEC). The data shows 7 nanowires which present magnetic field variations on the nanoscale attributed to local structural or compositional inhomogeneities in the nanowire. b) Current density map reconstructed from the measurement of magnetic field induced by a 250um current in a microwire. c) Quantitative imaging of the magnetic field produced by an odd or even number of atomically thin layers of CrI_3. The measurements, performed in cryogenic environment, reveal the antiferromagnetic nature of the material in the limits of few atomic layers.

A RAPID TECH TRANSFER TO THE INDUSTRY

Such performance has motivated a rapid transfer of NV scanning magnetometers to industry. The explosion of research and development activities in spintronics has intensified the need for reliable and accurate methods to explore the properties of magnetic materials at the nanoscale. In order to reach a diverse audience of scientists and research engineers, a commercial instrumental solution must meet several requirements, including stability, reproducibility and ease of use. This is all the more important when the final product combines a large number of advanced or even emerging technologies (quantum sensors, ultra-stable scanning probe microscopy, confocal optical reading of a single NV centre). A first essential step has been taken with the development of a reproducible micro-fabrication process allowing the production of SPM probes from very high purity diamond, offering a considerable improvement in the quantum properties of the NV centre, as well as its precise localisation at the apex of the probe [2]. This process, based on lithography and dry etching techniques borrowed from the semiconductor industry, has enabled an increase and scaling of the performance of the core component of the technology (see Figure 3a) The subsequent development of an instrumental platform for the integration of this new quantum sensor is also remarkable. On the one hand, the choice of components, and the realization of a dedicated platform allows to commercially offer performances superior to the best experimental prototypes realized so far (image size, acquisition speed, sensitivity). On the other hand, the integration in a simplified user interface of new measurement protocols using the quantum properties of the NV centre makes it possible to target a wide audience, beyond the community of experts in quantum mechanics, right into industry. Figure 3b shows this first commercial scanning NV magnetometer, built in partnership by Qnami and HORIBA. A version compatible with cryogenic (2K) temperatures is currently under development by Qnami.

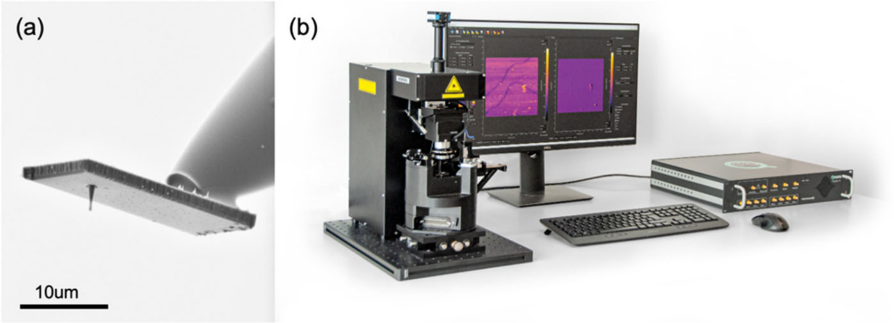

FIGURE 3. Commercially available SNVM. (a) SEM picture of a Quantilever^{TM}, an all-diamond probe containing a single NV center. (b) Qnami ProteusQ, the first commercially available Scanning NV Microscope realized in partnership between Qnami (Switzerland) and HORIBA Scientific (France). A version compatible with cryogenic temperatures is currently under development by Qnami.

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KEYWORDS

Scanning NV Microscopy, Scanning Probe Microscopy, Magnetic materials, Ferromagnets, Antiferromagnets, Van der Waals materials, MRAM, microwave imaging.

Magnetic mapping with nm-scale resolution for spintronic devices by transmission electron microscopy.

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INTRODUCTION

In this presentation, we will introduce three different methods that can be used to measure the magnetic fields in spintronic devices with nm-scale resolution. The first is off-axis electron holography which uses an electron biprism to interfere an object wave with a reference wave to form an interference pattern known as the hologram. Using a simple reconstruction technique, it is possible to obtain a phase image, which is sensitive to the electromagnetic fields in and around the specimen. Two alternative methods are differential phase contrast (DPC) imaging which has been used since the 1970s, or the more recent pixelated-STEM (4DSTEM). For both of these techniques, a convergent beam is scanned across the specimen and the magnetic field can be calculated by measuring the deflection of the beam. In this presentation we will present these three different methods of measuring magnetic fields on a ferromagnetic NiFe nanowire that has been used as a simple calibration specimen. We will discuss the performance of each, the ease of use and the advantages and disadvantages of each approach. We will then show these techniques applied to measure the magnetization in a range of different types of MRAM devices including 20 nm radius PSA-STT (Perpendicular shape anisotropy spin-transfer torque) MRAM (Magnetic random access memory) devices as they are heated in-situ in the TEM such that their stability can be assessed at elevated temperature.

MAGNETIC MAPPING OF A SIMPLE CALIBRATION SPECIMEN

Off-axis electron holography has been used for nearly 40 years to study magnetic fields in specimens [1]. The phase of an electron wave that has passed through a specimen will be changed by the electromagnetic field. This phase change is given by

$$\phi(x) = C_E \int V(x,z)dz - \frac{e}{\hbar}\iint B_\perp(x,z)dxdz$$

where z is the direction of the incident electron beam, x is a direction in the plane of the specimen, V is the electrostatic potential, C_E a constant and $B_\perp$ is the component of the magnetic induction that is perpendicular to both x and y. Therefore the use of holography for the measurement of magnetic fields is complicated in that the phase image is mixed with information about the electric field and as such, these two components need to be separated. As the magnetic induction field is a vector field and the electric field is scalar, it is possible to obtain the magnetic induction field by acquiring two holograms, either with the sample “flipped” by 180° or by reversing the magnetic induction field using the objective lens. Thus the difference between the two phase images is two times the magnetic phase contribution, while the electric phase is half of the sum of the two phase images.

For DPC and 4DSTEM, for 200 kV electrons, the magnetic induction, B⊥ in Tesla can be calculated from the measured displacements of the transmitted beam using the simple relation

$$B_{\perp=}-\frac{\gamma}{t}\cdot 1.649\cdot 10^{-3}$$

where γ is the deflection angle and t the specimen thickness in nm [2]. These techniques also similtaniously measure both the magnetic and electrostatic fields and the magnetic induction component again can be obtained by reversing the magnetic field to reverse magnetization in the sample, and then subtracting the electrostatic component.

Figure 1 shows experimental results obtained on a NiFe nanowire to assess the signal to noise, spatial resolution and accuracy of our measurements. Electron holography was performed using the Titan Ultimate and stacks of holograms were acquired to provide an improved signal-to-noise ratio. Figures 1(a) and (b) show holography reconstructions of the amplitude images of the NiFe nanowire in the two orientations, one with the sample rotated by 180°. The phase images for each orientation containing both the magnetic and electric contributions are shown in (c) and (d) respectively. Figures 1(e) and (f) show the magnetic and electric phase maps, respectively. Pixellated STEM measurements were acquired on a FEI Titan Themis operated at 200 kV. The experimental results can be seen in Figures 1(g) and (h) that show two virtual bright field images of the nanowire that have been calculated by summing the scattered intensity outside of the transmitted beam for each orientation. The total deflection of the beam containing both the magnetic and electric components for each orientation can be seen in Figures 1(i) and (j) where the contrast scale is in units of displacement in CCD pixels. The arrows also indicate the strength and direction of the beam displacement. Figure 1(k) shows the magnetic displacement component and Figure 1(l) shows the electrostatic displacement component. Figure 1(m) shows the magnetic induction that has been calculated from the derivative of magnetic phase measured by electron holography. The colour wheel and the arrows indicate the strength and direction of the field. This can be compared to Figures 1(n) showing the results for the pixelated STEM and (o) for the micromagnetic simulations. Profiles extracted from the regions indicated in Figures 1(m-o) have been extracted for the holography, 4D STEM and simulated maps of the magnetic induction. These are shown in Figure 1(p) for the case of profile 1, which passes through the wire and in Figure 1(q) for profile 2 which passes only through vacuum and measures the stray field at the end of the wire. These profiles that have been obtained for both off-axis electron holography and pixelated STEM are consistent with the simulations [3].

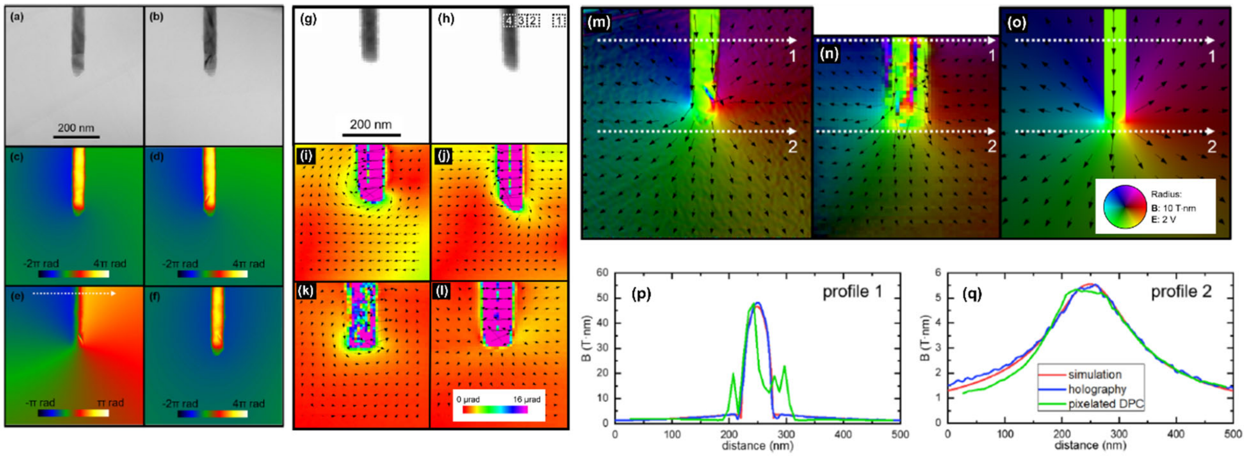

FIGURE 1. Comparison of electron holography and pixelated STEM on a simple NiFe nanowire compared to simulations.

MEASUREMENT OF THE THERMAL STABILITY OF PSA-STT MRAM DEVICES

Perpendicular shape anisotropy is a method that can potentially provide improved thermal stability in aggressively scaled STT-MRAM devices through an increased volume of the magnetic storage layer. In order to demonstrate these improvements directly, we used an optimized electron holography approach using novel specimen preparation and increased the signal-to-noise ratio by summing stacks of holograms. We will present observations of a 20 nm radius FeCoB / NiFe pillars as a function of temperature measured by off-axis electron holography. Figure 2 shows a (a) HAADF STEM image and (b) EDX of a pillar containing a PSA magnetic stack. The electrostatic and magnetic components of the phase are shown in Figure 2(c) and (d) respectively. To visualise the thermomagnetic stability within the nano-pillar, Figures 2(e) to (l) show magnetic induction maps of the PSA in the NiFe section of the nano-pillar acquired at 20 ^{0}C and then at 25 ^{0}C intervals from (f) 100 ^{0}C to (l) 250 ^{0}C. The magnetization direction is shown using arrows and colors described in the wheel in (a). We will show in this presentation that for the PSA-STT stacks, the magnetic induction field, directly connected to the magnetization field, is stable at these higher temperatures and are compared to much larger conventional STT stacks that become unstable at temperatures of around 150°C [5].

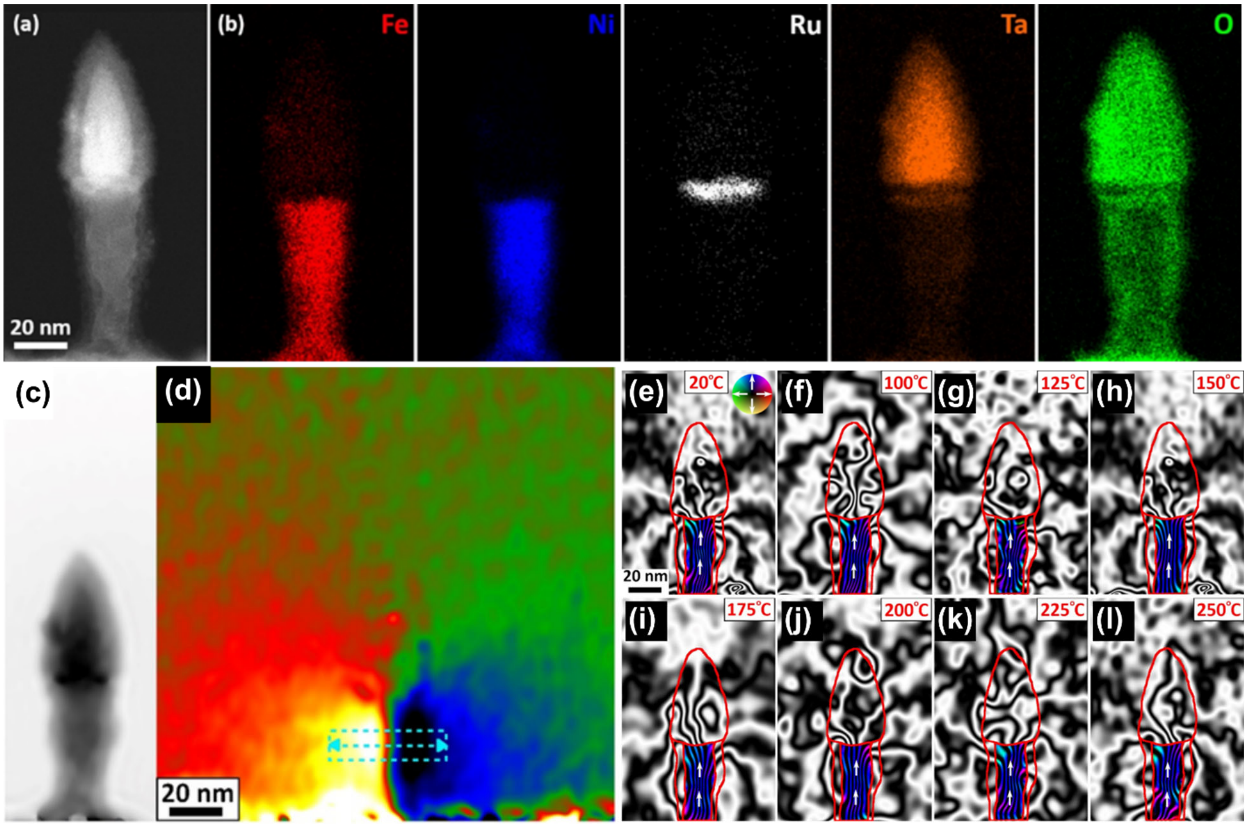

FIGURE 2. Electron holography was used to measure the stability of the magnetization in PSA-STT MRAM devices at elevated temperatures.

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KEYWORDS

Magnetic Imaging, Electron Holography, Pixellated STEM, Differential Phase Contrast, STT-MRAM

Thin EUV photoresist layers for microelectronic devices: pivotal benefits of the Orbitrap™ mass analyzer for accurate analysis

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INTRODUCTION

Photolithography is a well-established process used to pattern microelectronic devices. However, a deep understanding of the chemistry of all the photoresist components (polymer, photoacid generator (PAG) and quencher) is needed to allow to optimize and improve the process for future devices of smaller dimensions (nm). One of the important aspects to investigate is the 3D distribution within thin chemically amplified photoresist (CAR)[1] used for fine patterning in extreme ultraviolet lithography (EUVL). Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS) is a well-known technique used to assess the 3D distribution of organic molecules and polymers in solid substrates. However, its mass resolution, usually considered as relatively high (M/ΔM ~10000), can become insufficient to unambiguously assign detected peaks in the analysis of large organic fragments and molecules. To overcome this problem, an Orbitrap™ mass analyzer[2] can be used, allowing to increase the mass resolution up to more than 240000. This paper reports on the SIMS depth profiling of unexposed and photo exposed CAR films using both ToF- and Orbitrap^{TM} mass analyzers. It will be demonstrated that the ToF-SIMS method is found to be inadequate to study the chemical evolution of the CAR layers after EUV photo exposure, while the use of Orbitrap^{TM}-SIMS allows to obtain interesting insights on the chemical changes occurring during increasing photo exposure dose. Among all the differences in the two set-ups, the main advantage of the Orbitrap^{TM} mass analyzer is related to its increased mass resolution and mass accuracy (a few ppm) provided and to its MS/MS capability.

EXPERIMENTAL DETAILS

A model CAR material composed of a polymer with protection groups, a PAG and a quencher (see Figure 1a), to c)) was used. The material was spin-coated onto Si wafers, baked at 90 °C for 60 s, exposed in an ASML's EUV scanner NXE3300 at various doses up to 400 mJ/cm^2, and finally baked again (post exposed bake - PEB) at 90 °C for 60 s to amplify the catalytic deprotection reaction. During EUV photo exposure, the PAG cation decomposes in the photoresist layer, activating the acid formation (H^+) as described in Figure 1d) following two possible routes. During the PEB, the PAG is expected to diffuse and catalyze chemical reactions, such as the deprotection of the protective group in the polymer (Figure 1e)). The deprotected group will then leave the thin layer as volatile isobutene. The quencher's role is related to the enhancement of the pattern resolution (during the development) by neutralizing acids in the dark region and reducing their diffusion from exposed to unexposed regions.

ToF-SIMS analysis of these CAR films was performed with a ToF-SIMS NCS instrument (IONTOF GmbH, Münster, Germany) operated in dual beam mode using Bi_1^+ species at 15 keV as analysis beam (in spectrometry mode for high mass resolution) and Gas Cluster Ion Beam (GCIB) using Ar_{2000}^+ at 5 keV as sputter beam. The GCIB was chosen as the primary ion sputter source to preserve the molecular information of the different organic components in the layer, i.e. to minimize sputter induced damage. The Orbitrap^{TM}-SIMS analysis was performed on a Hybrid

SIMS instrument (IONTOF GmbH, Münster, Germany) operated in single beam mode, using the GCIB as primary ion gun with the same conditions as used in the ToF-SIMS experiment. Both ToF- and Orbitrap^{TM}-SIMS experiments were acquired in the negative ion detection mode.

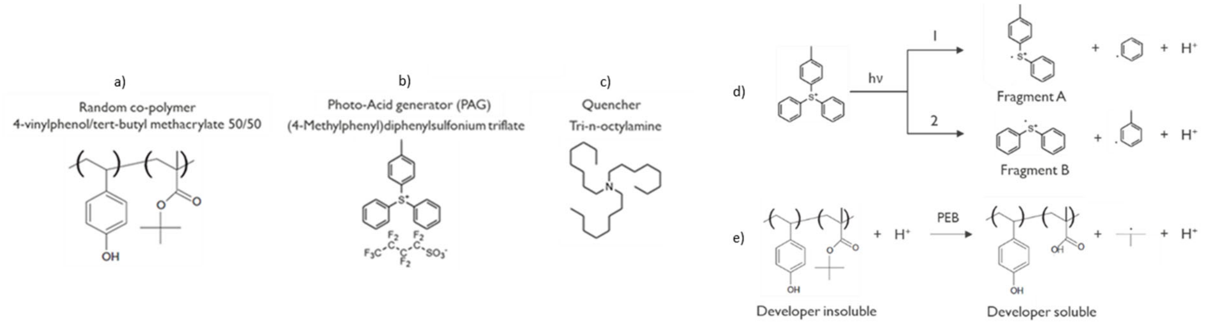

FIGURE 1. Schematic representation of the molecular structures for (a) random co-polymer, (b) PAG, (c) quencher, and of the reactions involved during (d) photo exposure and (e) post-photo exposure bake (PEB) for PAG cation and co-polymer.

RESULTS AND DISCUSSION

MS/MS[3] with the Orbitrap^{TM} mass analyzer was conducted on the unexposed sample in order to understand the molecular structure of the precursor peak measured at mass 277.1045 m/z and assumed to correspond to the PAG molecular peak $C_{19}H_{17}S^+$. Collisional energies (CE) between ~11.08 and ~55.42 eV were applied in the Higher energy Collisional Dissociation (HCD) cell, as shown in Figure 2. Specific product ions, originating from the fragmentation of the precursor, were observed and assigned. The precursor ion (at 277.1045 m/z) becomes barely visible after ~33.25 eV, indicating that this molecular ion has encountered a near complete fragmentation. We can also clearly see that the intensity of smaller fragments increases for higher CE. A clear assignment of these small fragment's peaks can be done thanks to the exceptional mass resolution and accuracy of the Orbitrap^{TM} analyzer. The observed fragmentation trends support the assignment of the peak at 277.1045 m/z to the molecular structure consistent with that of the PAG molecule as opposed to some other isomer (a molecule with formula $C_{13}H_{12}S$, but with a different molecular structure).

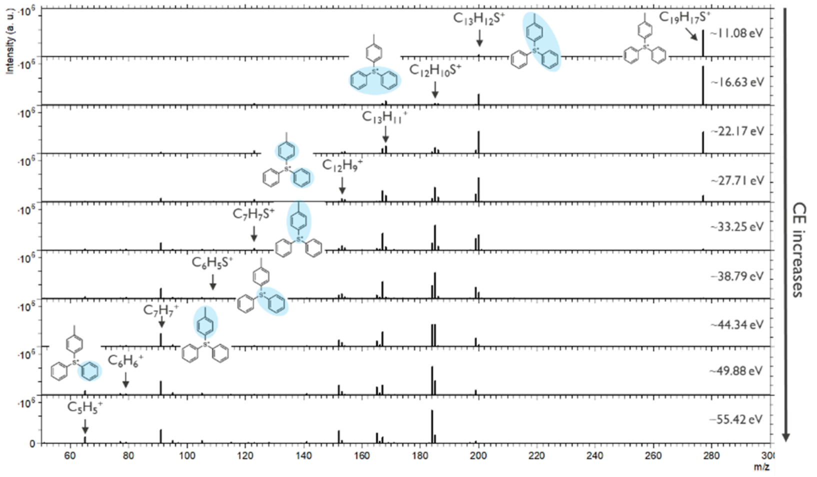

FIGURE 2. MS/MS spectra overlay at different CE. The most relevant fragments are indicated by an arrow and their molecular formula. The fragment structures are indicated on the molecular structure signified as shaded.

Being now confident with the peak assignment of the PAG molecular signal at mass 277.1045 m/z, further ToF- and Orbitrap^{TM}- SIMS depth profiles were carried out on the set of unexposed and EUV exposed CAR layers. Given the above-mentioned chemical amplification process, the PAG decomposition is expected to be translated in the SIMS spectra in a gradual decrease of the PAG's molecular peak intensity, leading to the complete disappearance of this peak when a very high exposure dose like 400 mJ/cm^2 is applied. However, it is clear that the PAG molecular peak is still observed for exposure doses higher than 100 mJ/cm^2 in the ToF-SIMS profiles displayed in Figure 3a). Moreover, the highest applied dose (400 mJ/cm^2) seems not to be sufficient to completely decompose the PAG. On the other hand, the Orbitrap^{TM}-SIMS profiles displayed in Figure 3b) show a drastic drop of the PAG molecular peak after the exposure at 100 mJ/cm^2, reaching intensities close to the background level for the exposure at 400 mJ/cm^2. As shown in the insets of Figure 3, a very broad peak is still measured with ToF-SIMS for the 400 mJ/cm^2 sample suggesting the presence of multiple peaks (most likely related to the polymer matrix, e.g. $C_xH_yO_z$ structure) which will result in a misleading assignment of the peak due to the limited mass resolution of ToF-SIMS. As a minimum mass resolution of ~63000 is required to avoid such mass interference, this problem is not observed in the Orbitrap^{TM}-SIMS measurements thanks to the sufficiently high enough mass resolving power (~230000). As shown in Figure 3b), the Orbitrap^{TM}-SIMS data now confirm the complete disappearance of the PAG molecular peak using 400 mJ/cm^2 exposure dose.

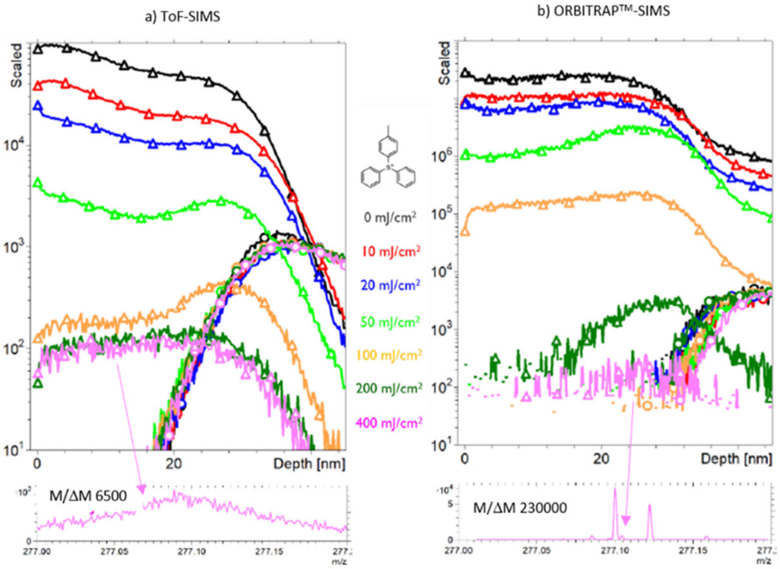

FIGURE 3. a) ToF- and b) Orbitrap^{TM} -SIMS profiles on unexposed and photo exposed samples. The plot shows the PAG molecular (triangles) and Si signals (circles). The inset shows the PAG mass peaks for the 400 mJ/cm^2 doses.

CONCLUSIONS

We described the application of GCIB-SIMS methodology for studying the chemistry and distribution of thin photoresist layers on EUV exposure. We demonstrated that SIMS experiments run with an Orbitrap^{TM} mass analyzer can reveal important modifications of the chemical composition, such as the PAG molecular ion disappearance induced by the exposure process. The above-mentioned modifications could not be highlighted with a conventional ToF-SIMS, due to severe mass interference between the PAG molecular ion and some neighboring signals related to the polymeric matrix. The trends in the 277.1045 m/z peak intensity (unambiguously assigned to the PAG using MS/MS performed in the Orbitrap^{TM} mass analyzer) as a function of exposure dose could be used as a potential method to define optimal EUV exposure dose.

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KEYWORDS

Orbitrap^{TM}, Time of Flight, Secondary Ion Mass Spectrometry, Photoresist, Extreme UV (EUV) photo-exposure, MS/MS

A Correlative TOF-SIMS & XPS Protocol For Analysis Of Organic Light-Emitting Diodes Layers

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INTRODUCTION

Since their invention in 1987 by Tang and Van Slyke [1], organic light-emitting diodes (OLEDs) have achieved tremendous progress leading to their commercialization twenty years later. Nowadays, research focuses on the improvement of the devices lifetime and efficiency by introducing new structures, molecules and dopants. Along these developments, the understanding of degradation mechanisms in the organic layers has become essential to increase the devices performances [2]. Composed of thin layers (~100nm in total), the analysis of OLEDs multilayers requires the use of instruments with good depth-resolution as well as a capacity to probe small changes from aging. Time of flight of secondary ion mass spectrometry (TOF-SIMS) and X-ray photoelectron spectroscopy (XPS) have been individually used to study the degradations in the devices [3, 4]. However, despite their complementarity, few studies correlate the results from each characterization techniques.

CORRELATIVE PROTOCOL

We developed a correlative protocol to obtain precise chemical characterization of OLEDs stacks and insight on their degradation mechanisms. By varying the argon cluster ion fluence over the surface, a bevel crater is formed. The analysis of the same crater by TOF-SIMS and XPS enables the correlation of the information from the two techniques. In TOF-SIMS, an image of the surface is obtained by scanning the surface of the crater, which allows the reconstitution of a profile of the different characteristic molecular ions. Then the sample is transferred to the XPS chamber using a transfer vessel under N_2 atmosphere; a line scan along the crater allows the identification of the different layers. High resolution core-level spectra acquired in each layer informs about the chemical environment of each elements. An easy correlation of the TOF-SIMS and XPS results as well as reduced analysis and sputtering damages on buried layers are achieved with this protocol.

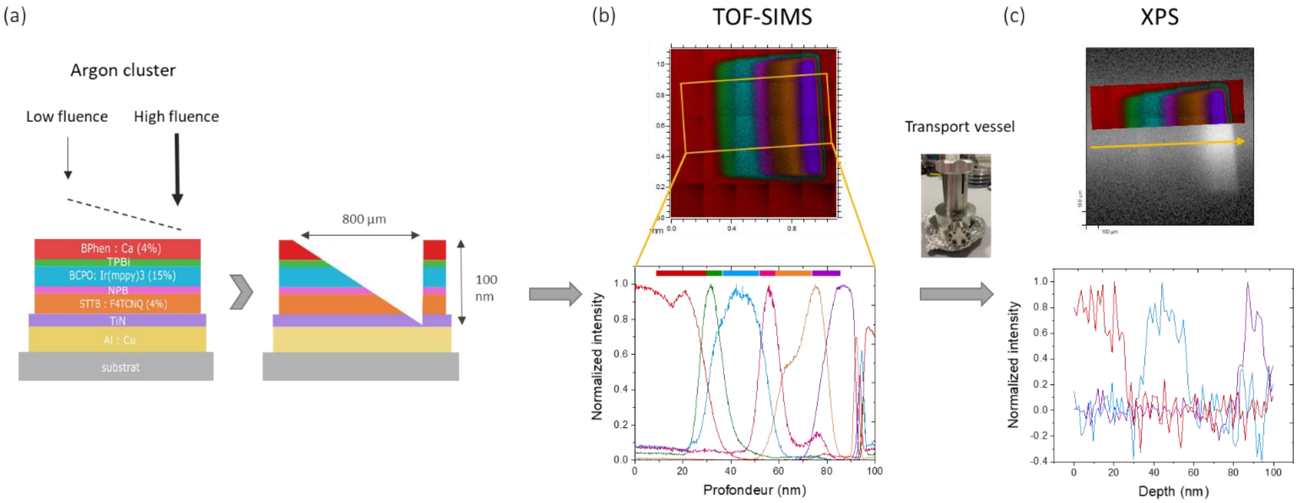

FIGURE 1. Correlative protocol for the analysis of thin multilayer OLED structures: (a) fabrication of the bevel crater by applying an argon cluster ion fluence gradient over the surface, (b) TOF-SIMS scan of the surface and the reconstituted profile and (c) XPS linescan over the surface of the bevel crater.

This protocol also allows tandem MS imaging to be used to resolve ambiguities in peak identification in the layers or to help identify the products of degradation [5]. Figure 2 shows a bevel crater in an OLED stack before and after a few minutes air exposure. The TOF-SIMS image is of the characteristic peak for BPhen. Before air exposure, the signal from this peak is located around the top of the crater that corresponds to its expected position in the stack (red layer in diagram). However, after air exposure this signal is much stronger at the bottom of the crater. To check that this signal really is BPhen and not a mass interference, tandem MS spectra were taken at the top and bottom of the crater and compared to a reference spectrum without air exposure. The similarity in these spectra confirms that at both locations the signal is coming from the BPhen molecule. This suggests that with air exposure the BPhen migrates over the surface of the crater. This is consistent with prior observations that this layer is particularly air sensitive, undergoing oxidation and crystallization rapidly upon air exposure [6]. This example highlights the need for transfer under a protective environment between XPS and TOF-SIMS instruments. When this experiment is repeated, replacing air exposure with a protected transfer between the two instruments there is no change in the position of the BPhen signal.

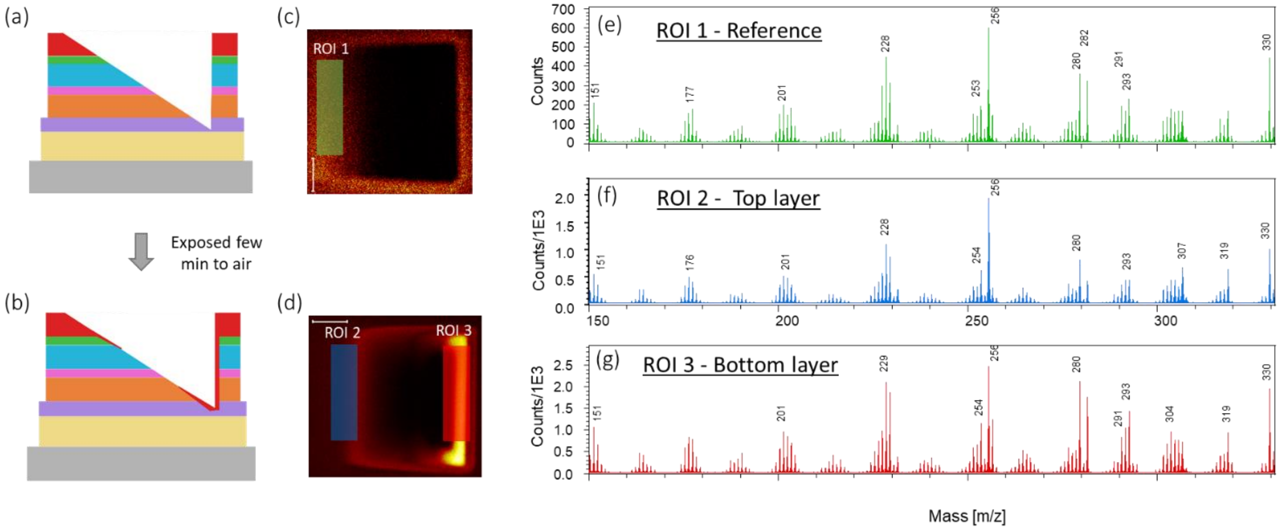

FIGURE 2. Tandem MS imaging of a bevel crater in an OLED stack before and after a few minutes exposure to air. Lateral scheme of the bevel crater (a) before and (b) after air exposure, TOF-SIMS image and ROI selected to compare the spectrum (c) before and (d) after air exposure, (e), (f) and (g) mass spectrum of the different ROI

CONCLUSIONS AND PERSPECTIVES

As well as facilitating the study of ageing in hybrid inorganic/organic stacks such as OLEDs, this bevel crater approach can also be applied to a wide range of applications where TOF-SIMS and XPS depth profiling are required on exactly the same sample area. For inorganic samples, a monoatomic ion beam (Ar, Cs, O, Xe, etc) can be used instead of the argon cluster beam.

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KEYWORDS

OLEDs, TOF-SIMS, XPS, correlative protocol, bevel crater

Scanning Microwave Impedance Microscopy for Nanoscale Characterization and Metrology of Semiconductor Devices

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INTRODUCTION

The revolution in materials engineering that has enabled the continued performance improvements in semiconductor devices also requires new metrology and characterization technologies to be adapted to the manufacturing process. We introduce here scanning Microwave Impedance Microscopy (sMIM), a technology that can measure critical material properties such as the dielectric constant (k-value), capacitance, resistivity and permittivity all at the nanoscale. Types of measurements to be presented include C-V for dielectric quality/integrity and mapping of carrier concentration in a number of devices. Additional applications are envisioned in emerging memory material such as PCM and MRAM. Until recently, sMIM images have only been qualitative but new developments now provide quantified images of material properties such as carrier concentration. We will present the methodology behind this latest development and show related examples.

SCANNING MICROWAVE IMPEDANCE MICROSCOPY

In this technique, an AFM cantilever is used as a microwave source to measure the electrical properties of materials at nanometer scale. An sMIM measurement provides the local permittivity and conductivity of films. From this measurement we derive properties such as capacitance, dopant concentration, resistivity and can also identify certain defects. Since microwaves can penetrate deep into the sample, we can measure sub-surface layers as well.

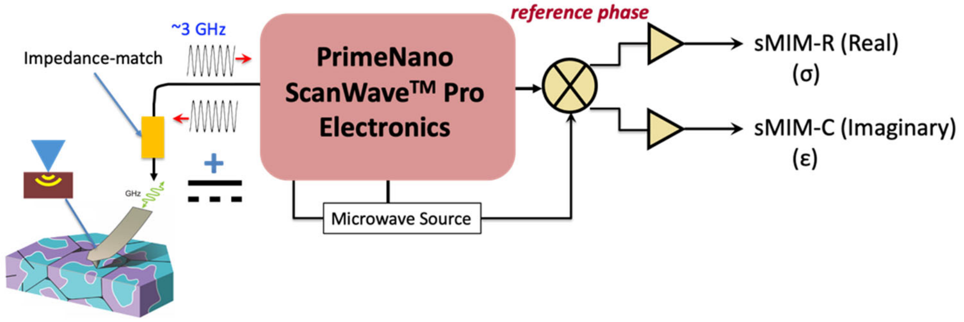


FIGURE 1. The ScanWave sMIM system uses a shielded probe to deliver microwaves to the custom AFM tip and collects the reflection determine the resistance and capacitance of the sample immediately beneath the tip.

Carrier Concentration Measurements

The carrier concentration in semiconductors is a very critical property that must be controlled precisely. In today's devices, the range of dopant concentration is very broad, from intrinsic silicon to degeneratively doped silicon. sMIM lends itself very nicely to make these measurements because of the ultra-high sensitivity of this technology as implemented in the ScanWave product. It was previously shown that sMIM can measure carrier concentrations from 1E15 to 1E20 a/cm^3 [1]. The sensitivity of ScanWave to capacitance is less than 0.1 aF and when this is used to measure carrier concentration, variations in intrinsic silicon can be detected as can variations in heavily doped material (Fig 2). The entire range typically used in semiconductor manufacturing is easily measured with sMIM.

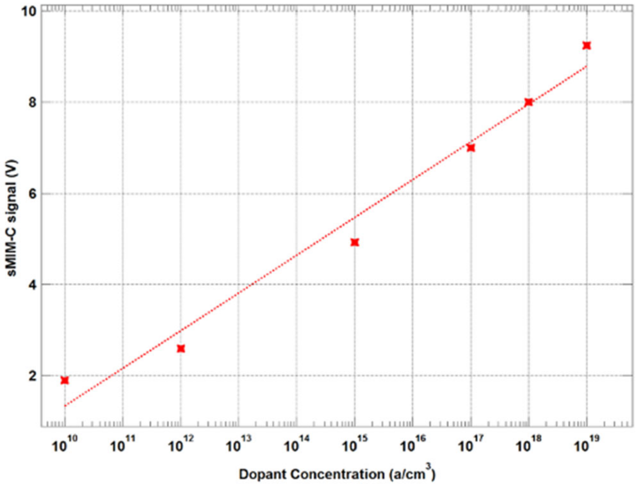
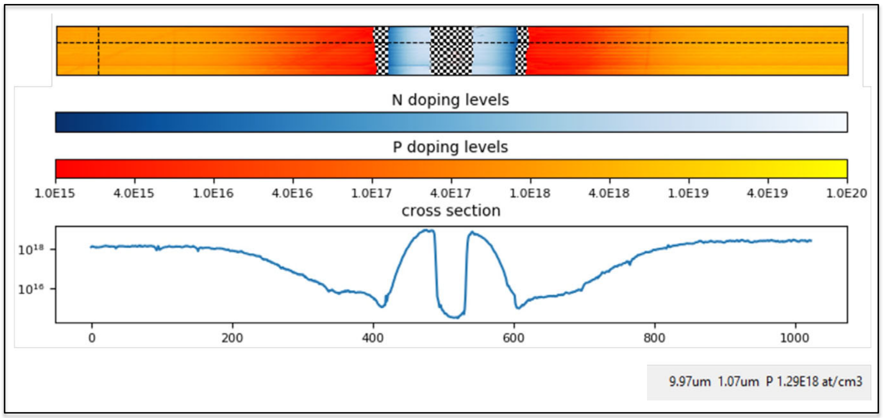


FIGURE 2. Response of ScanWave Capacitance Signal to Carrier Concentration in Silicon.

Quantification of Carrier Concentration

We developed the capability to automatically quantify the carrier concentration by using a reference sample, specialized hardware and software. Because the response of the sMIM signal is log-linear to carrier concentration, the quantification process is mathematically simplified [2]. The quantified results are shown as a thermal map (Fig 3) where any point in the image contains the local carrier concentration and operations such as a line scan are also enabled (lower part of Fig. 3). The line scan in this cross-sectional image provides a carrier depth profile. The carrier concentration value is displayed in the bottom right of the image for the corresponding cursor location.



9.97um 1.07um P 1.29E18 at/cm3

FIGURE 3. Quantified results of a two-piece sample of epitaxially doped silicon glued face-to-face for comparison of the doping level between the two samples.

Repeatability of Carrier Concentration Measurements

The repeatability of this measurement was determined using an implanted reference sample with a staircase of increasing doping levels from left to middle for n-type and middle to right for p-type. Ten measurements per dopant level were taken and the repeatability of the measurement was calculated (error bars) to be well within a tenth of a decade of carrier concentration as shown in figure 4.

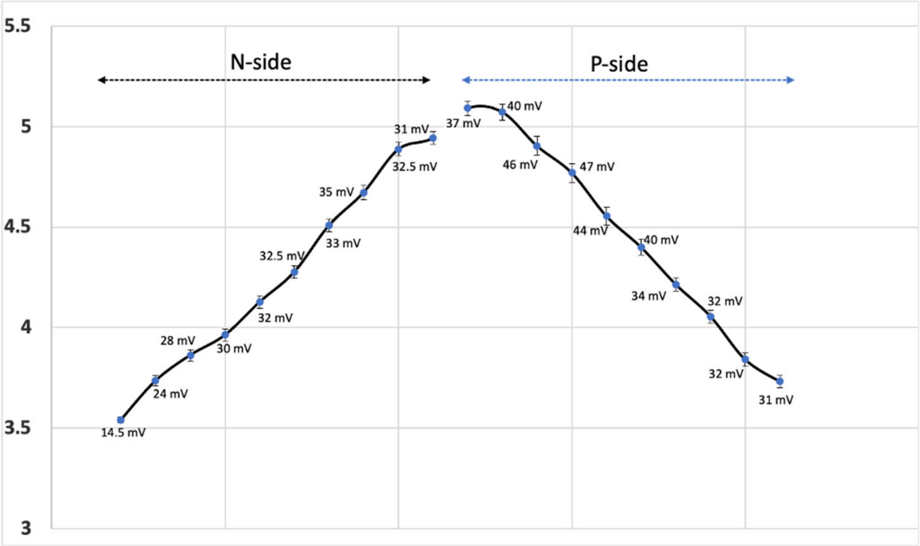


FIGURE 4. Repeatability Data for Carrier Concentration in Staircase Sample. Carrier levels are from 1E15 to 1E20 a/cm^3 for n & p type dopants. The sMIM signal is in volts.

CONCLUSION

Scanning Microwave Impedance Microscopy offers a non-invasive fast way to make electrical property measurements of material and systems. The response of the sMIM signal to carrier concentration and dielectric constant is log-linear and this lends itself easily to quantification of the measurement. We present here the first ever automated quantification of carrier concentration using sMIM. Using the newly developed quantification hardware and software, measurements with a repeatability better than one tenth of a decade of carrier concentration is demonstrated. The next electrical property of materials to be quantified is dielectric constant (k-value).

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KEYWORDS

SPM, AFM, sMIM, Semiconductors, Dopant Concentration, Carrier Concentration, Dielectric Constant, k-value.

A Correlative Metrology Flow for Grains Analysis in Poly-Si Vertical Channel of 3D NAND Architectures

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INTRODUCTION

Here, we report on the integration of a corelative metrology flow that merges transmission electron microscopy (TEM) with 2D and 3D-based scanning probe microscopy (SPM), here used also as data provider in simulations. First, we study the grain structure of vertical Poly-Si channels by a combination of 2D SPM and in-plane TEM. Second, we use a multi-probe sensing scheme implemented in a novel tool for the execution of 3D SPM, (i.e., scalpel SPM) and generate tomographic information of the conductive properties. The high spatial resolution of conductive atomic force microscopy (C-AFM) with the 3D sensing capability offered by the concept of scalpel SPM, we determine the individual size of conductive grains inside the channel, while imaging the 3D network formed inside the channel for hundreds of nm in the z dimension. Finally, both types of information are combined feeding our 3D TCAD framework of simulation for the generation of multiple figures of merit of the memory cell.

RESULTS AND DISCUSSIONS

The structure used in this work replicates a vertical poly-Si channel for 3D NAND based on a macaroni geometry (Fig. 1a,b).[1] The test vehicle is a dense array of hollow poly-silicon tubes, embedded in oxide. The outer device diameter is 80 nm, the poly-Si width is 11 nm, and the channel height is 300 nm. After the poly-silicon is formed the remaining space is filled with SiO_2, thus creating a structure where the poly-Si is entirely embedded within SiO_2 (Fig. 2a). The vertical channel-holes are clearly visible with top-view SEM (Fig. 2b) and atomic force microscopy (AFM) providing surface sensitive information (Fig. 2c). For the sake of simplicity our structures do not have source/drain contacts and gates. However, the electrical characteristics (I_D-V_G and I_G-V_G) are shown in Fig. 3 obtained from a fully-fabricated device based on the same channel material. By leveraging the presence of SiO_2 on all the sides of our vertical pillars we etch away the oxide through a wet etch (buffered HF at room temperature) and inspect the vertical poly-Si channel with the SEM, thus showing the poly-crystalline structure as in Fig. 4. Previous works have shown the impact of poly-crystalline nature, presence of interface and oxide traps in the drive current and reliability.[2,4] *In-plane grain analysis merging TEM with SPM.*

Fig. 5a shows the procedure to thin down the sample and make it electron transparent for in-plane TEM inspection. The results are visible in Fig. 5b-e, where TEM is applied to for the identification of poly-Si crystalline grains with high resolution. Structural information about the grains size and local density is accessible as in Fig. 5c,f, with visible grains in range 12-15 nm lateral dimensions. Although this is a clear method for the direct observation of structural information on the vertical channel, TEM alone does not provide any direct information about the conductive properties of the area under study. For detailed 2D-observation of conductive properties in the poly-Si grains, we use C-AFM to sense the current flowing in the tip-sample system. Fig. 6 shows the schematic of the series of resistance that constitute the virtual circuit seen by the scanning probe on the poly-crystalline channel. By probing the local conductive variation at the tip-sample junctions, the individual contribution of grains to the channel conduction becomes visible. The results are shown in Fig. 7 where individual grains in the macaroni channel can be clearly identified. Using this method we can achieve high lateral resolution on the individual channel in multiple locations, as visible in Fig. 7. Statistic information on grains size in 2D can be collected also in large area (i.e., up to 5 x 5 μm^2). In Fig. 8 the distribution of the grain size is reported, plotting the equivalent radius of grains approximated as sphere objects. In Fig. 9 we show the correlation between grain size and the current flowing in the tip-sample junction at the level of individual grain. This adds information to Fig. 8 by adding a method to interpret the presence of outliers in which large grains are carrying low current and vice versa. It must be clarified that the tip-sample current sampling should be considered different in every pixel of the raster maps (Fig. 9), as such the integral of the current flowing in the 2D map would be representative of the current density in the working device.

A. *3D tomographic observation*

As previously demonstrated the results of Fig. 8,9 can be extended to the third dimension in the vertical channel by applying a slice-and-view methodology.[5] This is used here to extract local conductive information of the grains composing the vertical channel in correspondence of the scanning probe (Fig. 10). To enable that, the sensing probe should be alternated with a diamond probe for material removal, in a concept often referred to as Scalpel SPM (as in Fig. 10). Recently, to eliminate the need for manual probe replacement while enabling the rapid acquisition of statistically relevant datasets we developed a dedicated multi-probe tool, named RPM3D.[5] This leverages the use of three independent probes alternating their operation on the same area of the sample surface, currently providing a solid baseline for interlaced high data acquisition rate and an interferometric detection system providing sub nanometer spatial accuracy. Note that our method offers a straightforward way to alternate two probes in the same area, i.e., one for removal and one for sensing, thus implementing a multi-probes 3D tomographic method. In case of the structures in Fig. 10, we slice in a controlled manner through the vertical channel, removing material with a rate of a few nm/scan for a total depth of 180 nm. A partial set of the acquired 2D conductive profiles (raw data) with material removal down to 2nm/scan is used to collect 75+ current maps of our sample at different heights. Once the entire set of C-AFM slices is acquired, a process of off-line interpolation is used to reconstruct in 3D the tomogram as visible in Fig. 11 (tomogram). Note that the technique is destructive leaving behind a crater in the area under study. Fig. 11 shows the enhanced conductivity of poly-Si as a reconstructed current tomogram (showing various axials projections). A transparency threshold is applied to the data-scale in order to highlight the presence of conductive features in the poly-Si. Similarly, the high resistive values associated with SiO_2 are made transparent. As described in Fig. 7-9 information acquired in our 2D profiles can be considered as a local map at plane z for the overall resistance of the path formed under the probe. Therefore, the reconstruction of these maps in 3D can be considered as proxy for the off-state (un-gated) device percolative current network.

B. *Input for 3D TCAD model*

The combined information available through TEM and Scalpel SPM can be used as input for a dedicated 3D TCAD approach for 3D NAND.[2,4] In the model, the poly-Si channel is reproduced through a randomly generated grain structure, while increased scattering at the grain boundaries is considered by locally reducing the carrier velocity. This results in a percolative current profile that is highly dependent on the assumed grain size, both in terms of the current density value and the spread (Fig. 12). With our metrology method, the grain information in Fig.8 can be directly imported into the TCAD model as in Fig.12. Note that the grain size and the associated 3D percolative paths are among the most important parameters for a detailed simulation of cell behavior. These were generally introduced as a fitting parameter in the past, while this work shows a new method for their direct measurement. In addition, we provide a pathway for the visualization of the percolation behavior, this was previously only a simulated information, while it can be now inspected in detail by sectioning and thresholding (Fig. 14). Finally, it is worth mentioning that other modes (beyond C-AFM) can be alternated in our analysis flow, including contact and non-contact electrical AFMs. An example is reported in Fig. 15 where we apply to our test vehicle scanning capacitance microscopy (SCM) that is sensitive to dopant type and doping level, but any other techniques in the scanning probes constellation can be used thus making our approach flexible toward a wide set of materials information inside the 3D NAND channel.

In conclusion, a correlative analysis work is reported to study structural and electrical properties of vertical poly-Si channel for 3D NAND application where in-plane TEM is combined with a dedicated 3D tomographic probing methodology for grains conductivity that provide data to a 3D TCAD simulation flow.

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II. KEYWORDS

Scalpel SPM, 3D metrology, 3D NAND characterization, RPM-3D

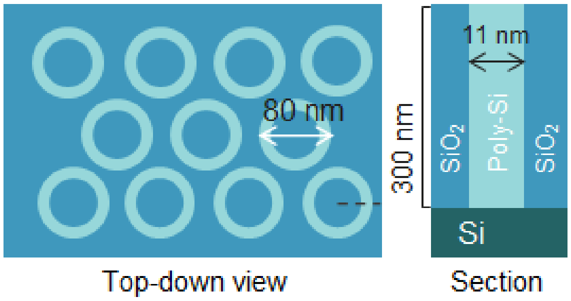

Fig. 1 Schematic of the investigated structure for vertical poly-Si channel 3D NAND devices. A dense array of vertical poly-Si channels is embedded into SiO$_2$ enabling a robust test-vehicle for the analysis of percolative current behavior in these structures.

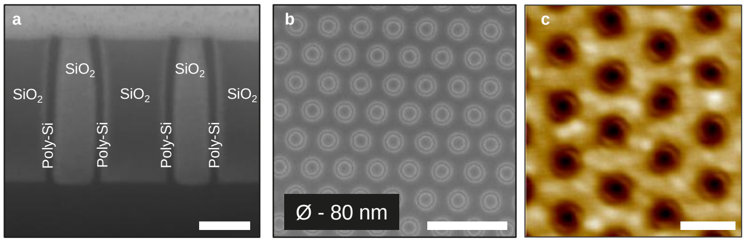

Fig. 2 Cross-section (a) scalebar 80 nm, and top-view (b) SEM images of the vertical poly-Si channel 3D NAND devices (scalebar 200 nm). The vertical channel-holes are clearly visible with 11 nm thick poly-Si . (c) The holes array is inspected with AFM for details on the surface morphology (scalebar 100 nm and z-scale 2 nm).

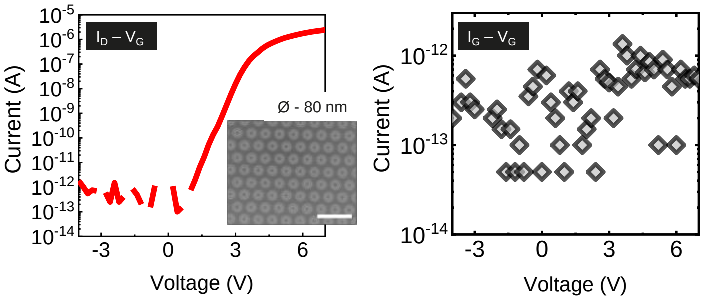

Fig. 3 Fully-functional devices are fabricated using the same channel material reported in Fig. 1,2. Typical I_D-V_G trace (a) and (b) I_G-V_G are reported.

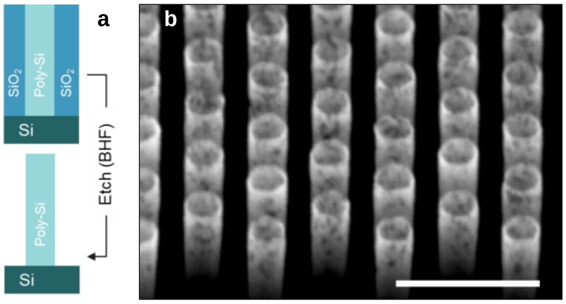

Fig. 4 (a) Schematic of the etching procedure to expose the poly-Si channels. (b) The SEM inspection shows the granularity source of scattering in the grain boundary and change in crystal orientation.

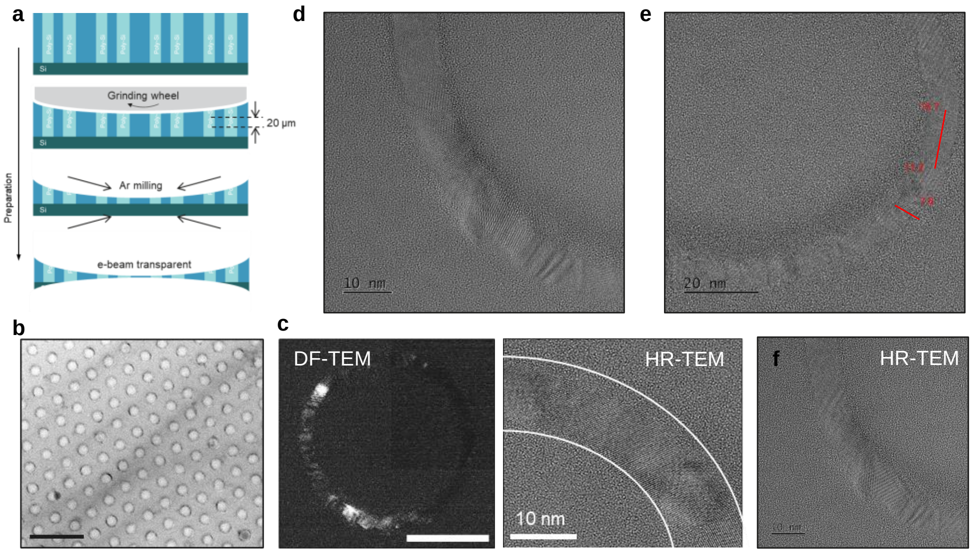

Fig. 5 (a) Schematic of the in-plane TEM sample preparation. (b) Top-view TEM in the area of interest (large field-of-view). (b) DF-TEM of individual memory hole, with contrast variation induced by local density variation in the poly-Si. (c-d) High-resolution (HR)-TEM for the poly-Si channel, with details on individual grain analysis and structural information. (e-f) Internal white bands are added to guide the eyes in the regions of interest.

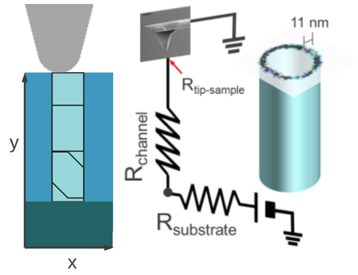

Fig. 6 (a) Schematic of C-AFM analysis performed on the poly-Si channel. The inset shows the series of resistance and biasing conditions with a 2D conductive profile collected on top of the poly-Si channel.

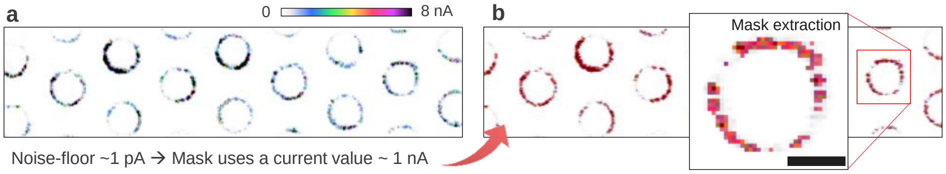

Fig. 7 Planar C-AFM current maps in macaroni channel devices. (a) The conductivity of the poly-Si is visible with fluctuations induced by the local variation of the tip-sample junction resistance. (b) The 2D profiles are masked for the extraction of quantitative information in regions of higher conductivity (red), scalebar 40 nm

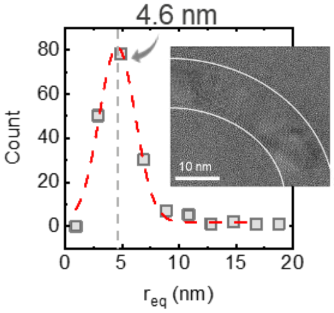

Fig. 8 Using the information of masked C-AFM dataset (Fig. 7) we plot the grains size distribution in the area of interest, approximating the grains to round objects with Req. equivalent radius.

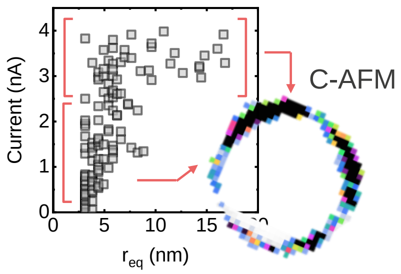

Fig. 9 Beyond grain size our dataset contains electrical information, thus allowing to plot the correlation between grain size and current sensed in correspondence of each grain. In the inset, a 2D C-AFM profile is reported to show the variations observed.

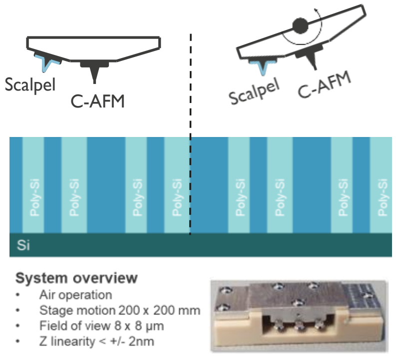

Fig. 10 Schematic of the operations with the RPM3D. Two probes can be alternated on the same area of the sample to perform a slice-and-view sensing scheme i.e., Scalpel SPM. In the inset optical image of the tip holder.

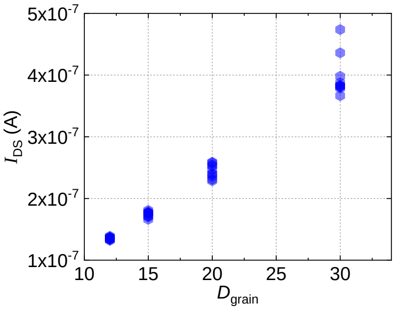

Fig. 12. Simulated drive current obtained for different grains size, obtained with 0.1 V as drain-source bias to match analysis conditions.

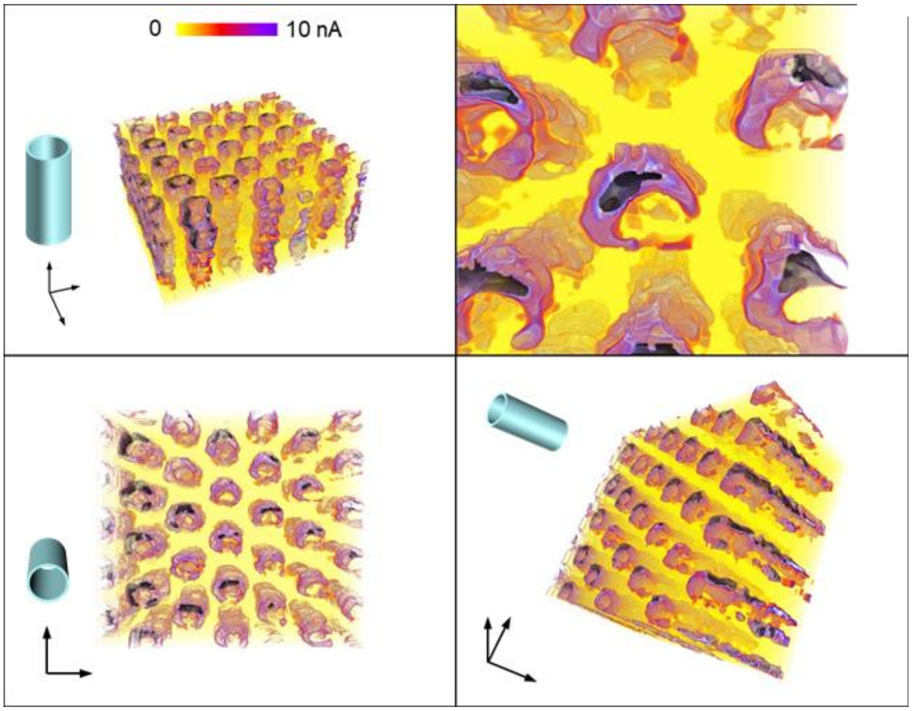

Fig. 11 Scalpel SPM results obtained in a 1 x 1µm^2 axonometric view. Tomographic reconstruction of the poly-Si memory cell visualized by volume rendering in double cross-section (axes according to inset). We filter the tomogram to suppress the high current contribution thus revealing the network of GBs inside the poly-Si channel (iso-surface at fixed threshold green shape).

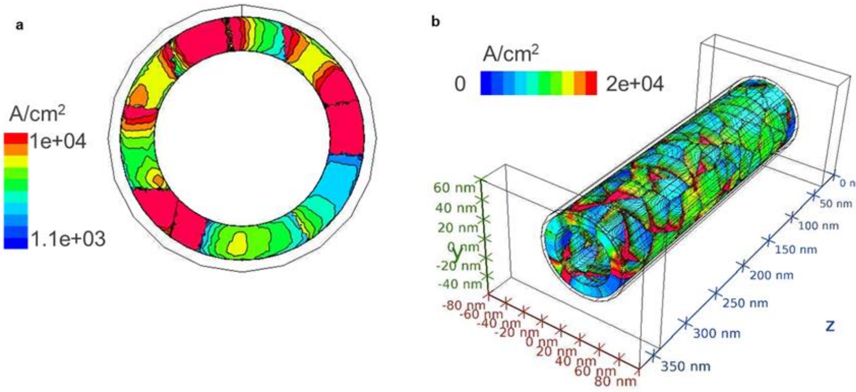

Fig. 13 3D TCAD model using experimental grain information as input. (a) Simulated cross-section view and (b), 3D simulation of the current density in the channel region of the device. Note, for the sake of simplicity simulations are performed without trap charge impact (also available in our model).

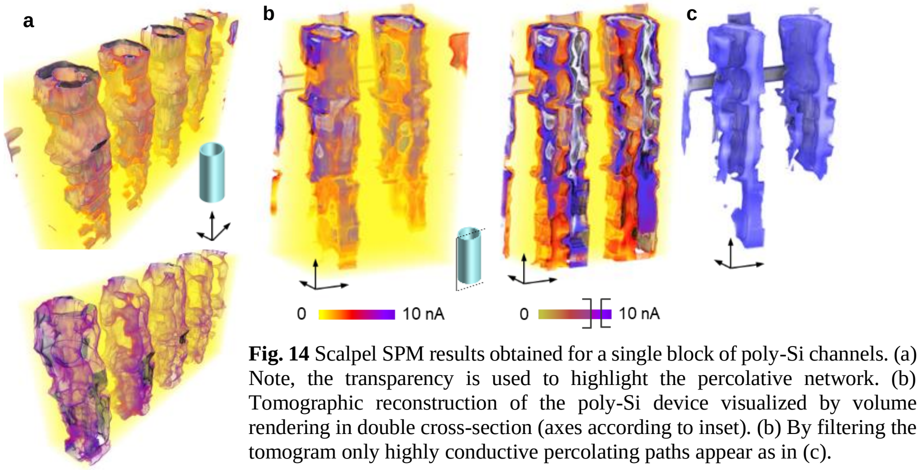

Fig. 14 Scalpel SPM results obtained for a single block of poly-Si channels. (a) Note, the transparency is used to highlight the percolative network. (b) Tomographic reconstruction of the poly-Si device visualized by volume rendering in double cross-section (axes according to inset). (b) By filtering the tomogram only highly conductive percolating paths appear as in (c).

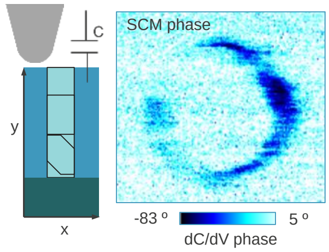

Fig. 15 Schematics of SCM mode applied to the 3D NAND structures in this work. A exemplary SCM phase channel is also shown, here the dC/dV phase is sensitive to dopant type and concentration.

Dopant Activation Evaluation in Si:P by Scanning Spreading Resistance Microscopy and Differential Hall Effect Metrology

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INTRODUCTION

Heavily n-doped epitaxially grown Si layers are of great importance for source/drain (S/D) application in advanced node nMOS devices. Introduction of ultra high concentration of P into Si and formation of Si:P helps reducing the S/D ohmic contact resistivity and induces the needed strain into the channel. For contact resistivity reduction, the dopant activation level is more important than the high dopant amount. Various techniques are being used to evaluate dopant activation in Si:P layers. Among these two methods are Scanning Spreading Resistance Microscopy (SSRM) [1][2] and Differential Hall Effect Metrology (DHEM) [3][4].

Commonly used to study incorporation, diffusion, and activation processes of dopants in semiconductor devices, SSRM uses an atomic force microscope equipped with a hard conductive probe that is scanned in contact mode on the cross-sectioned sample's surface. Simultaneously a DC bias is applied to the sample and the total resistance is measured using a logarithmic amplifier. The use of a logarithmic amplifier allows the sensing of a wide range of resistance values (10Ω - 1GΩ) enabling to resolve nearly the entire range of relevant carrier concentrations in doped semiconductor samples. The current fed into the logarithmic amplifier is determined by the total resistance (load) of the tip-sample system. Particularly for Si, when a sufficiently high force is applied (> μN) a local phase transformation occurs, and a β-Sn pocket is induced by the high pressure in the Si underneath the tip. In that case spreading resistance is the resistance of the Schottky-contact located between the semiconductor substrate and this pocket [2]. Measured resistance values as a function of depth are converted into resistivity and carrier concentration depth profiles using calibration measurements and conversion relationships.

DHEM provides depth profiles of mobility, resistivity and carrier concentration through a semiconductor layer by making successive sheet resistance (R_s) and Hall voltage measurements using Hall effect/Van der Pauw techniques, as the electrically active thickness of the layer is reduced through successive oxidation steps. Controlled oxidation is achieved by electrochemical anodization in presence of a specially formulated electrolyte. In a DHEM measurement, first a cross-shaped Van der Pauw test-pattern is prepared on the sample to be characterized. The cross has a mesa structure isolating the top film to be characterized from the surrounding portion of the layer. Measurement is typically carried out on p-type films formed over n-type substrates, or n-type films formed over p-type substrates, so that the p-n junction underneath isolates the top film from the substrate. Four electrical contacts are formed at the ends of the four arms of the cross-shaped test-pattern and the nozzle of a small process chamber comprising a cathode is sealed against a process area that includes a test region at the center of the test-pattern, where the four cross arms meet. The nozzle has the capability of delivering an oxidation electrolyte, deionized (DI)water and nitrogen gas to the process area and the test region. Through electrochemical oxidation the electrically active thickness of the layer at the test region is reduced in a highly controlled stepwise manner and measurements of R_s and Hall voltage are carried out after each thickness reduction step. Data collected can then be processed to yield depth profiles of resistivity, mobility, and carrier concentration. In this contribution we have carried out SSRM and DHEM measurements on Si:P epi layers subjected to different processing conditions to study the effects of such conditions on dopant activation and to compare the results from the two techniques.

EXPERIMENTAL DETAILS

In-situ phosphorus (P) doped Si epi-layers were grown over two sets of 300mm diameter boron doped monitor wafers. While one set was kept as the reference, the other set was treated by a spike-annealing process at 1000 °C. In the data presented below, sample D02 represents the wafer with the as-deposited Si:P epi layer, which was about 45nm thick. Sample D03, with about 53nm thick epi-layer, was the wafer subjected to the annealing process. Bulk sheet resistance measurements were made using 4-point probe (4PP). SSRM measurements were carried out at IMEC with a probe that was calibrated using an n-type Si staircase structure with doping ranging from 1.65E16/cm^3 to 1.16E20/cm^3, as determined by SRP. Cross-shaped Van der Pauw test-patterns were formed on 8mmx8mm areas on the samples. DHEM measurements were performed at ALP, employing an ALPro^{TM}100 electrical property depth profiler tool, which was also used to determine the bulk R_s and mobility values. All measurements were carried out in accordance with ASTM Standards [5]. Secondary Ion Mass Spectrometry (SIMS) was used to measure the total dopant profiles through the films.

RESULTS AND DISCUSSION

For sample D02, the bulk R_s and bulk mobility values measured by the ALPro^{TM} 100 tool were 138.3 Ω/ and 57.9 cm^2/V-sec, respectively. The corresponding values for sample D03 were 63.5 Ω/ and 37.4 cm^2/V-sec. Therefore, bulk measurements showed lower sheet resistance and mobility for the annealed sample. Figure 1 shows the dopant depth profiles obtained by SIMS and the carrier concentration profiles from DHEM and SSRM techniques for samples D02 and D03. One can make some general observations from the data in this figure. Dopant concentration from SIMS is ~ 1.4E21/cm^3. There is only a small difference in the dopant distribution profiles between the as deposited sample (D02) and the spike annealed sample (D03). Despite the fact that the SIMS profiles are similar, however, the spike annealed sample shows much higher dopant activation as measured by DHEM. Carrier concentration is ~2.5x higher in sample D03 (~5E20/cm^3) compared to sample D02 (~2E20/cm^3). Activation levels measured by SSRM, however, are lower for both samples, and the peak carrier concentration value increases only slightly upon spike annealing, going from ~2E20/cm^3 in sample D02 to ~2.2E20/cm^3 in sample D03. DHEM clearly indicates the sharp interface between the p-type substrate and the n-type epi-layer and its depth calibration agrees well with the expected thicknesses of the epi layers. The tail of the SSRM data is much more graded.

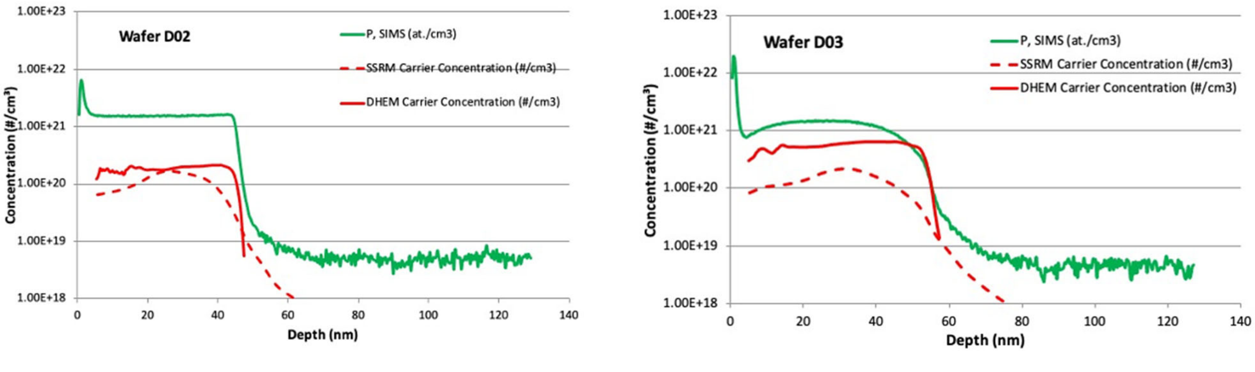

FIGURE 1. SIMS total dopant, and SSRM and DHEM carrier concentration depth profiles for samples D02 and D03.

Mobility depth profiles for the two samples were also obtained by DHEM. As can be seen from the data shown in Figure 2, the mobility value for sample D02 is in the 50-60 cm^2/V-sec range, whereas it is in the range of 30-40 cm^2/V-sec for sample D03. This is an expected result since D03 sample was annealed and activated and displayed higher carrier concentration values as seen in Figure 1.

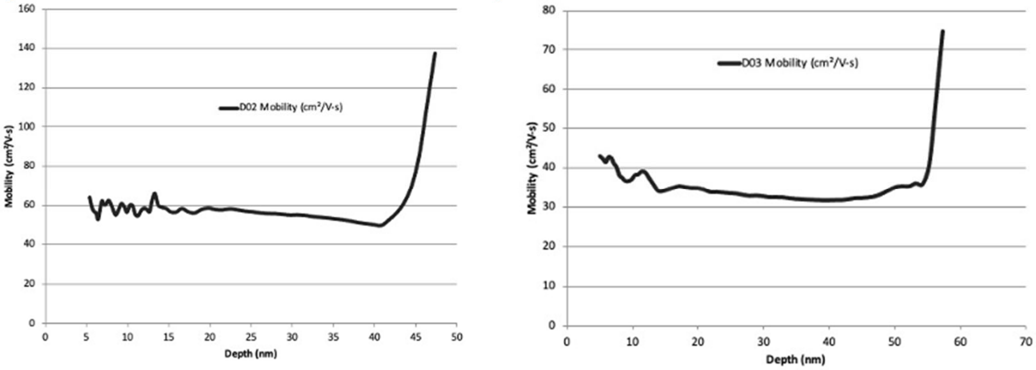

FIGURE 2. Mobility depth profiles obtained by DHEM for samples D02 and D03.

To better understand the appreciable differences observed in the carrier concentration depth profiles provided by DHEM and SSRM techniques we calculated the bulk R_s values for the two samples. These calculations, along with the bulk R_s values obtained from the four-point probe (4PP) measurements and from the ALPro™ 100 DHEM system are given in Table1. It should be noted that for DHEM calculations, the carrier concentration profiles and the mobility profiles were used for integration. As can be seen from this data the bulk R_s measurements from 4PP and DHEM system agree very well. One can conclude that SSRM underestimated the carrier concentration values in these doped epi layers. DHEM measurements provided consistent results.

TABLE 1. Measured and calculated bulk values of sheet resistance for the two samples characterized.

SAMPLE No	Measured R_s (Ω/) 4PP	Measured R_s (Ω/) DHEM	Calculated R_s (Ω/) DHEM
D02	136	138.3	139
D03	62	63.5	65.1

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KEYWORDS

SSRM, DHEM, dopant activation, depth profile, differential hall effect metrology, scanning spreading resistance microscopy.

Comparison of Dopant Activation in Si as Characterized by Spreading Resistance Profiling (SRP) and Differential Hall Effect Metrology (DHEM)

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INTRODUCTION

Advanced devices employ ever shrinking source/drain (S/D) junction depths, which bring along high parasitic resistance challenges. Therefore, doping/annealing/activation processes are being developed to reduce contact resistivity. Prediction of contact resistivity and device performance require a knowledge of the exact location and activation of dopant species in the junction area of such structures. As a result, the need for techniques that offer high depth resolution and accuracy for profiling carriers through ultra-thin layers has been increasing.

There are various techniques for depth profiling electrical properties of semiconductors. SRP is a two-probe spreading resistance measurement approach that has been widely used for this purpose [1]. To obtain a carrier concentration depth profile using SRP, the sample is polished and beveled at low angle (<0.5° for very shallow junctions) to expose the junction. The two probes are then stepped along the beveled surface and the collected data is interpreted to find the spreading resistance values. These are then translated into resistivity using relationships established through calibration. Finally, carrier concentrations are calculated using models providing resistivity-carrier concentration relationships [2]. DHEM is a more direct method that provides resistivity, mobility, and carrier concentration depth profiles at sub-nm resolution [3, 4]. The method employs electrochemical means to reduce the thickness of a semiconductor film at a test site at the center of a cross-shaped test pattern, and determines the sheet resistance and Hall voltage values for the thinned down layer using Van der Pauw/Hall effect measurements. Data collected can then be interpreted and depth profiles may be plotted after repeating the thinning and measuring cycles numerous times. In this contribution, we are comparing the data obtained from two depth profiling methods described above for a shallow and an-ultra shallow junction formed through ion implantation.

EXPERIMENTAL DETAILS

Two sets of samples were prepared for characterization. For one set, an n-type Si substrate (2-7 Ω-cm) was implanted with $^{11}BF_2^+$ species with energy ~ 10keV, dose ~2E15 #/cm^2, tilt ~7° and twist ~22° using a Varian EHP-500 system. The second set employed a p-type Si substrate (15-25 Ω-cm) that received $^{75}As^+$ implantation under similar conditions. After implantation, a photolithography/dry etch process sequence was performed on a selected region of the wafers to fabricate cross-shaped test patterns [4]. Wafers were then cut into small pieces and two different annealing methods were used for activation. The B implanted samples were subjected to an RTA process at 950 °C in a nitrogen atmosphere for 30 seconds. The As implanted samples received a CO_2 laser anneal step in air, at a power level of 130W (0.72 J/cm^2). After annealing, samples with the test patterns went through another photolithography step to open contact pads at the ends of the cross arms. Ti/Al contacts were formed through E-beam evaporation followed by resist lift off. DHEM measurements employed the cross patterned samples with metal contacts. Depth profile data was collected at ~1.5 nm deep increments. Blanket wafer pieces without the cross patterns were used for SRP measurements after beveling at an angle ~0.09°. Data was collected with 2.5 grams of force on the SRP probes.

RESULTS AND DISCUSSION

Fig. 1 shows the cross-sectional TEMs of the samples before and after the annealing steps. As can be seen from this data, implantation created about 17-18 nm thick amorphized region at the surface of the B doped sample with prominent end-of-range (EOR) defects at the a-Si/Si interface. After the 950 °C RTA step, the EOR defects were mostly dissolved and the surface region was crystallized. As for the As implanted sample, the amorphized region is about 21-22 nm thick and the laser annealing step did not eliminate the defects, an observation suggesting that annealing/activation was largely limited to the top 20-25 nm of the surface region.

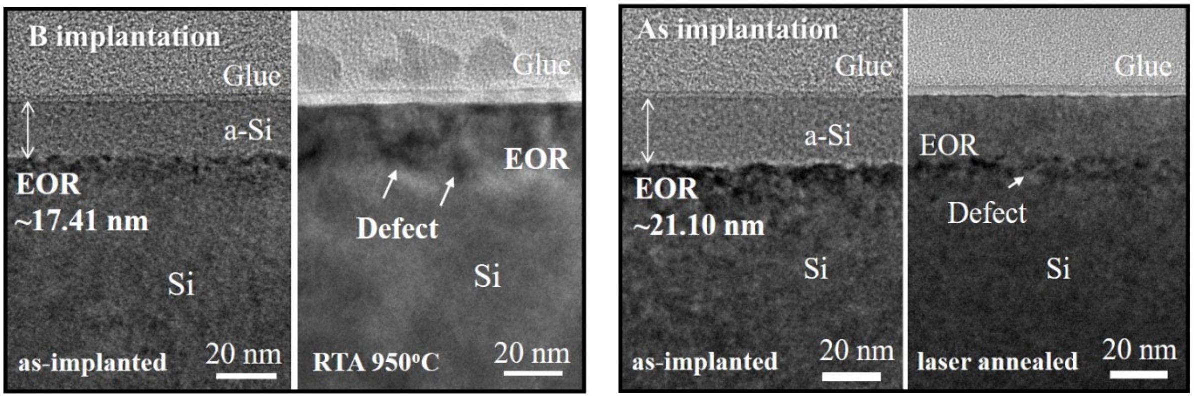

FIGURE 1. TEM cross-sections for the B implanted sample before and after RTA anneal (on the left); and for the As implanted sample before and after laser anneal (on the right).

The SRP and DHEM carrier concentration depth profiles of the annealed samples are shown in Fig. 2. DHEM data shows a deeper dopant activation level for the RTA annealed sample ($10^{19}/cm^3$ carriers at ~50nm depth) compared to the laser annealed sample ($10^{19}/cm^3$ carriers at ~26nm depth). This is in line with the fact that laser annealing deposits much of its energy close to the surface forming an ultra-shallow junction. It also agrees with the TEM data that shows recrystallization being limited to the top 20-25nm thick region. One other observation from the DHEM data is the fact that the peak activation for As is quite high within the top 5nm region for the laser annealed sample. For the B doped and RTA annealed sample, SRP suggests much lower activation compared to DHEM, discrepancy being the largest within the top 20nm of the surface. Carrier concentration values measured by DHEM is almost an order of magnitude larger in this region. Deeper into the junction, agreement between DHEM and SRP is better although the SRP carrier concentration values are still lower. For the As doped and laser annealed samples, disagreement between the SRP and DHEM data is much larger. Here, the SRP carrier concentration values are lower than those measured by DHEM within the first ~21nm deep section, however, they exceed the DHEM values deeper into the structure. Furthermore, the electrical type of the top layer given by the SRP tool was p-type for this sample despite the fact that it was As doped.

SRP has been successfully used in the industry for studying deep junctions. However, as the junction depth gets smaller and smaller SRP resolution gets reduced by artifacts such as carrier spilling, surface states, and increasing correction factors [5]. Extensive calibration procedures required are also potential error centers for this technique. For DHEM the most important calibration involves determination of the thickness of the anodic oxide formed at each oxidation step and its conversion into Si thickness used to form the oxide (depth calibration) [3]. It has been demonstrated that sub-nm depth control is possible in DHEM, which makes it an excellent method for ultra-shallow junction measurements as well as for evaluation of activation right near the surface, where SRP generally fails to resolve.

To further evaluate the data in Fig. 2, calculations were carried out to derive the bulk sheet resistance (R_s) values and to compare them with the measured values. These results are summarized in Table 1. The bulk R_s values for the two samples were measured using the cross-shaped test patterns and employing the Van der Pauw technique. The effective bulk mobilities were also measured by Hall effect and they were found to be 40 and 34 cm^2/V-sec for the B doped and As doped samples, respectively.

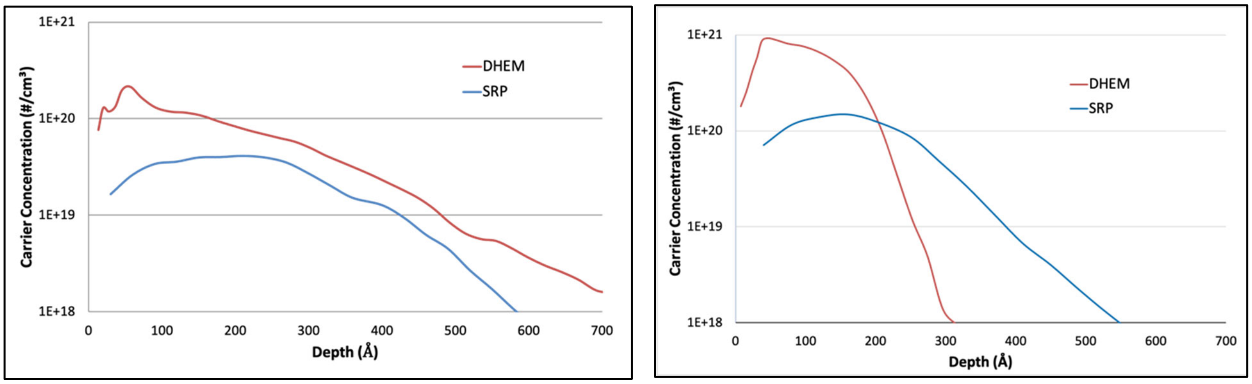

FIGURE 2. Carrier concentration depth profiles obtained from the B implanted and RTA annealed sample (left) and As implanted and laser annealed sample (right) using SRP and DHEM techniques.

As can be seen from Table 1, the bulk R_s values measured for both samples agree well with the values obtained from the DHEM data by using the mobility depth profiles measured and integrating through the thickness of the samples. R_s calculations for the SRP data employed the resistivity depth profiles corresponding to the SRP data plotted in Fig. 2. Integration yielded values that were much higher than the measured bulk values for both samples. This is a clear indication that SRP greatly underestimated the activation levels of the shallow and ultra-shallow structures used in this study.

TABLE 1. Measured and calculated bulk sheet resistance (R_s Ω/) values for the B doped and As doped samples.

Sample	R_s bulk measured By Van der Pauw	R_s calculated by Integrating DHEM data	R_s calculated by integrating SRP data
B doped + RTA	362.8	368.8	840.5
As doped + laser anneal	198.4	207.9	355.2

CONCLUSION

SRP measurements of carrier concentration depth profiles underestimated the near-surface dopant activation, whereas DHEM provided dependable results for the 20-70nm junctions measured in this study. The sharp variation in the carrier concentration profile tail for the ultra shallow junction was also properly resolved by DHEM, whereas SRP was found to be inadequate for this measurement. Comparison of the measured and calculated bulk sheet resistance values for both samples demonstrated the reliability of the DHEM measurements.

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KEYWORDS

Spreading Resistance Profiling, SRP, Differential Hall Effect Metrology, DHEM, Depth Profiling, Dopant Activation

IMPROVED GEOMETRICAL CORRECTION IN MICRO FOUR-POINT PROBE MEASUREMENTS WITH THREE OMEGA CORRECTION

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INTRODUCTION

Micro four-point probe (M4PP) metrology with lock-in technique is routinely used in high-resolution mapping of electrical properties of a broad category of materials[1]. The accuracy of M4PP measurements depends on many factors, e.g. sample type, probe pitch [2], self-heating, etc. One of the key factors for achieving accurate measurements is electrode position; when electrodes get in contact with the probed surface, their actual positions might differ from their nominal values, potentially introducing measurement errors [3]. In multi-cantilever (>4) collinear probes, where electrodes are spaced along one dimension, it has been shown that electrode position errors can be eliminated by exhaustive sub-sampling of 4-point configurations, and minimization of observed vs. model resistances [3,4,5,6,8]. However, position errors due to joule heating of probe or sample has not been previously addressed. Here we demonstrate how the recently introduced 3ω correction of measured resistance [7] can significantly reduce in-line position errors using a multi-cantilever sampling approach and fitting algorithm in bulk and thin film samples.

THEORY

In a four-point probe measurement, an electric current I is forced through two electrodes located at $\mathbf{r}_3$ and $\mathbf{r}_4$, while the potential difference ΔV is recorded between the other two electrodes located at $\mathbf{r}_1$ and $\mathbf{r}_2$. The measured potential difference when the four electrodes are in contact with a bulk sample is given by:

$$\Delta V(\mathbf{r}_1, \mathbf{r}_2, \mathbf{r}_3, \mathbf{r}_4) = \frac{\rho I}{2\pi}\left(\frac{1}{|\mathbf{r}_1-\mathbf{r}_3|} - \frac{1}{|\mathbf{r}_1-\mathbf{r}_4|} - \frac{1}{|\mathbf{r}_2-\mathbf{r}_3|} + \frac{1}{|\mathbf{r}_2-\mathbf{r}_4|}\right) \qquad 1$$

where ρ is sample resistivity. A multi-cantilever sampling procedure, where M4PP resistance is measured for different 4-electrode subsets of the available electrodes, yields an overdetermined dataset with respect to electrode positions, enabling the latter to be regressed using standard procedures [8]. However, Joule heating of the sample cause by the probe current can have a percent-level influence on the first harmonic resistance [7]. Here, we extend the approach of Ref. [8] to improve the determination of electrode positions in situations where Joule heating effects may be considerable. Based on [8], we define the model misfit as:

$$\chi^2 = \sum_{i=1}^{N} \left(R_{i,\mathrm{mod}}(\rho, X, \beta_i) - R_{i,\mathrm{meas}}\right)^2 \qquad 2$$

where N is the number of measurements, $R_{i,\mathrm{mod}}$ is model resistance (cf. Eq. 1) of the i-th measurement, ρ is regressed sample resistivity, β_i is an index vector of the electrodes used in each configuration, and $X = [X_1, \ldots, X_n]$ is a vector of positions of the n electrodes participating in the electrical measurements. The observed resistance $R_{i,\mathrm{meas}}$ takes the value of the first harmonic resistance $R_{1\omega}$ in case of no thermal correction, and $(R_{1\omega} - 3R_{3\omega})$ if the 3ω correction is applied [7]. With n=8 available electrodes, the number of unique k=4 point sub-samples is $\binom{8}{4} = 70$ which clearly has enough degrees of freedom for regressing ρ and X, to reduce geometrical errors involved in the measurement. Fig.1 shows a scanning electron microscope (SEM) image of the non-equidistant L8PP probe that was simulated [8].

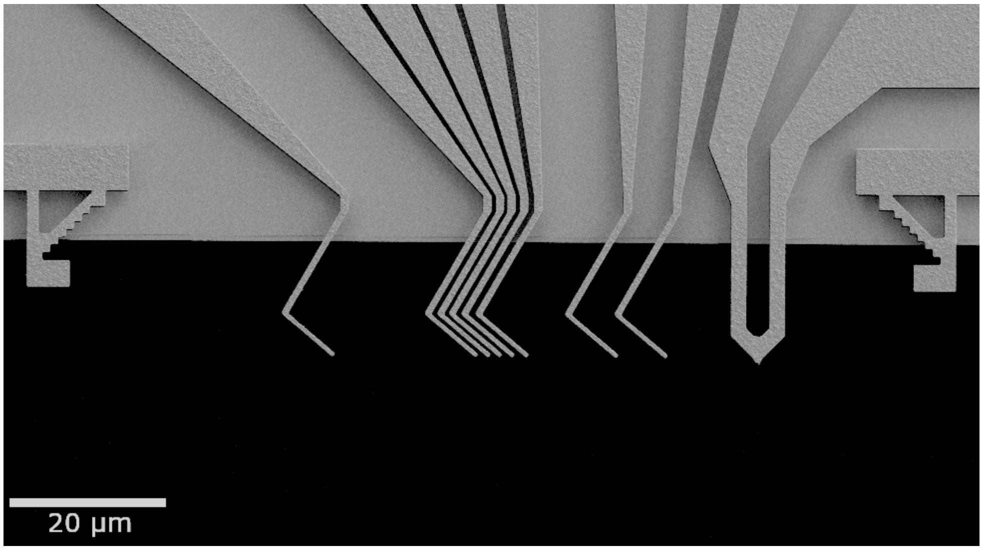

Fig. 1. Scanning electron microscope image of the L8PP probe used. The probe comprises a silicon body with L-shaped cantilever electrodes and a strain gauge (to the right) for surface detection extending beyond the body. Eight electrodes from right to left position X_1 through X_n any sub-set of four can be used for an M4PP measurement (Courtesy: Lior Shiv).

Finite Element Method (FEM) simulations were performed in COMSOL Multiphysics®. For simulations we used boron (B) doped silicon at 300K with the parameters listed in Table 1. We have included both the thermoelectric parameters and the temperature coefficient of resistance (TCR) in the FEM simulations. However, we have implemented linearized resistivity [9] for sample and rest of the parameters remained unchanged with temperature.

Dopant	Resistivity (Ω cm)	Seebeck coefficient (μV K^{-1})	Thermal conductivity (Wm^{-1}K^{-1})	TCR (‰ K^{-1})
Boron	0.0132	632	128.3	0.18

Table 1 List of electrical and thermal parameters (at 300K) of the silicon used for FEM simulation.

We used a large hemispherical bulk substrate with coupled electric currents, heat transfer in solids, and thermoelectric effects. Two terminals of opposite polarity applied a sinusoidal current through two hemispherical contacts (each 30 nm in radius). A time-dependent solver was used to simulate the AC voltage at two observation points (set as point probes), which accounted for the voltage probes of the real measurement. All the four-point configurations were sequentially sampled via a Matlab-COMSOL link. The time-dependent voltage response from each measurement configuration was transformed via a numerical lock-in amplifier into the sought resistance harmonics [7].

RESULTS AND DISCUSSION

The simulated resistances $R_{i,\mathrm{meas}}$ were treated by the multivariable fitting routine that minimizes the error of Eq. (2) and computes the sample resistivity ρ and electrode locations X_2 through X_{n-1} (the positions of the outer electrodes must be fixed in order to fit inner positions [8]). The position offset ΔD of each electrode relative to its nominal position, is shown in Figs. 2a and 2b for four representative currents; with thermally-uncorrected $R_{i,\mathrm{meas}} = R_{1\omega}$ in Fig. 2a, and 3ω corrected $R_{i,\mathrm{meas}} = R_{1\omega} - 3R_{3\omega}$ in Fig. 2b.

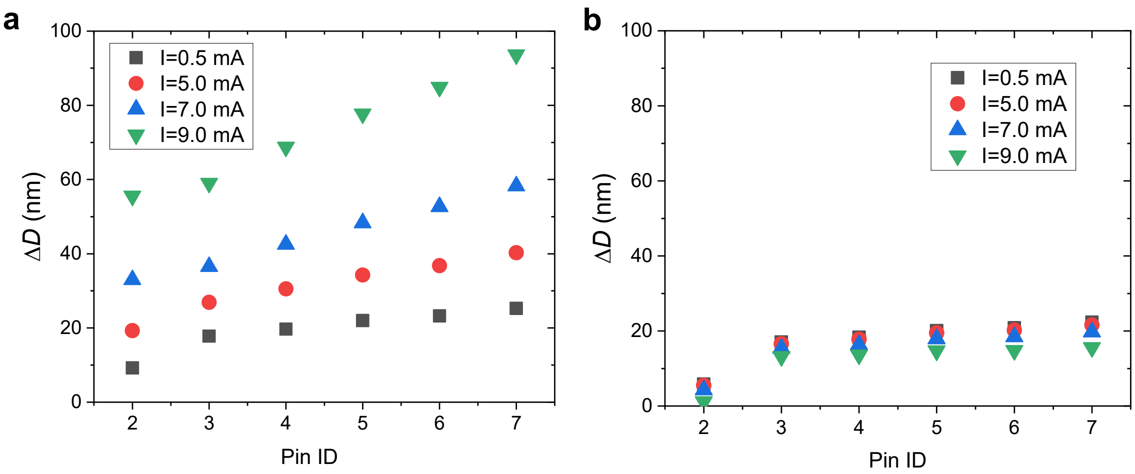

Fig. 2. Offsets of best-fit electrode positions from their nominal values for uncorrected (a), and 3ω-corrected (b) resistances.

It is evident from Fig. 2a that for the uncorrected measurements, the difference between nominal and regressed electrode positions notably increases with applied current. With the 3ω-correction, current dependence is almost entirely removed (Fig. 2b), yielding comparable position uncertainties regardless of the amount of heating. Performing 3ω correction to the first harmonic resistances completely removes effect of TCR and substantially reduce the Peltier effect on apparent electrode positions [7]. A systematic error is observed in Fig. 2b, we believe this is associated with the remained Seebeck/Peltier contribution, which is not possible to correct with 3ω as that signal does not appear at 3ω. In conclusion, we have demonstrated that the 3ω correction leads to an improved accuracy of the regressed electrode positions, which will allow more accurate M4PP measurements.

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KEYWORDS

Micro four-point probe (M4PP), Three omega correction, Joule heating, In-line errors, Electrode pitch.

AKONIS: SIMS Excellence Brought To The Fab

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INTRODUCTION

The new CAMECA AKONIS SIMS tool fills a critical gap in semiconductor fabrication processes by providing high throughput, high precision detection for implant profiles, composition analysis and interfacial data directly in the semiconductor manufacturing line. AKONIS provides a very high level of automation to ensure repeatability across tools for fab level process control and tool-to-tool matching.

Building upon fifty years of experience in ion instrumentation and over thirty years of close partnerships with leading semiconductor manufacturers worldwide, AKONIS is a leap forward in high precision characterization of implants, interfaces and compositional analysis along with high repeatability metrology for the most demanding semiconductor process development and control applications.

AKONIS benefits from recent development in Ultra Low Impact Energy ionic column technology (< 150 eV), coupled with a full wafer handling system including a high-resolution stage enabling measurements on pads down to 20 µm.

ADVANCED AUTOMATION AND EASE OF USE

AKONIS implements sophisticated automation routines on the primary ion column. These allow it to run an analysis at the target current setpoint with a tightly focused beam over a broad range of energies - from 150 eV to 7 keV - for applications from ultra-thin films to deep implants.

Moreover, the instrument enables running automated chain analyses, switching between different applications that may require differing instrument conditions - such as mass resolution, analysis current, or impact energy - without any need for human intervention, as illustrated in Fig. 1. This level of automation ensures that a fab operator can run multiple such instruments, each analyzing varying applications - meeting real-world fab analytical demands. With AKONIS it's possible to commute energy between runs and reach a very good RSD. Fig. 2 displays the RSD of phosphorous implant in SiP with energy commutation between runs (RSD <0.2%)

In addition, fitted with optical carrier enhancement (OCE) capability, the instrument is reliably and easily used for charge compensation while analyzing thin insulating films, a growing market in the semiconductor application space.

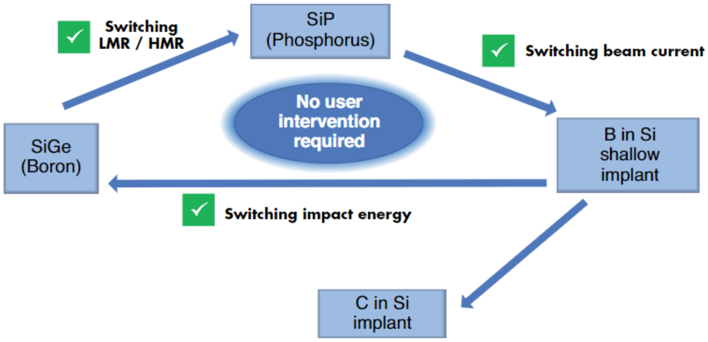

FIGURE 1. AKONIS automated operation scenario shows a) switching between low mass resolution (LMR) and high mass resolution (HMR) recipes, then b) switching beam current to raster on a small pad, and finally c) impact energy switching for a deeper implant profiling

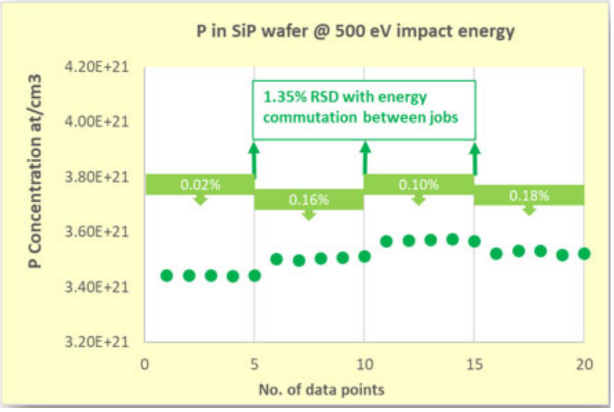

FIGURE 2. RSD of phosphorous implant in SiP with energy commutation between runs (RSD <0.2%)

STATISTICAL PROCESS CONTROL

The number of steps in device fabrication is increasing nonlinearly with each technology node. So, the importance of running each step with maximum repeatability cannot be overemphasized. AKONIS has been designed to respond to this need. It uses a novel ion source, a new ultra-low-energy primary column, and heavy automation of its beam optics to produce a relative standard deviation (RSD) of less than 1% for dose measurement on a broad array of customer applications in fully automated analysis mode. Fig. 3 shows an overlay of 25 B implant profiles, measured on pad craters on 300 mm wafers, in unattended analysis at a throughput-friendly 30 nm/min — all while demonstrating a good detection limit and dynamic range, with a dose repeatability of less than 1%.

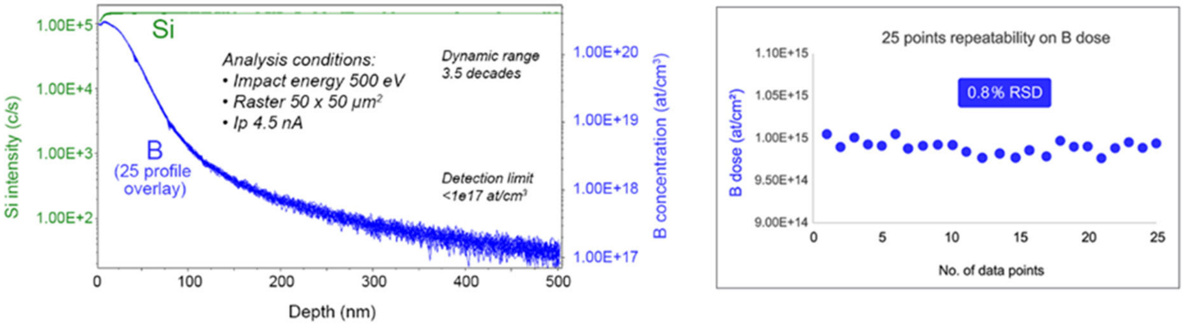

FIGURE 3. Left - Overlay of 25 B implant in Si raw profiles, showing high repeatability with a good detection limit and dynamic range for pad analysis. Right - Dose repeatability over the 25-point profile of B implant in Si, for statistical process control using test pads on pattern wafers. (RSD = relative standard deviation.)

The column of Akonis has been designed to reach very good primary current stability for analysis duration and long term for SPC on applications as shown in Fig. 4.

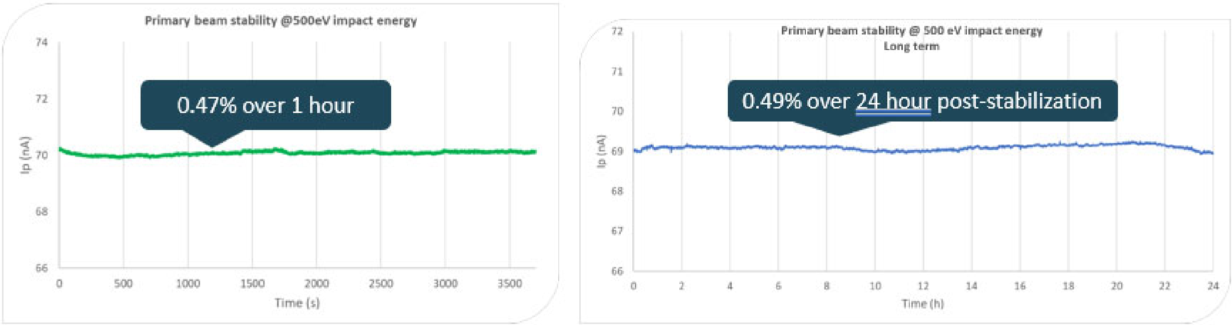

FIGURE 4. Left – Primary beam stability at 500eV impact energy over 1hour (short term stability). Right - Primary beam stability at 500eV impact energy over 24 hours (long term stability)

KEYWORDS

SIMS, High Volume Manufacturing support, Process Control, Automation

Successes and Challenges in Applications of a Laboratory-Based Scanning XPS/HAXPES Instrument

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INTRODUCTION

X-ray Photoelectron Spectroscopy (XPS) is a widely used surface analysis technique with many well-established industrial and research applications, including nanoelectronics. The surface sensitivity (top 5-10 nm) of XPS and its ability to provide short-range chemical bonding information makes the technique extremely popular in the characterization of electronic materials. While its surface sensitivity is an important attribute, in some cases, the depth of analysis of XPS is not sufficient to analyze buried interfaces without first sputtering the sample surface. The interfaces of interest for characterization or metrology are often buried underneath metal electrodes or oxide layers and/or localized in small areas, which has been an increasing challenge for XPS.

An alternative to sputtering the sample is Hard X-ray Photoelectron Spectroscopy (HAXPES) which utilizes X-rays typically defined as having energies greater than 5 keV. By increasing the photon energy of the X-ray source, the mean free path of photoelectrons is increased, resulting in an increased information depth obtained from the sample. Depending on the energy used, these hard X-rays can provide depths of analysis three or more times greater than soft x-rays used on conventional XPS systems.

This paper describes the development and applications of a laboratory-based instrument, the PHI *Quantes*, equipped with two scanning microprobe monochromated X-ray sources, Al Kα (1486.6 eV) and Cr Kα (5414.8 eV), thus enabling both traditional XPS and HAXPES experiments in the same instrument.

ADVANTAGES OF LAB-BASED HAXPES INSTRUMENT

The PHI *Quantes* spectrometer combines a conventional monochromatic soft X-ray source (Aluminum Kα, hν = 1486.6 eV) with a monochromatic X-ray source three times higher in energy (Chromium Kα, hν = 5414.8 eV)[1]. The higher kinetic energy of electrons ejected using a higher-energy X-ray source results in a larger inelastic mean free path (IMFP) of electrons, making the sampling depth from which they can escape larger. For example, the inelastic mean free path for a Si 2p electron is ~ 9.5 nm when the Cr X-ray source is used vs. ~3.3 nm when an Al X-ray is used as the excitation source.

Higher escape depth of photoelectrons offers several advantages:

1. Structural investigations that are not possible with soft Al X-rays. This includes analysis of buried interfaces, such as electronic layers below a surface capping layer and compositional studies in the bulk of materials and interfaces below the sampling depth of soft X-rays.
2. Reduced effect of surface contamination on the photoelectron signal. The relative fraction of the adventitious layer with respect to the total sampling signal for Cr-induced photoelectrons is ~3 times smaller than for Al-induced photoelectrons, resulting in much smaller signal attenuation due to contamination overlayer presence.

3. A deeper sampling depth using the Cr source allows one to probe beyond the depth of possible damage induced by ion sputtering. To take advantage of this benefit, the probing depth of the X-ray source must be deeper than the damage depth of the ion source. Damage depth is strongly dependent on ion beam sputtering parameters and material being analyzed. For commonly used ion beam settings of monatomic Ar^+ at 2-5 kV, the damage depth is on the order of 5-12 nm (higher for a higher energy beam), which is why we detect signs of damage in XPS spectra for ion-beam sensitive materials. For efficient and accurate chemical analysis of buried layers and interfaces, the photoelectrons analyzed must originate from below the ion beam damage depth, thus from depths of ~15 nm or more. A Cr X-ray source is well suited to meet this requirement.

In addition to higher sampling depth, higher primary X-ray source energy provides access to additional higher binding energy transitions**.** Compared to Al Kα, Cr provides access to ~120 more transitions. Additional photoelectron transitions provide complementary chemical information and interpretation. The database of chemical shifts is well tabulated for transitions obtained using Al X-ray sources. A similar chemical state database is needed for higher binding energy transitions, accessible by higher energy sources. Figure 1 shows high-resolution spectra obtained using a Cr X-ray source for three reference materials – pure Al metal[2], Al nitride AlN[3,] and Al oxide Al_2O_3[4]. The chemical shift for the Al 1s transition, now accessible using a Cr source, is obtained.

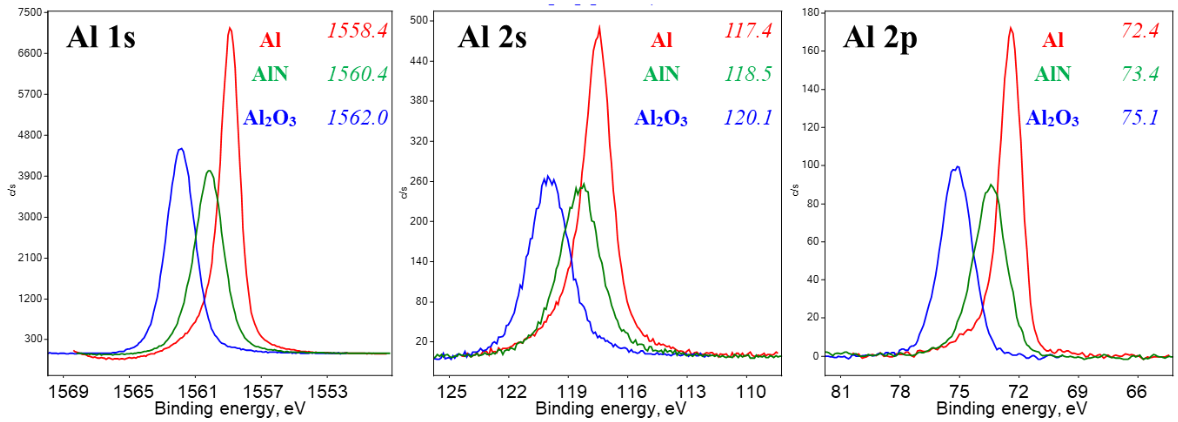

Figure 1. High-resolution HAXPES Al 1s, Al 2s and Al 2p spectra for pure Al metal, Al nitride, and Al oxide.

Moreover, accessible transitions cover a large range of kinetic energy and, hence, sampling depth. For example, the Ti 1s photoelectron has a kinetic energy of ~*444* eV originating from a sampling depth of ~ 3-4 nm, while the Ti 2p photoelectron has a much higher kinetic energy of ~*4950* eV originating from as deep as 22-24 nm. Variable depth analysis can be easily performed for studying gradients, segregation, and oxidation phenomena.

Many of the Auger transitions contribute to the binding energy range of soft Al X-ray source – *0-1400* eV. When the Cr X-ray source is used, Auger transitions are shifted to a higher binding energy range clearing up the spectral range where most databases have data on chemical shifts.

CHALLENGES IN QUANTIFICATION OF HAXPES DATA

The full benefits of the lab-based HAXPES technique are dependent on the development of parameters for accurate quantification. We at Physical Electronics have started developing experimental pure elemental relative sensitivity factors (PERSFs) for our Cr X-ray source using data obtained from ionic liquids and pure bulk elements. PERSFs were obtained by measuring the peak intensity of the selected element normalized by the peak intensity of key reference material (sputter cleaned Ag foil in our case).[5] Table 1 shows the results of the quantification of aluminum[2-4] and silicon-based compounds[6-8] using PERSFs. One can see that quantification is very accurate for some compounds using some transitions, while off by 5-7 % for others.

TABLE 1. Quantification (percent atomic) of Al- and Si-based compounds using PERSFs. Averages of 2-3 datasets per compound are shown.

Compound	Al 1s	Al 2s	Al 2p
Al_2O_3 (40% nominal Al)	38.5	36.2	37.1
AlN (50% nominal Al)	51.4	50.0	51.2

Compound	Si 1s	Si 2s	Si 2p
SiO_2 (33.3% nominal Si)	33.1	31.8	32.9
SiC (50 % nominal Si)	49.4	47.9	50.9
Si_3N_4 (42.8% nominal Si)	42.8	47.9	50.9

The uncertainties of quantification that have been discussed in the literature for conventional Al and Mg X-ray source data[9] are even more significant for HAXPES data. These include the uncertainty of background subtraction, XPS peak satellite structure handling, and the accuracy of derived RSFs. Due to the much larger range of kinetic energy of photoelectrons in HAXPES data, the scattering and matrix effects on quantification may also be more significant.

APPLICATIONS OF HAXPES

We will discuss new applications of laboratory HAXPES for the analysis of materials and interfaces used in device technology. HAXPES is of particular interest for optimizing GaN high electron mobility transistors (HEMTs) for the electronic power market because the layer thickness of the gate oxide necessarily increases well beyond the sub-5 nm values encountered in logic transistors. HAXPES is a promising technique to investigate an Al_2O_3/GaN interface with a thick gate oxide without the need for extensive sputtering. Another benefit of HAXPES for GaN-based structures is the elimination of overlap between the N1s core level and the Ga LMM Auger lines which occurs using a standard Al Kα source. Recently developed software, *StrataPHI,* for thin-film structure determination from a single take-off angle HAXPES data creates an opportunity for high-throughput metrological applications for multi-layered semiconductor devices.

Operando HAXPES is a relatively new field in which a prototypical device is analyzed while an external stimulus is applied during the experiment. We will report on operando HAXPES measurements with Cr Kα excitation on a prototypical memory device (100×100 µm active area) fabricated from a Sr-doped lanthanum manganite oxide as active material showing reversible resistance changes upon biasing, also known as resistive switching (RS). To precisely understand the device's operating modes, HAXPES spectra obtained under sample bias were studied.

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KEYWORDS

Characterization, XPS, HAXPES, operando, HEMT, thin-film structures

Characterization of Electronic Materials Using the PHI *VersaProbe* 4 Multi-Technique XPS Scanning Microprobe

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INTRODUCTION

Developments of advanced electronic materials, such as batteries, solar cells, and flexible display panels require detailed knowledge of the electronic band structure in order to achieve the desired performance. Properties of interest include electron affinity, work function, ionization energy, and bandgap. Traditionally, measuring these properties required the use of multiple instruments, making it difficult to analyze the sample in the exact same location under the same conditions. Moreover, numerous transfers between different instruments increase the likelihood of sample contamination.

The PHI *VersaProbe* multi-technique instrument has options allowing measurement of these important properties using a single analytical chamber. Low energy inverse photoemission spectroscopy (LEIPS) coupled with ultraviolet photoelectron spectroscopy (UPS) can be used to fully characterize a material's band structure. Figure 1 shows a schematic of a band structure analysis, showing the contribution of UPS and LEIPS to the measurement. The valence and conduction bands can be characterized using UPS and LEIPS, respectively. UPS can measure the work function and ionization energy, while LEIPS is used to measure the electron affinity of a particular material. LEIPS is a lower energy variant of inverse photoemission spectroscopy (IPES). The lower energy of the incident electron beam makes it less damaging to more sensitive organic electronic materials, which are a growing avenue of materials research. The electron affinities of several OLED materials, such as TCTA, CBP, and Ir(ppy)3 have been measured with LEIPS.[1]

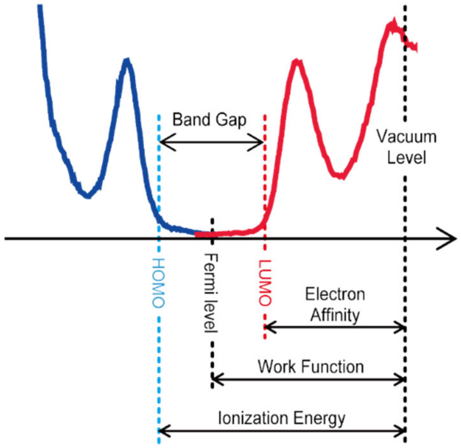

FIGURE 1. A schematic of the electronic properties that can be measured using UPS (blue) and LEIPS (red).

This talk will overview LEIPS and UPS and how they are used together to characterize band structure. In addition, some examples of current applications of the techniques on electronic materials will be discussed.

UPS, LEIPS AND XPS USING A SINGLE ANALYTICAL CHAMBER

In a PHI *VersaProbe*, LEIPS, UPS and X-ray photoelectron spectroscopy (XPS) are all available on a single instrument. The same point can be analyzed with all three techniques without removing the sample from the instrument. The UV source operation is completely integrated into the software allowing for remote operation of the source, and can be queued along with XPS measurements. The UV beam size is 1.5 mm in diameter and can be equipped with an optional UV filter, to reduce the photon flux for samples that are UV sensitive. LEIPS differs from IPES in that the energy of the incident electrons is much lower. While IPES typically uses 10 eV electrons, LEIPS electron energy is < 5 eV. LEIPS was first demonstrated by Yoshida et al.[2] Electrons are generated at fixed energy using a BaO source, while the sample stage is biased to achieve net incident energy of < 5 eV. As the electrons fill unoccupied conduction band states, photons are emitted and detected using a fixed wavelength detector. Electron affinities up to 5.79 eV can be measured using user-selectable bandpass filters. A C_{60} film exposed to a standard IPES source shows evidence for electron beam damage after 10 minutes of exposure, while the same material shows no change after 120 minutes using LEIPS.

APPLICATIONS OF UPS AND LEIPS

Along with a general overview of UPS and LEIPS, a few current applications of the techniques will be presented. A combination UPS and XPS depth profile on a multilayer film stack shows a change in the ionization potential of the material as each layer is exposed upon sputtering. By combining a UPS and XPS depth profile, the electronic structure information (from UPS) and the chemical state information (from XPS) can be obtained from a single sputter crater.

Solid-state batteries are viewed as the next generation of batteries due to their improved thermal stability and safety over lithium-ion batteries. However, wide range commercial use is limited by several challenges. One such challenge is the internal resistance generated between the electrolyte and electrode interface, which limits the charge-discharge cycling performance. A combination of TOF-SIMS, XPS, UPS and LEIPS were used to characterize this interface between the cathode-electrolyte of a LiPON/$LiCoO_2$ solid-state battery.[3]

Recent work at Universiti Malaysia Sabah[4] illustrated the effect of graphene oxide on the electronic properties and performance of Engelhard Titanosilicate-10 (ETS-10). ETS-10 is typically not used in photocatalytic applications due to its relatively high (~4.0 eV) optical bandgap. UPS and LEIPS measurements show that when graphene oxide is incorporated into ETS-10, the optical band gap is considerably lower. This study also represents the first example of using UPS and LEIPS on a semiconductor photocatalytic powder.

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KEYWORDS

UPS, LEIPS, IPES, XPS, Solid-state battery

Robust, Quantitative IR-AFM For Use In An In-FAB Multimodal Metrology Scheme

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INTRODUCTION

For continued increases in performance and efficiency, device structures are getting more complex not only geometrically, but also in material composition. In fact, tuning material properties to achieve desired characteristics is increasingly important for next generation devices. Naturally, the importance of the quality of production of these carefully designed structures is increasing correspondingly. It is unsurprising therefore that there is an increasing focus on assessing material composition and purity for metrology purposes. Optical methods seem well posed to assess chemical or elemental composition, and a number of techniques are being developed based on spectroscopy (IR, UV or Raman), or X-Ray fluorescence [1]. While these optical methods allow to investigate large area's at high throughputs, they necessarily obtain information at a resolution of micrometers due to spotsizes used. This means these methods average always over many structures and that they need models to interpret measurement data. Ensemble averaging is known to hide important individual deviations from the average [2]. Modelling the increasing complexity of the structures to the increasingly tight specifications demanded by future processes means these models will contain many parameters and are going to be hard to fit correctly. These considerations lead to a call for multi-modal metrology where different modalities are combined in one analysis to make use of the strong points of each modality. Here is an opportunity for unconventional metrology techniques to fill in gaps in what conventional metrology techniques can provide and thus to enhance the added value of the complete metrology suite. One such unconventional metrology technique could be Scanning Probe Microscopy (SPM). It is especially complementary to optical techniques: it provides high resolution, non-destructive measurements of individual device structures with potentially a large range of material properties – we will focus on chemical identification using tip-enhanced IR spectroscopy in this contribution. On the other hand, it is a very slow technique. Even the fastest systems (NFI) have only a fraction of the throughput of optical methods. This complementarity makes it a natural selection for multimodal metrology in combination with optical techniques. However, there are additional caveats with SPM based techniques: they rely on inherently variable --- because man-made --- objects (the tips) which are sensing through highly non-linear interactions the complex device structures. These two aspects make it difficult to interpret quantitatively signal levels, or even to guarantee a certain sensitivity. In its typical lab-environment application this is not a problem, and people know routinely to extract useful information at the limits of theoretically attainable sensitivity, although sometimes operating a SPM is considered more a handicraft than a science. However, for automated application as an inline metrology tool, it is paramount that sensitivity and quantitative interpretation are guaranteed and understood. Here we report on our steps towards this goal.

ROBUST, QUANTITATIVE IR-AFM

As mentioned in the introduction, we focus on a particular use of SPM, namely IR-AFM, in the particular implementation by vendor Molecular Vista called Photo-induced Force Microscopy (PiFM)[3]. In this implementation, (mid-)IR light is focussed on a metal coated AFM tip. The tip effectively acts as an antenna causing a strong field enhancement (of ~30x in the absence of a sample) in a volume around the tip of which the lengthscale is governed by the tip radius, typically 10 nm. This electromagnetic field may either induce dipoles in sample and tip, causing a repulsive force between them, or may induce heating and thermal expansion of the sample (and tip), causing a change in height. The AFM cantilever is then used to sense the force or height in a measurement scheme involving frequency mixing. For this, topography is measured by amplitude modulation of the second eigenmode of the cantilever, while the IR light is pulsed at a frequency corresponding to the difference between second and first eigenmodes. The non-linear tip-sample interaction acts as frequency mixer causing a response also at the difference frequency, which is the first eigenmode. Typically, the second mode amplitude during scanning is around 1 nm, while the first eigenmode response is much smaller.

In order to understand systematically and quantitatively the contrast and image formation in IR-AFM and their dependence on measurement settings and sample properties, we performed both extensive experiments and simulations. The simulations encompass Finite Element Modelling (FEM) of the Electro-Magnetic (EM) field around the tip and sample, FEM of the time-dependent thermal expansion of the sample and a numerical solver for Ordinary Differential Equations to describe the cantilever motion in experimental conditions. We varied sample and measurement parameters systematically in the simulations, and compared them to experiments to verify we captured the behaviour and to guide our understanding of this system.

Finite Element Modelling of Tip-Sample Interaction in IR-AFM

The FEM of the electromagnetic field revealed that in absence of a sample, the field is enhanced by about 30x times compared to the incident field strength due to the antenna effect of the tip (our simulation includes about 5 micrometer of tip height). With the tip in close proximity to the sample, this effect is even stronger. This is because, when the tip is closer than its radius, multiple scattering can occur between tip and sample. From the distribution of the EM field, we can directly calculate the induced force between tip and sample, see fig 1 (middle) for the dependence of this force on tip-sample distance. From the EM field distribution we can also calculate the power deposited in the sample. Scaling this power with a time dependent strength of the applied pulse allows us to calculate the time dependent thermal expansion of the sample as well. Here we see that, due to the tiny heated volume, the heat dissipates on a quicker timescale than the laser pulse, such that the thermal expansion follows the shape of the laser pulse, see fig. 1 (right). It is also clear from the simulations that thermal expansion of the tip is a significant contribution to the total signal (around 50% in the cases we simulated). For the cases we looked at (organics, oxides, nitrides), thermal expansion is the dominant contrast mechanism, although for metals or 2D materials, the photo-induced force looks to be the dominant contrast mechanism. From simulations involving differen layer thicknesses it is also clear that an important consideration with thermal expansion is the thermal conductivity of the sample. This means that, especially for very thin top layers, buried layers may influence the signal level. It also means that topography may influence the signal level – in small, freestanding structures, heat can only be conducted downward, not sideways. This all points to the importance of taking into account the actual device structure to understand signal levels.

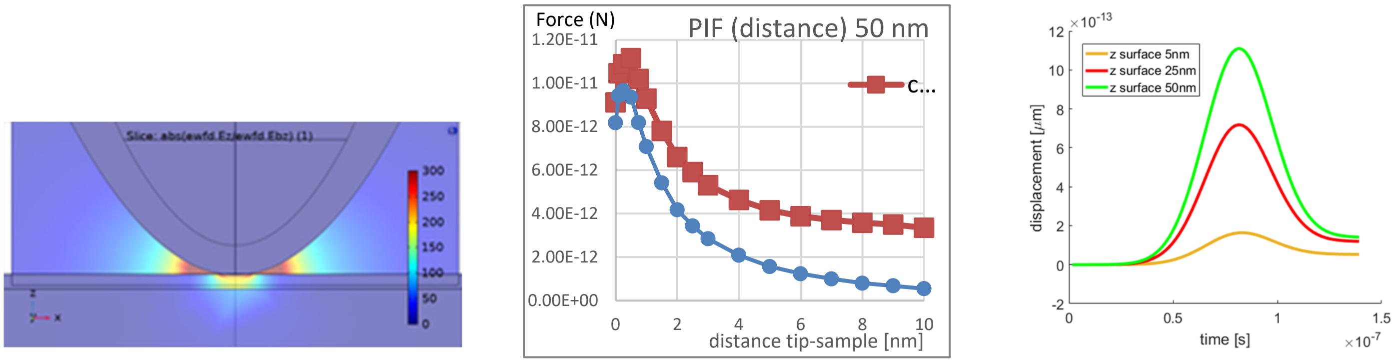
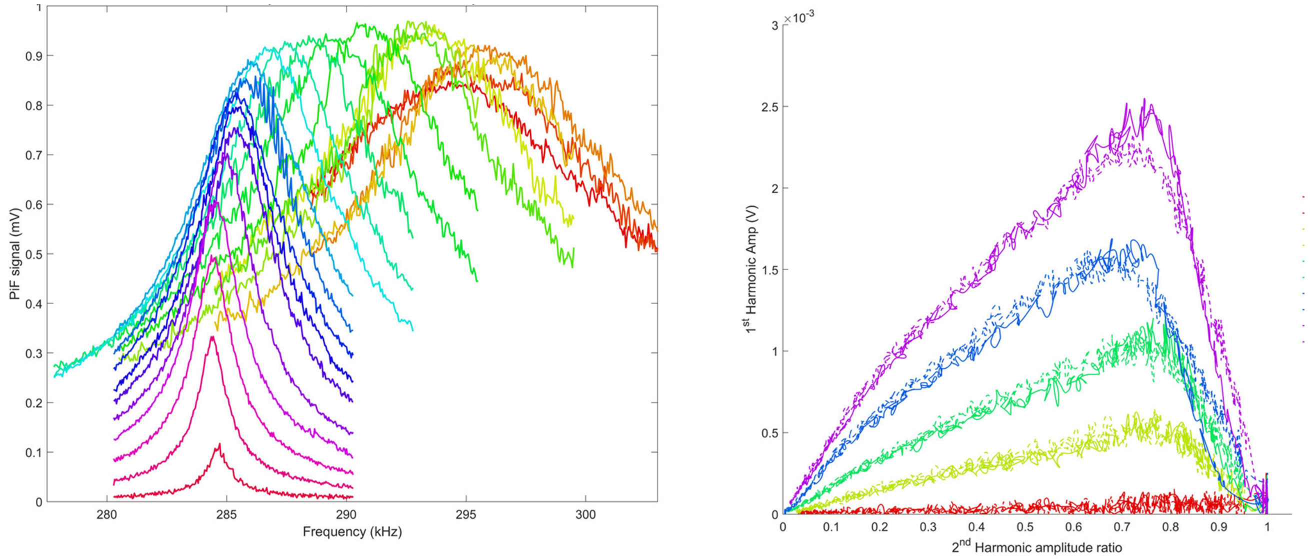


FIGURE 1. (Left) Result of FEM of electeromagnetic field strength. This is a zoom in on the tip-sample contact showing clearly the strongly enhanced field between tip and sample. (Middle) Opically induced Force as function of tip sample distance calculated from the EM field distributions for a 50nm thick layer of SiO_2. (Right) Result of FEM of the time-dependent thermal expansion of the sample for three different thiciknesses of SiO_2 on top of a Si substrate.

Experimental Investigation of Measurement Parameters in IR-AFM

From the non-linear interactions and complicated measurement scheme, it is clear that it is of paramount importance to understand the cantilever dynamics and how these are influenced by measurement parameters to result in signal levels. We started with a systematic experimental investigation to understand the influence of key measurement parameters (Fig 2 top panels) and to build up a protocol to perform robust measurements (fig 2 bottom panel). Note that the linear increase of signal level with layer thickness agrees well with the FEM results for thermal expansion of this same model system (fig. 1 (right)).



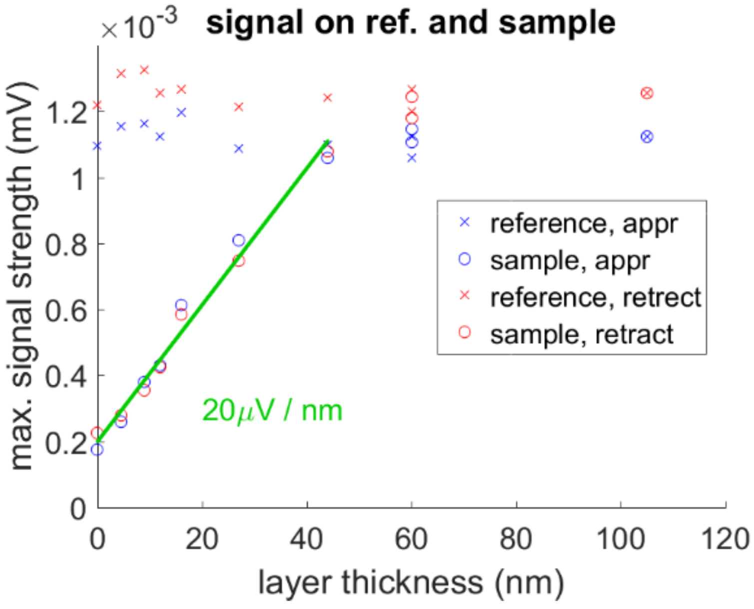


FIGURE 2. (Top left) Experimental signal level at different imaging setpoints (50% [orange] to 95% [red]) as function of frequency. The x axis denotes demodulation frequency, excitation is at f2 (~1.6 MHz) minus the indicated frequency (Top right) Signal level at fixed excitation frequency as function of amplitude ratio for different laser powers (0% [red] to 20% [purple]). (Bottom left) Signal level as function of layer thickness measured using a protocol to account for variability from experimental parameters such as depicted in top left. Each dot is a new sample, with renewed optimization of measurement settings. The crosses are measurements on the reference (thickest) sample conducted after each individual measurement on a thinner sample.

Then we continued to build a model of the cantilever dynamics to capture its complicated behaviour. We iterated between simulations and experiments to make sure we used relevant modelling parameters and captured relevant cantilever dynamics. We implemented the interaction as a standard lennard jones potential between (gold) tip and SiO_2 surface. The thermal expansion was modelled as a time-dependent decrease of tip-sample distance. Photo-induced force was not yet included in the results shown here. Perhaps unsurprisingly, the non-linear interaction and the frequency mixing scheme mean there is very rich behaviour of cantilever dynamics which is captured only in small part by regular lock-in based SPM techniques. These dynamics were indeed also found when checking the experiments. An example of the correspondance between simulations and experiments is given in fig. 3. This allows us to link the outcome of the FEM simulations to signal levels in the AFM taking into account measurement parameters.

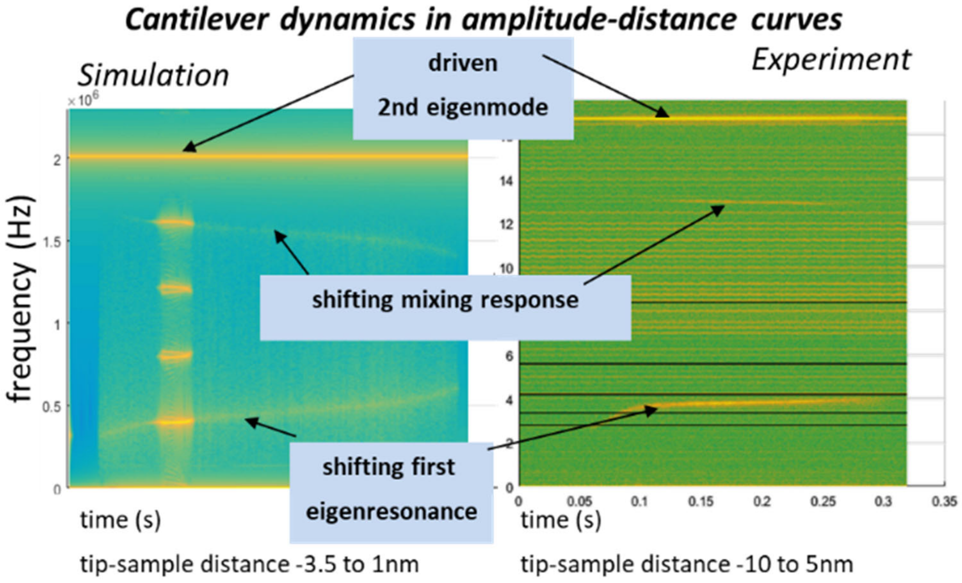


FIGURE 3. (Left) simulation and (right) experiment showing cantilever dynamics during an amplitude-distance approach cycle. Horizontal axis: time (and tip-sample distance); vertical axis: frequency. Colour scale: amplitude of motion. Each vertical slice represents a spectrum at that time or tip-sample distance. A number of correspondances between experiment and simulation have been highlighted.

All together, we progress towards a quantitative understanding of IR-AFM, allowing interpretation of signal levels independent of experimental parameters and in terms of the actual sample structure. This paves the way to integrate this technique in a robust, reliable and automated way into multimodal measurement schemes for use in a FAB.

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KEYWORDS

SPM, IR-AFM, robust, multimodal, automated

Mueller-matrix scattered-field microscopy for the measurement of finite deep sub-wavelength nanostructures

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INTRODUCTION

Optical scatterometry is currently the workhorse tool for measuring the critical dimension (CD) in current semiconductor manufacturing [1], where the measurements are made on special target gratings etched in scribe lines between chips. The grating target typically consists of repetitive dense structures. However, when the grating target only contains few repetitive structures, or in the extreme case, the grating target becomes an isolated structure, conventional optical scatterometry will be infeasible anymore.

In this work, we propose a new approach called Mueller-matrix scattered-field microscopy (MSM), which is capable of quantitatively determine the geometrical parameters of finite deep sub-wavelength nanostructures. The experimental setup of MSM employs a high numerical-aperture (NA) objective lens to collect a broad range of spatial frequencies of the scattered field in terms of Mueller-matrix images. A rigorous forward scattering model is established for MSM to reconstruct nanostructures, which takes account of the vectorial nature of the scattered field when passing through the imaging system and the effect of defocus in the measurement process. The experimental results performed on a series of isolated Si lines demonstrate that the proposed MSM can resolve a feature size of $\lambda/16$ (λ is the wavelength) with a sub-7 nm accuracy. It is also expected that this work paves the way for a powerful and efficient characterization tool for future mass IC manufacturing.

EXPERIMENTAL SETUP

Figure 1 presents the schematic of MSM, which consists of an illuminating light path indicated by the red arrow and an imaging light path indicated by the blue arrow, respectively. For the illuminating light path, a laser driven broadband light source is used and the light emitted by it is collimated by the lens L_1. The light is filter into a monochromatic light with the wavelength of 633 nm by the bandpass filter and is reflected by a rotatable mirror. Then the light passes through the polarization state generator (PSG) consisting of a polarizer and a phase retarder. Next, after passing through a non-polarizing beam splitter BS and lens L_2, the light is focused on the back focal plane (BPF) of the objective lens (OB, Zeiss Epiplan-Apochromat 50× with NA of 0.95). After passing through the OB, a parallel light illuminates the sample with uniform intensity over the spot. Moreover, we can rotate the mirror to change the position of the focal point on BPF, then the incident angle of illuminating light is also changed. As for the imaging light path, the scattered light from the sample is collected by OB and passes successively through lens L_2 and BS. Then the scattered light passes through the polarization state analyzer (PSA) consisting of an analyzer and another phase retarder. The OB, L_2, L_3, and L_4 form two 4-f imaging systems, and finally the sample is imaged onto the camera. Note that, the phase retarders in PSG and PSA are both kept rotating during the measurement to generate different combinations of polarization states [2]. As a result, all 16 images of the Mueller-matrix of the sample can be acquired in a single measurement. For details about calibration of MSM, please refer to [3].

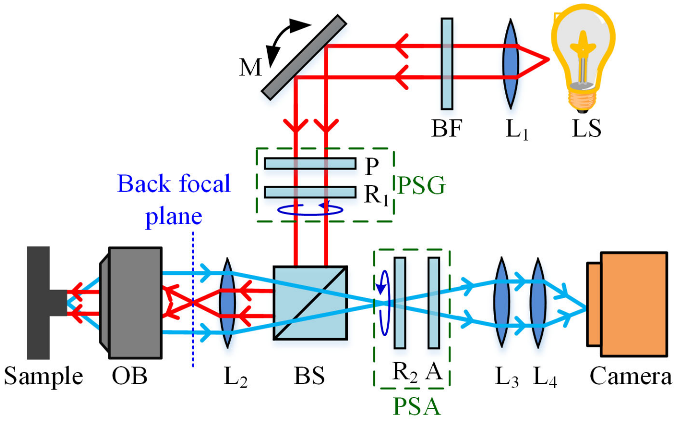

FIGURE 1. The schematic of the developed Mueller-matrix scattered-field microscope. LS: light source; BF: bandpass filter; M: mirror; P: polarizer; R_1, R_2: phase retarder; BS: beam splitter; OB: objective lens; A: analyzer; L_1~L_4: lenses.

MEASUREMENT RESULTS

To demonstrate the capability of MSM for measuring finite deep subwavelength nanostructures, a series of isolated Si lines on a Si substrate with different dimensions has been prepared by e-beam lithography followed by dry etching. As schematically shown in Figure 2(a), we design six lines named L1 ~ L6 with a nominal width increases from 20 nm to 120 nm in a 20 nm interval and a nominal height of 50 nm. Figure 2(b) and Figure 2(c) show the scanning-electron microscopy (SEM) micrograph of one of the fabricated isolated line samples. Note that the above isolated Si lines represent an extreme case of the finite deep subwavelength nanostructures. It can be expected that the proposed approach is also applicable to other finite subwavelength features.

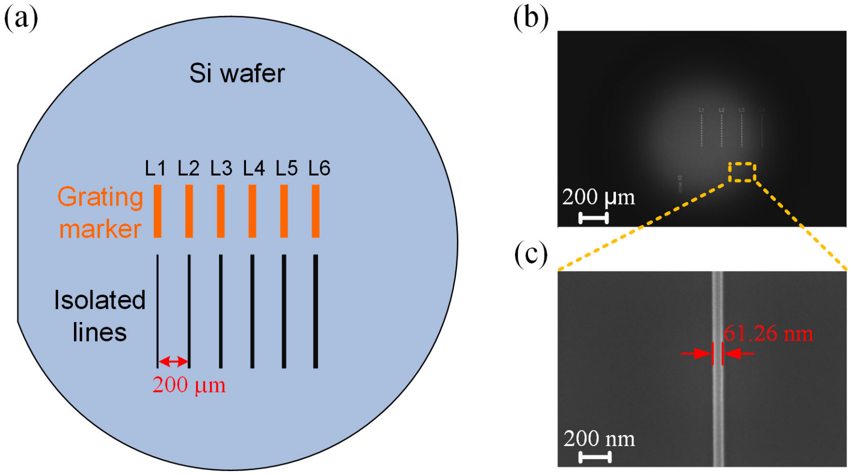

FIGURE 2. (a) The layout of the isolated Si lines on the Si wafer; (b) The SEM micrograph of the investigated isolated Si lines; (c) The SEM micrograph of the line with a nominal width of 60 nm.

Then, we established a forward model for MSM and used it to fit the measured Mueller-matrix image to measure the width of the isolated Si lines [4]. After solving the inverse fitting, the final fitting Mueller-matrix (i.e. the best-fit calculated Mueller-matrix to the measurement) of the isolated Si line with a nominal width of 100 nm at the normal incidence is shown in Figure 3. Great agreement can be observed in Figure 3, especially in m_{34} and m_{43}. As a result, the width measured by MSM is 106.90 ± 10.25 nm (with a 95% confidence interval). For comparison, the measured results by SEM is 100.90 ± 2.70 nm (with a 95% confidence interval). The relative error of MSM is 5.94% with respect to SEM. Table 1 presents the comparison of measured results from MSM and SEM for different isolated lines. As can be observed from Table 1, compared with SEM measurements, the absolute error MSM is less than about 7 nm for the linewidths of 40 ~ 120 nm. And the coefficient of determination R^2 between the MSM- and SEM-measured results is 0.976 for the linewidths of 40 ~ 120 nm, which reveals a great correlation.

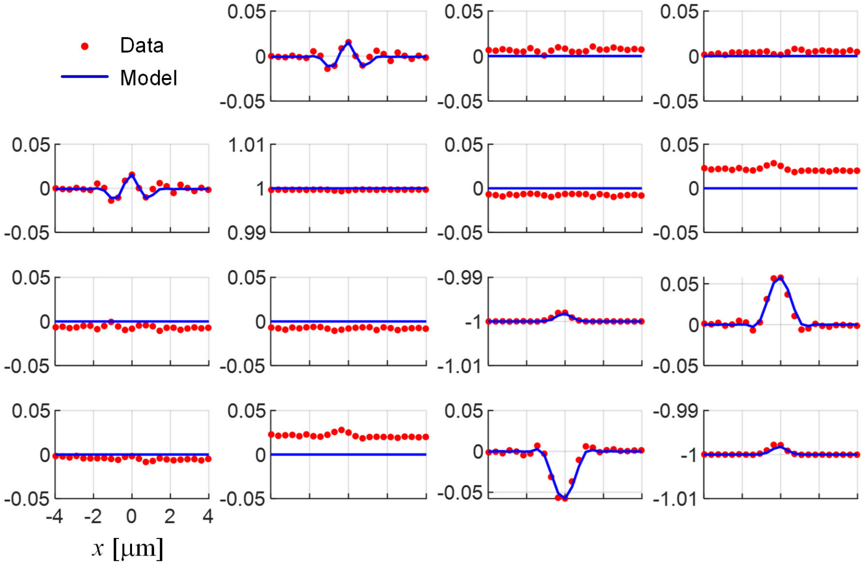

FIGURE 3. The best-fit calculated and measured Mueller matrices of the isolated Si line with a nominal width of 100 nm at the normal incidence. The SEM- and MSM-measured widths are 100.90 ± 2.70 nm and 106.90 ± 10.25 nm, respectively. The relative error is 5.94%.

TABLE 1. Comparison of the measured width of isolated Si lines from MSM and SEM measurements. The uncertainties appended to MSM- and SEM-measured values all have a 95% confidence level.

SEM [nm]	120.70± 2.36	100.90± 2.70	79.28± 2.90	61.26± 2.56	41.44± 1.76	19.82± 1.78
MSM [nm]	113.61± 14.38	106.90± 10.25	86.12± 4.29	67.38± 2.66	47.38± 2.77	12.47± 3.90
Relative Error	5.87%	5.94%	8.63%	9.98%	14.34%	37.06%

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KEYWORDS

Optical scatterometry; Mueller matrix image; nanostructure metrology; inverse scattering.

A See-Through Metrology Toolbox For Fast Gate-All-Around Device Characterization

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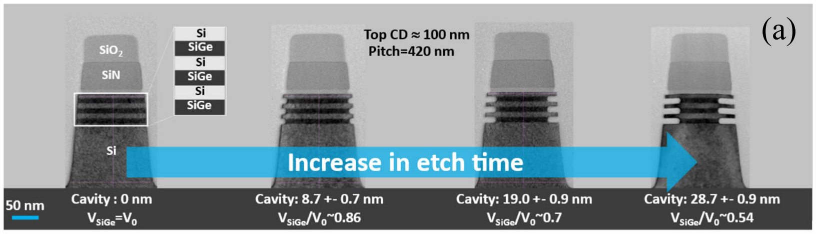
INTRODUCTION

The fine-tuning and control of processing during the fabrication of three-dimensional gate-all-around (GAA) devices require fast and precise metrology of buried features. This is particularly true after the selective lateral etching of the sacrificial SiGe during the inner spacer and release modules of the nanosheet (NS) and forksheet (FS) process flows [1,2]. A geometrical parameter with a strong impact on the final device performance is e.g. the cavity depth, which defines the inner spacer dimension in the final GAA device [2]. Unfortunately, these measurements must take place after cavity etch, i.e. when the device geometry is complex and the information is buried deep within the structure. Standard inspection, e.g. with scanning electron microscopy (SEM), is therefore of little use such that slow and destructive cross-sectional electron microscopy is the only existing option for such measurements.

We propose a see-through metrology toolbox focusing on top-down measurements of the dimensions of buried cavities in devices comprising SiGe/Si or poly-Si/SiO_2 superlattices. We demonstrate the complementary strengths of three types of high-throughput techniques, i.e optical critical dimension (OCD) scatterometry [3], high-voltage SEM [4] and top-down spectroscopic (TDS) techniques [5].

RESULTS AND DISCUSSION

This paper is based on measurements of the three devices shown in the transmission electron microscopy (TEM) images of Fig 1. The nanosheet devices (Fig. 1(a)) show a variation in the average SiGe cavity depth between 0 and 28.7 nm. The cavities in these devices are buried under a thick SiO_2 and SiN hard mask (HM). The forksheet devices (Fig. 1(b)) have a varying average SiGe cavity depth ranging from 0 nm to full release. Finally, the 3D memory devices (Fig. 1(c)) are composed of a poly-Si/SiO_2 superlattice with a varying depth of the poly-Si cavities. These wider devices have deep poly-Si cavities, ranging from 88 to 121 nm.



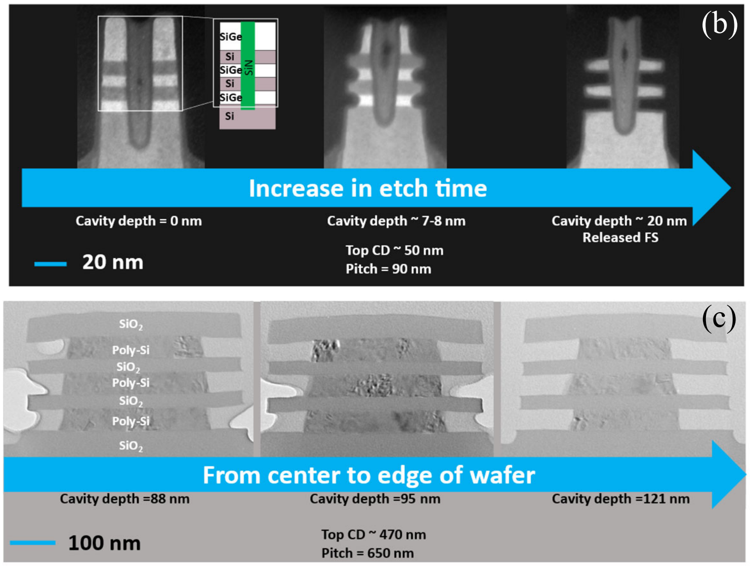


FIGURE 1. (a) Nanosheets with different average SiGe cavity depths ranging from 0 and 28.7 nm. The top CD~100 nm and the SiGe/Si superlattice is buried under a ~100-nm thick SiO_2/SiN hard mask (b) Forksheets with different average SiGe cavity depths ranging from 0 nm to forksheet release. (c) 3D memories with average poly-Si cavity depths ranging from 88 to 121 nm.

Optical Critical Dimension (OCD) Scatterometry

OCD is the technique of our toolbox allowing measurements on large periodic arrays of devices and offering high sensitivity not only to cavity depth but also to the rest of the device geometry [3].

Fig. 2 illustrates the powerful capabilities of the NOVA Stand-Alone (SA) OCD tool for measuring buried information on nanosheet devices. Not only the cavity depth but also the other critical geometrical parameters, i.e. top CD, line height and sidewall angle, are measured with a high sensitivity. This allows the reconstruction of the full device geometries, as shown in Fig. 2(b). Furthermore, these fast non-contact measurements lead to full wafer maps, as exemplified in Fig. 2(c).

OCD was also tested on forksheets and 3D memories with equally good results (not shown in this abstract).

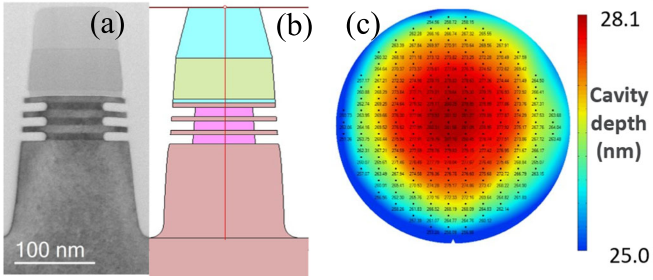


FIGURE 2. Comparison of (a) the TEM and (b) the reconstructed OCD profiles of a nanosheet sample with nominal cavity depth of 30 nm. (c) Within-wafer variations in cavity depth as measured with NOVA SA OCD.

High-Voltage Scanning Electron Microscopy (HV-SEM)

HV-SEM is the technique of our toolbox for measuring the cavity depth in single devices [4] offering not only cavity imaging potential on wide devices with a good (~nm) lateral resolution but also access to critical information such as cavity roughness.

The unique see-through capabilities of the HV-SEM PROVision tool of Applied Materials are demonstrated in Fig. 3 on devices with relaxed dimensions such as our 3D memories. As indicated in Figs. 3(a) and (b), the grey areas observed at the line edges are the buried poly-Si cavities, i.e. the part of the top SiO_2 without any underlying poly-Si. This figure also demonstrates that the PROVision tool gives access to the roughness of these deep cavities. In the shown example, the cavity is imaged deeper, in agreement with the TEM of Fig. 1, but also rougher at the edge of the wafer than at its center. Furthermore, all the acquired information is extracted fast (~10-20 min/wafer) such that wafer maps can be generated to understand the uniformity of the process [Fig. 3(c)], enabling fast DOE's and massive data nondestructive process splits, necessary to ramp up such complicated processes in fast time to markets.

HV-SEM was also tested on nanosheets and forksheets with similar results (not shown in this abstract).

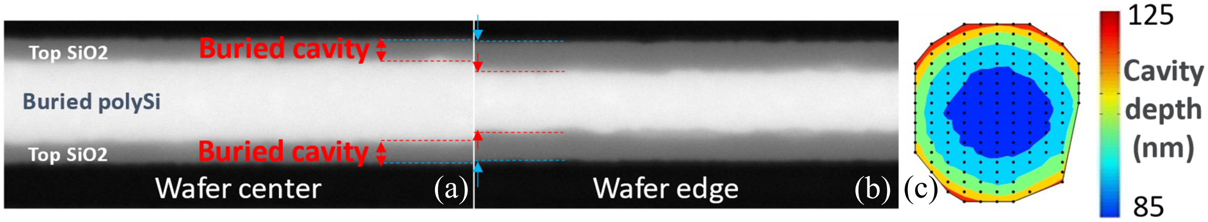


FIGURE 3. Comparison of the HV-SEM micrographs acquired with PROVision at the wafer center (a) and edge (b) of the 3D memory. Top CD, depth and roughness of the poly-Si cavities are imaged simultaneously (c) Within-wafer variations in cavity depth as measured with PROVision.

Top-Down Spectroscopic (TDS) Techniques

TDS techniques are the third type of techniques in our toolbox [5]. The critical value added by these techniques is that the measured intensities give information about the remaining volume of sacrificial material and offer thus easy interpretation. TDS measurements of cavity depth are demonstrated in Fig 4 on respectively nanosheet and forksheet samples. As observed, independently from the TDS technique, the measured signals are simply an image of the volume of remaining SiGe. The latter signals therefore drop as the cavity depth increases.

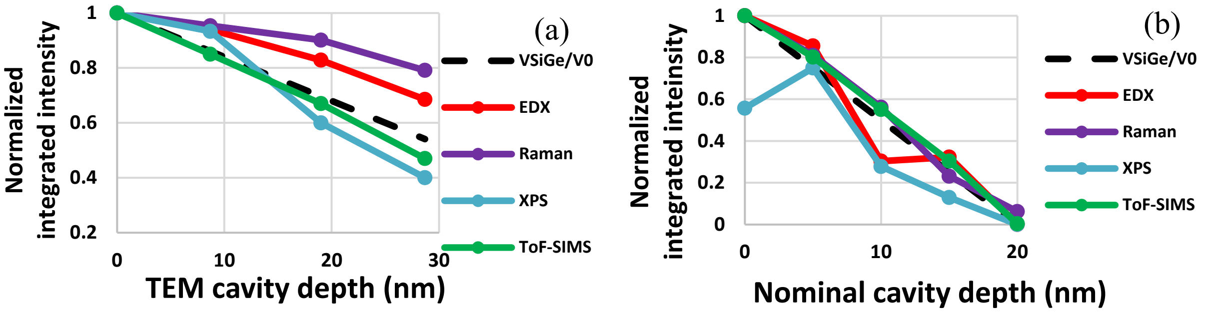


FIGURE 4. TDS measurement of cavity depth on the (a) nanosheet and (b) forksheet samples. The integrated (Si)Ge peak drops linearly as the cavity gets deeper, whether using energy-dispersive X-ray spectroscopy (EDX), Raman spectroscopy, X-ray photoelectron spectroscopy (XPS) and Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS).

CONCLUSIONS

This paper demonstrates the value of our toolbox for fast wafer-scale measurement of buried and hidden information in GAA devices. First, OCD is the technique recommended for measuring not only cavity depth but also the rest of the device geometry on large targets. Second, HV-SEM allows cavity measurements or even imaging in single devices. Finally, TDS techniques measure volume changes of the sacrificial material. The combination of such techniques allows a local, accurate as well as statistically relevant characterization of the GAA processing.

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KEYWORDS

Gate all around, nanosheet, forksheet, cavity etch, inner spacer, lateral recess, inline metrology

In-line Multi-scale Thickness And Roughness Characterization For FD-SOI HVM

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INTRODUCTION

The importance of thickness and roughness control to limit the threshold voltage variability in CMOS electronics based on Fully Depleted Silicon-on-Insulator (FD-SOI) technology has been widely discussed. The spatial frequency range to be considered goes from full 300 mm wafers to transistor scale (10 nm).

The most commonly used metrologies are Spectroscopic Ellipsometry (SE) for low spatial frequencies, Scanning White Light Interferometry (SWLI) and Atomic Force Microscopy (AFM) for medium and high spatial frequency range. Multiple in-line options are available for the SE, on the contrary SWLI and AFM are often low throughput and off-line tools. This paper describes how Differential Reflectance Microscopy (DRM) was implemented and correlated to laser light scattering and AFM to provide an in-line and high throughput characterization of a wide spatial frequency range, compatible with high volume manufacturing.

INFLUENCE OF TOP SILICON LAYER UNIFORMITY ON DEVICES VARIABILITY

With scaling down device dimensions the variability of the electric characteristics becomes a major challenge. FD-SOI technology allows better performances and excellent variability immunity due to utilization of undoped channel. The specific variability factors for this technology have been analyzed in details [1]. The channel silicon thickness (T_{Si}) is a major variability factor: device V_T correlates to T_{Si} variation, with an empirical relation estimated to be dV_T/dT_{Si}=39mV/nm for 28nm grid transistors [1].

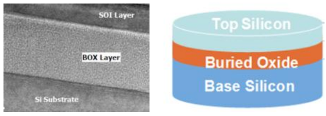

FIGURE 1. FD-SOI material schematics, showing Top Silicon (TOP) and Buried Oxide (BOX)

IN-LINE THICKNESS AND ROUGHNESS CHARACTERIZATION

For an effective FD-SOI process monitoring, multiple spatial frequencies need to be characterized, as described in [3] and [5]. The table below summarizes the spatial frequencies and associated metrologies, detailed hereafter:

TABLE 1.

Frequency band [μm^{-1}]	Spatial band [μm]	Variability impact	Metrology
1-100	0.01-1	Device to device	AFM
0.1-1	1-10	Device to device	AFM
$1*10^{-3}$-0.1	10-1000	Device to device	DRM
$1*10^{-3}$-$1*10^{-4}$	$1*10^{3}$-$1*10^{4}$	Within die	DRM/haze correlation
$1*10^{-4}$-$1*10^{-5}$	$1*10^{4}$-$1*10^{5}$	Die to die	Ellipsometer

In-Line Differential Reflectance Microscopy Implementation

Novel DRM technology was implemented as in-line characterization of the local thickness for top silicon (TOP) and buried oxide (BOX) layers in FD-SOI line. As detailed in [4], DRM is based on the dependence of the optical reflectivity of a layer on its thickness. For a two-layer stack, the appropriate wavelengths were selected to separate the contributions of the TOP and the BOX layers. Thus Bright Field images collected with a microscope objective correspond to thickness maps of TOP and BOX layers. Exact T_{Si} and T_{SiO2} maps are calculated from these images using second order polynomial model. The intensity to thickness calibration was performed on several SOI wafers using SE measurements as a reference (FIG.2).

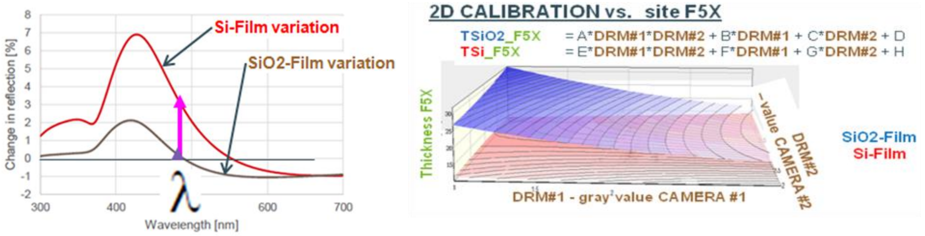

FIGURE 2. Reflectivity variation for Si and SiO_2 versus wavelength and DRM calibration with SE data

The DRM covers a spatial frequency interval ranging from the image size (266 µm to 12 mm depending on the objective magnification) down to its resolution (1 µm at highest magnification available). Single images can be stitched to cover the full wafer surface. The system has been optimized to deliver a fast throughput (tens of wafers per hour) and thanks to the data acquisition and treatment protocol, the DRM in-line capability is now close to SE.

Laser Light Scattering Local Variation As Local Thickness Standard Deviation Proxy

DRM provides full wafer thickness maps for both TOP and BOX layers. However in a HVM line this is an additional metrology step. In order to gain in efficiency, DRM data were correlated with defect inspection tool parameters to get both defects and thickness information on a single measurement. Unpatterned FD-SOI wafers are inspected using a laser light defect inspection system (Surfscan SP5 from KLA). Laser light scattered by the defects and the surface is collected over a selectable portion of the solid angle. The scattering from the surface is commonly named as “haze”. As the incident laser power isn’t absorbed into the TOP layer completely, the reflectivity and the scattering (the haze) are a function of local thickness variations of our dual-layer system [2] and [6].

FDSOI typical TOP thickness is 12 nm: the penetration depth of SP5 laser into silicon (defined as depth for 1/e intensity drop) is 4.8 nm, meaning that > 5% of the incident radiation is conserved for 12 nm depth.

Thus considering the haze standard deviation on an appropriate area, haze metrics correlate to thickness metrics.

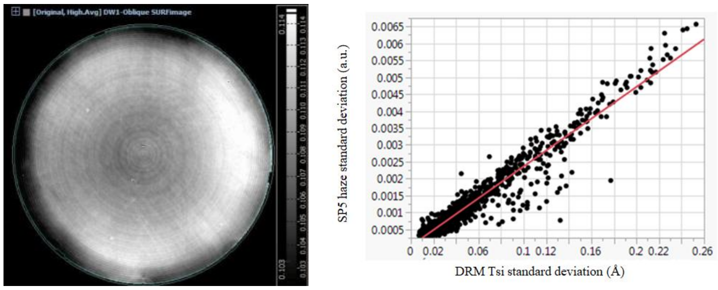

FIGURE 3. (On the left) Haze map of a 300 mm FD-SOI wafer. The gray scale corresponds to arbitrary units. (On the right) Haze to TOP thickness standard deviation correlation for 1400 data points

The overall haze map and DRM thickness map were divided in multiple fields of 15x15 mm and the standard deviation of the haze and the thickness was extracted for each field. A linear correlation with $R^2>0.9$ over more than 1000 data points was established.

This thickness proxy allows a fast T_{Si} uniformity assessment on a large population in complement to accurate thickness measurements on a limited population.

Comparison Of The Power Spectral Density Measured By DRM And AFM

FD-SOI manufacturing includes several process steps that influence the uniformity of the top silicon layer. As described in [4], one-dimensional PSD function (PSD_{1D}) is an effective characterization of roughness and thickness variations of a homogeneous and isotropic material.

We compared the PSD_{1D} from AFM scans and the PSD_{1D} from the DRM images (266µmx266 µm field of view), for finishing processes A and B. The absolute value of the PSD_{1D} and the spatial frequencies range are different: DRM is a thickness metrology and the PSD_{1D} depends on both interface variations, whereas the AFM signal characterizes the top surface height variations only. Thus for the same spatial range $PSD_{DRM} > PSD_{AFM}$. Also the DRM is covering the spatial range [1-133 µm] and the AFM [0.12-15 µm].

Despite these gaps, in line DRM metrology leads to the same conclusion as AFM on the impact of the finishing process on the PSD_{1D}. Coupling both methods we can measure the PSD on a wider range and get statistics thanks to DRM fast throughput.

As discussed above, T_{Si} control over medium and high frequency range is important to limit device to device variability: on this example process B is well suited to our application, because of lower PSD_{1D} curve. This characterization is useful to compare different product generations and drive continuous improvement.

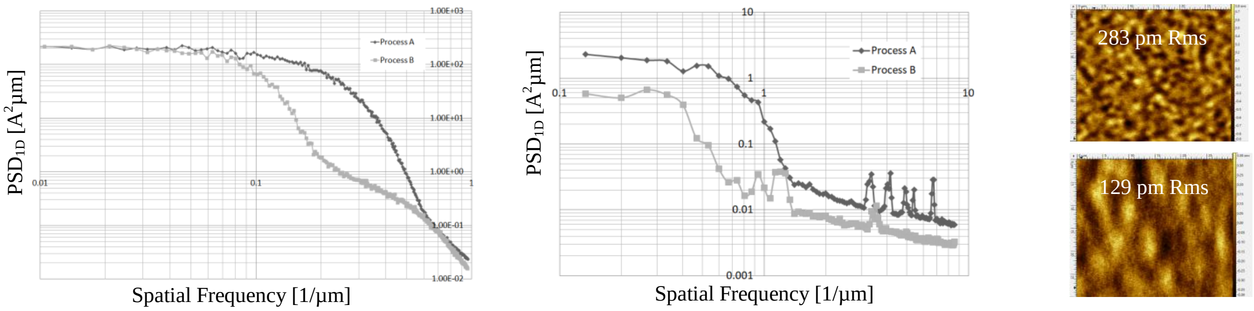

FIGURE 5. PSD_{1D} function representing the top silicon layer roughness for finishing process A and B measured by DRM (on the left) and AFM (on the right), AFM scans (30x30 µm) for process A (top right) and B (bottom right)

CONCLUSION

In this work multiple characterization methods were combined and correlated to evaluate the top silicon uniformity of FD-SOI material over a large spatial frequency range. In-line DRM metrology and its correlation with SP5 haze for low spatial frequencies and with the AFM for high spatial frequencies allows a non destructive and high throughput monitoring of FD-SOI uniformity for high volume manufacturing. Also DRM and SP5 haze monitoring enables exploring the intermediate spatial range between the AFM and Ellipsometry, correlated to the intra-die and device scale variability.

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KEYWORDS

Fully Depleted Silicon-on-Insulator, In-line Metrology, Thin Film Uniformity, Atomic Force Microscopy, Differential Reflectance Microscopy, Non Destructive Characterization

Thin films and nano-gratings study using X-ray standing waves excited by an in-lab X-ray source

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Nanofabrication technology is rapidly progressing in two directions. First, more complex 3D architecture, and second, structure sizes reduced to sub-nm scale. The state of the nanofabrication technology is already beyond the capabilities of state-of-the-art nano-metrology. The International Roadmap for Devices and Systems from 2020 assumes that implementing hybrid metrology will address this challenge. Extended scatterometry is considered a part of this hybrid metrology.

We focus our study on two scattering techniques: X-ray diffraction (XRD) and angular resolved grazing-incidence X-ray fluorescence (GIXRF). XRD is based on analyzing the far-field of X-rays scattered on the periodic structure. The GIXRF is based on the secondary scattering modulated by the near-field in the form of the 2D/3D X-ray standing wave (XSW). The XRD signal depends on the geometrical configuration of the structure, such as grating period, high and shapes. By using a grazing incidence geometry, one can tune the probe depth and its lateral position to study the buried structures at sub-nm resolution. The buried structures are then detected by fluorescence analysis, making the scheme element-specific and showing the material and its in-depth position inside the structure. Very recently, a similar measurement scheme was demonstrated to be helpful for the characterization of buried periodic 2D and 3D nanostructures[1].

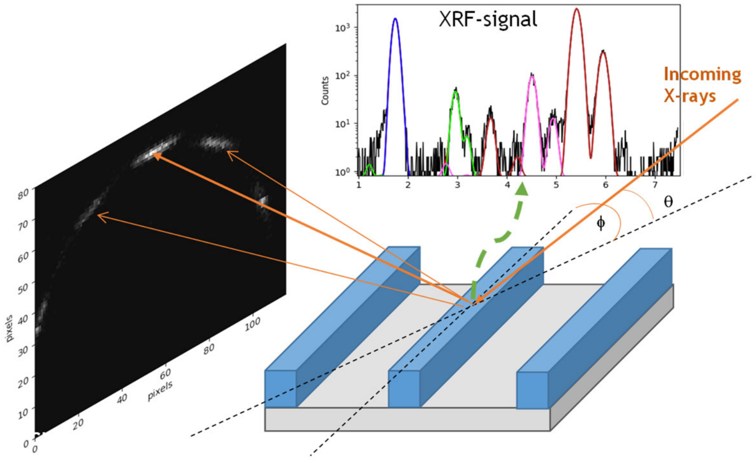
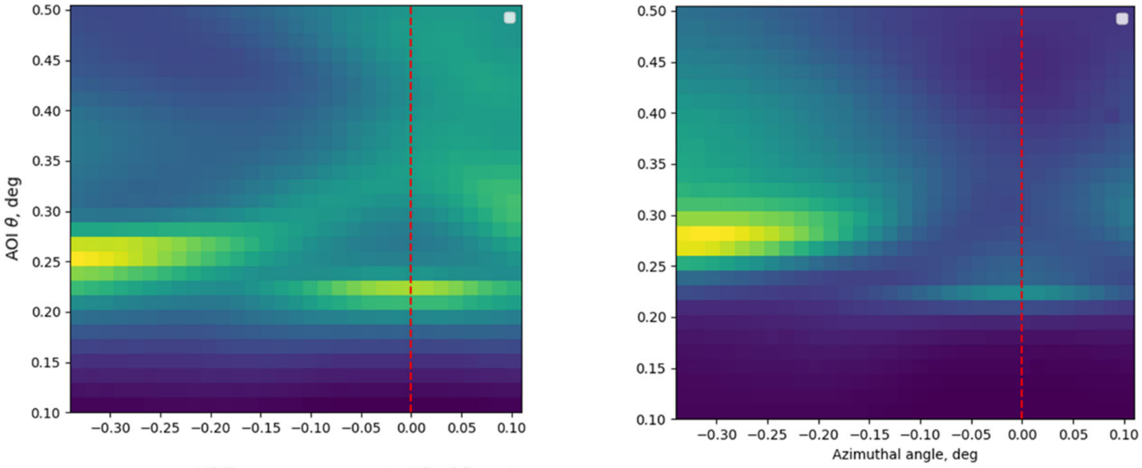


FIGURE 1. Schematic presentation of 2D XSW experiment.

We plan to extend this analysis by combining it with XRD: measuring both XRF and XRD at each incidence and azimuthal position. The measurement scheme is illustrated in Fig.1. Both XRD and GIXRF signals can be simulated using the many-beam dynamical diffraction theory. To evaluate the perspectives of an in-lab implementation of this technique, we have measured the GIXRF maps and XRD patterns from periodic nano-scale 2D gratings with various periods and marker-coatings using our laboratory XRD setup. To test this hypothesis and study the experimental measurement aspects, we recorded the angular XRF maps for TiN gratings with pitches 32, 36 and 44 nm. To increase the complexity of the sample, we have coated the gratings with a 3 nm thin Cr layer. The results of the first measurements, shown in Fig. 2, will be discussed. We will also present the initial step of GIXRF map analysis using the recently published semi-analytical approach[2], capable of relatively fast simulation of these complex XRF maps.



XRF measurements (Cr,32nm)

XRF measurements (Ti,32nm)

FIGURE 2. Measured XRF maps for TiN grating coated with 3 nm Cr.

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KEYWORDS

3D X-ray standing waves; X-ray scatterometry; hybrid X-ray characterization.

Rapid, Semi-Quantitative Elemental Depth Profiling Using Plasma Profiling Time-Of-Flight Mass Spectrometry

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INTRODUCTION

Plasma Profiling Time-Of-Flight Mass Spectrometry (PP-TOFMS) is a novel elemental depth profiling technique developed by Horiba Scientific. It couples an argon plasma source for sample sputtering and ionization with an orthogonal time-of-flight mass spectrometer. The technique delivers nanometer-scale depth profiles with high sensitivity and is capable of providing calibration-free semi-quantitative results. Moreover, the operation of the instrument is simpler and faster compared to typical SIMS instruments requiring only a few minutes including sample introduction and pumping.

The instrument is installed in a cleanroom at CEA-Leti in close proximity to process tools allowing fast feedback for materials development. The potential of this technique will be illustrated by several examples…

INSTRUMENTAL CONDITIONS

The PP-TOFMS technique couples a plasma source for sample sputtering and ionization to an orthogonal time-of-flight mass spectrometer. The plasma source uses a pulsed RF argon discharge allowing the analysis of conducting as well as insulating materials. It is typically operated at pressures around 150 Pa with an applied power of a few tens of W. Under such conditions, the sputtering rate is around 10 nm/s and the sputtering crater diameter is 4 mm. While ions are extracted continuously, counting is commonly done during the power off time where Penning ionization occur[1]. Penning ionization is far less selective than direct ionization, allowing semi-quantitative analyses via the Ion Beam Ratio method[2]. Mass spectra are easy to read as the technique mostly produces monoatomic ions. The instrument can be open to a wide range of users as user training is quick and operation is simple. This technique can therefore be used upstream of more complicated and time-consuming SIMS measurements.

APPLICATIONS

GeSbTe thin films for memory applications

Phase change random access memory (PCRAM) is a technology based on the reversible transition between a highly electrically resistive amorphous phase and a low resistivity crystalline phase of chalcogenide materials. PCRAM are already produced in advanced fabs (e.g. in Intel 3D XPoint product line) and extensive research is being conducted to improve their properties. Material properties, such as temperature stability or crystallization conditions are composition driven. Precise control of in-depth composition is thus critical for material engineering.

Figure 1 (a) illustrates the very good agreement on elemental depth profiles obtained with well-established time-of-flight mass spectrometry (TOF-SIMS) and PP-TOFMS measurements. The technique was extensively used to support the material development[3], in particular to study the effect of passivation layers to maintain a Ge-rich composition after annealing as presented Figure 2.

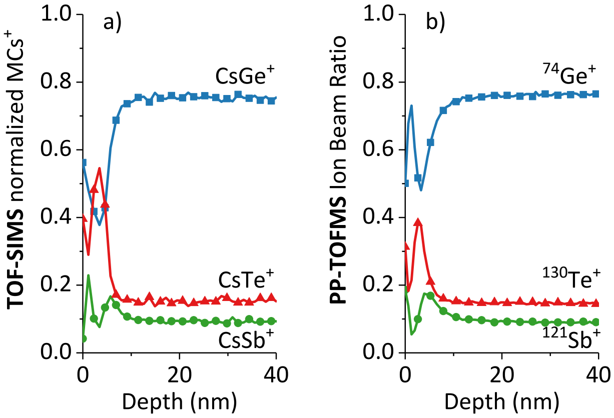

FIGURE 1. Chalcogenides atomic fractions estimated using TOF-SIMS (a) and PP-TOFMS (b).

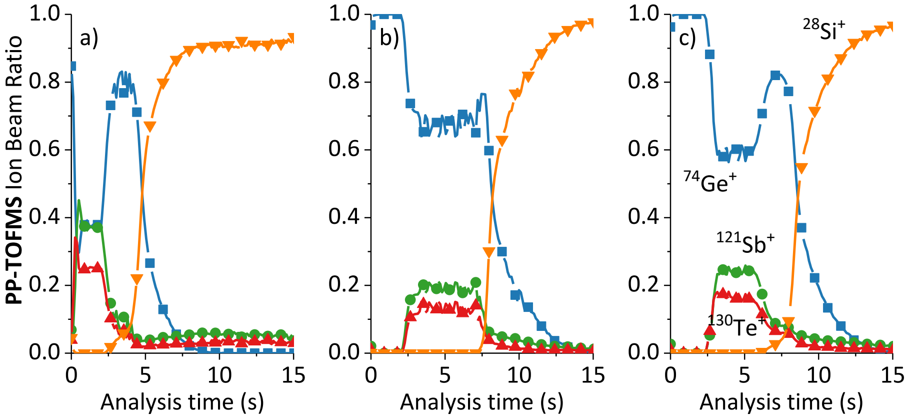

FIGURE 2. PP-TOFMS depth profiles of Ge-rich GeSbTe thin layers: after annealing without passivation layer (a), with the passivation layer (b) before and (c) after annealing.

InAlN barrier layers engineering for power applications

Due to their outstanding properties and high performance, III-nitride materials based on GaN, AlN, InN and their compounds are increasingly being used in the manufacture of high-power and optoelectronics components. However, the growth of high-quality ternary or quaternary alloys can be challenging as many process parameters need to be optimized.

We focus here on the production of InAlN barrier layers grown in close-coupled showerhead metal-organic vapor phase epitaxy (MOVPE) reactors. Figure 3 shows a superposition of PP-TOFMS and SIMS profiles for an InAlN layer on GaN. The profiles from the two different techniques match very closely in terms of Al, Ga and In relative composition[4]. This allowed PP-TOFMS profiling to be used instead of SIMS to give quick feedback about changes in process conditions to obtain an optimized recipe to minimize Ga content in InAlN layers in a showerhead reactor in a few weeks[5].

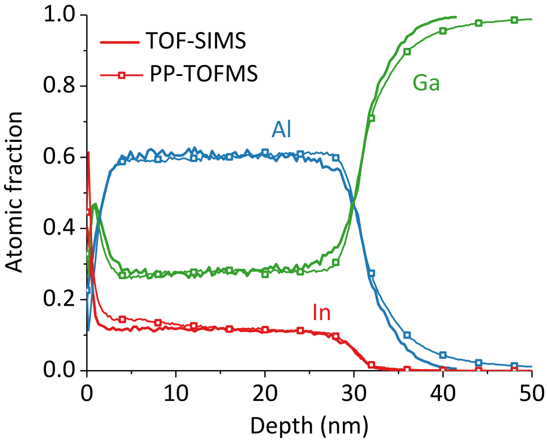

FIGURE 3. Depth profiles obtained using calibrated PP-TOFMS and TOF-SIMS measurements.

Conclusions and perspectives

In conclusion for these two cases PP-TOFMS has been shown to be complementary to SIMS analysis and is particularly useful as a cleanroom-based tool for rapid elemental depth profiling accessible by a wide user base. It may also be used to identify unknown contaminants as the mass spectra contain less molecular ions than in TOF-SIMS and are thus easier to interpret. This technique is currently being tested on a wide range of semiconductor applications.

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KEYWORDS

Depth profiling, PP-TOFMS, SIMS, TOFMS, Memory, III-N materials

Turn-Key Compressed Sensing System For Electron Microscopy

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INTRODUCTION

Compressed Sensing (CS) in serial scanning instruments involves sampling a minority fraction (i.e., 20%) of the full pixel density while allowing a faithful reconstruction of the object. A number of requirements must be satisfied to achieve a faithful reconstruction. Among these requirements is a high degree of statistical randomness in the sparse sampling strategy. Executing a highly random, high speed, precise scan pattern has presented a barrier to implementing a practical CS Scan Generator (CSSG) for electron microscopy. The sparse sampling performance is dictated by a combination of the CSSG hardware, the CS sampling strategy and scanning system dynamics.

An approach to overcome barriers to practical CS implementation in serial scanning electron microscope (SEM) or scanning transmission electron microscopes (STEM) is presented which integrates scan generator hardware specifically developed for CS, a novel and generalized CS sparse sampling strategy, and an ultra-fast reconstruction method, to form a complete CS system for electron microscopy. The system is also compatible with other serial scanning characterization techniques, such as AFM, EDS, Auger and even 3D sparse sampling applied to techniques such as laser scanning microscopy (LSM). The system is capable of producing a wide variety of highly random sparse sampling scan patterns with any fractional degree of sparsity from 0-99.9% while not requiring fast beam blanking. Reconstructing a 2kx2k or 4kx4k image requires ~150-300ms. The ultra-fast reconstruction means it is possible to view a dynamic reduced raster reconstructed image based upon a fractional real-time dose. This CS platform provides a framework to explore a rich environment of use cases in CS electron microscopy that benefit from the combination of faster acquisition and reduced probe interaction.

DESIGNING A COMPRESSED SENSING SYSTEM FOR ELECTRON MICROSCOPY

The hardware design architecture of the CSSG is dependent on the CS serial sparse sampling scan strategies, as the latter defines the requirements for the former. Evolution of the CS sparse sampling scan strategies will be described as segue into the CSSG hardware architecture overview, followed by example data.

The origins of this project reach back to 2012 when Synchrotron Research Inc. (SRI) was seeking to use CS as part of a scanning option on a hyperspectral imaging NEXAFS spectrometer developed by SRI for the NIST beamline suite, now operating at NSLS II. CS for electron microscopy concepts progressed steadily over time through NIST funding[1] and methods were written which permitted the simulation of theoretical sparse sampling patterns and CS reconstruction. As best methods crystallized, it became clear a custom scan generator would yield optimal performance, while simultaneously allowing the greatest experimental liberty to explore CS electron microscopy. The envisioned hardware became reality when funding to fabricate the CSSG hardware was supported by the Sensors Directorate of Air Force Research Labs (AFRL/RYD) under Contract No. FA8650-18-C-1201. External hardware interfaces were developed and the CS software reconstruction methods were integrated into a universal control platform with a Python-based user interface.

Evolution Of An Idealized Compressed Sensing Matrix For Electron Microscopy

As mentioned, one of the common issues when designing a CS serial scan strategy is to mitigate effects tied to scan system dynamics[2]. To minimize hysteresis, slew and other scan distortions, CS scan matrices were explored which ensured predominantly smooth and largely continuous scan pattern properties. Space-filling curves (SFCs) represent a family of topological curves which possess such properties. It was found through simulated reconstruction that SFCs in general "worked", but as a mathematical family are prone to non-idealities when applied directly as a CS sampling matrix. Namely, SFCs are pseudo random, which does not satisfy a highly statistically random sampling. SFCs are also discretized in degree of sparsity, as dictated by the order of the SFC and the pixel density. Invoking a random perturbation about the indices of any SFC was found, again through simulation, to improve the reconstruction performance but still did not optimize the randomness, nor eliminate the discretization in scan sparsity.

The "final solution" was to employ the SFC as a "slow" carrier signal modulated by a "fast" randomized perturbation signal. In this manner, by combining the "slow" continuous carrier and "fast" random modulation, a programmatic highly randomized pattern may be invoked with any fractional degree of sparsity and with a high geometrical degree of freedom (DOF) in 2D or 3D. The DOF enables by this method is a distinct advantage over line-hopping methods applied to CS electron microscopy[3]. The ratio of work performed by the carrier signal relative to the randomized modulated signal may be regulated as one of multiple handles to accommodate physical constraints of native hardware, such as amplifier circuits and scan coil response. Sparse sampling paths are optionally smoothed with a maximum curvature driven by the scan criteria, and random perturbations are not restricted to vertices. Note, the schema does not generally require any beam blanking along the scan path! Conceptually, a continuous (seamless) montage pattern may also be formed by extending the fill area in contiguous blocks. The fill blocks do not need to be orthogonal, square or even Euclidean (i.e., fill primitives can be triangles, circles, or non-Euclidean geometries.). The system is compatible with scan paths which do require beam blanking, such as so-called "fly-back" scan patterns. A wide variety of SFCs may be applied with this system, including serpentine curves, spiral curves, Lissajous curves and other parametric curves. Given a-priori information derived from either lower resolution full field imaging data (i.e., optical image) or digital design files (i.e., GDSII) congestion maps can guide adaptive sparse sampling strategies which dynamically adjust sparsity and pixel density to significantly optimize the information collection efficiency.

Key Features Of The CSSG Architecture

The design objective was a state-of-art CS scan generator which would match or exceed capabilities of any electron microscope platform on the current market. The CSSG is FPGA-based with a PCIe bus architecture operating with 24-bit 50MHz hardware. The effective number of bits will be limited by the electronics (i.e., scan amplifiers) on the native SEM/STEM/FIB. Each "fast" randomized modulated signal converter is referenced to a "slow" carrier signal converter to form a compound carrier-modulator output. Four compound carrier-modulator DACs standard on each CSSG can control two columns simultaneously (i.e., FIB-SEM) at full speed, or two pair of scan coils on a STEM, or a X-Y-Z CS scan on a 3D LSM. The FPGA functions as a bi-directional 50MHz data pipe synchronizing the outgoing DAC signals controlling the scan pattern with the incoming 12-bit ADC signals from SE detectors, BSE detectors or electrical probes. Up to eight ADCs can be combined for simultaneous detection, all synchronized with the scanning signal. There are 12 GPIO ports for logic control. There is an automated built-in signal-to-noise ratio (SNR) function which will truncate the dwell time within ~140ns of a pre-determined SNR value being reached. This SNR function can further reduce CS acquisition time. Dwell times range from 20ns – 20.97ms. All scans are vector-based. Any generalized set of points may be user programmed as input. The CSSG hardware is housed in a small form factor thermally stabilized GPU style enclosure.

Interfacing the CSSG is similar to any EDS or external scan generator for electron beam lithography. A Python-based GUI allow users to control basic microscope functions, including stage control for montage acquisition and basic column control. An API is available for extensibility and custom development.

CSSG Results & Discussion

Panels CS-1 through CS-4 a of Figure 1) show a series of compressively sensed images. CS-1 and CS-2 were acquired at 80% sparsity in a 2Kx2K pixel array and CS-3 and CS-4 were acquired at 90% sparsity in a 4Kx4K array. It challenging to graphically display highly sparse sampled data, but features can be correlated to the reconstructed images RI-1 through RI-4 on the right side of the graphic. CS/RI-1 and CS/RI-2 are overlapping regions from a gold-on-carbon specimen acquired on a thermal emitter and Everhart-Thornley style secondary electron detector. CS-1 is 80% sparse, ~25um FOV and 12.2nm pixel size. CS-2 is an 80% sparse 5x5 serpentine montage, and the blue solid line and red dots representing the montage tile path are for visualization purposes only. Each montage tile is 6.1um FOV and 3.1nm pixel size. Comparing varying pixel size for the same sparsity in the ROI is a method to compare CS sampling parameters. CS-3 and CS-4 are 90% sparsity sampling images on a regular grid acquired on a Schottky field emitter platform using a through-lens detector. All scans shown were performed using a Hilbert style SFC.

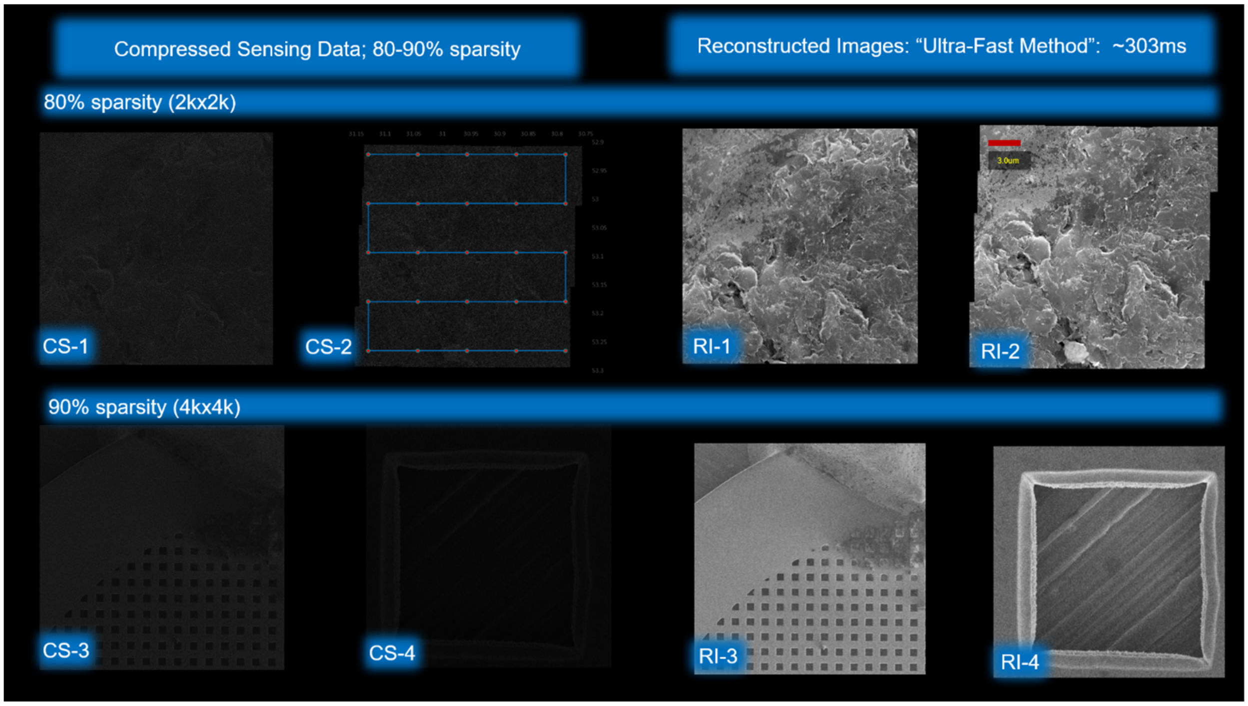

FIGURE 1. Compressively Sensed scanning electron microscope images are shown on the left (CS- #) and corresponding Reconstructed Images (RI-#) are shown on the right half of the graphic. See text for details.

A near real-time validation module currently in field testing estimates the resolution from the Fourier transform of the sparse data and the SNR from the Gaussian noise estimated from eigenvalues of the patch covariance. A second diagnostic module in field testing measures scan distortions from the microscope. The inverted pre-distortion fields are then applied through the CSSG to acquire a distortion corrected sparsely sampled scan. A third functional module in field testing measures the point spread function (PSF) of the microscope and applies this PSF kernel in post processing to correct beam distortions. In future, these modules could function as part of a health monitoring schema to track platform performance. Early adopters are being sought for collaboration.

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KEYWORDS

Compressed Sensing, Sparse Sampling, Electron Microscopy

SEM Charging of Floating Metal Structures in Dielectric

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INTRODUCTION

Emerging recording head technologies in the hard disc drive industry require high throughput metrology on the sub-nanometer length scales. [1] Heat Assisted Magnetic Recording (HAMR) incorporates metallic structures isolated in dielectric [2], and these floating structures present challenges when imaging in the Scanning Electron Microscope (SEM). (Figure 1A) The metallic features, often with sharp corners, charge up under electron beam irradiation, leading to degraded image quality and arcing discharge events that can damage the tool. [3, 4] In this study, the charge and electric field build-up and mitigation of these floating metal features is investigated. Metallic sheet films (Figure 1B) provide insight into the penetration depth of the electrons and the optimal image quality that can be achieved for grounded features. Floating metallic structures with the built-in ability to controllably leak electron current showed the shape-dependence of the charging. The experimental results were compared to SEM simulations to understand how the electron beam parameters were interacting with the sample. Using these insights, guidelines for imaging the floating metal structures were developed.

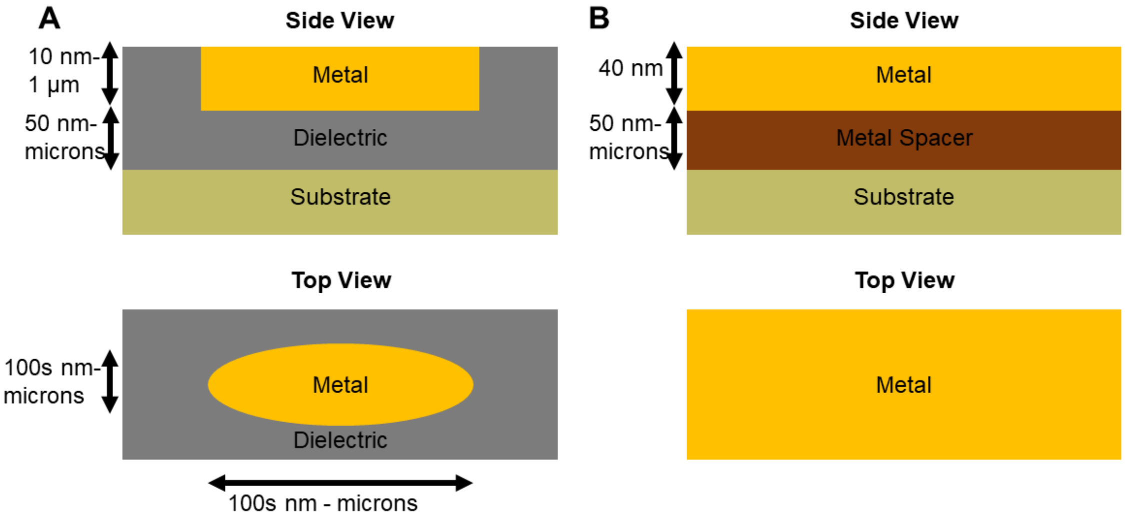

FIGURE 1. Schematics of A) floating metal structure often produced when making HAMR recording heads and B) sheet film wafers used to understand electron beam interaction with metal films

SEM IMAGING AND SIMULATION RESULTS

Exploring and understanding SEM images of floating metal features was done through a combination of experimental imaging and simulation. The SEM imaging was performed on a KLA e-beam Wafer Defect Review (eDR®) tool. Electron beam paths were simulated using Casino software. SEM image and charging simulations were performed with proprietary custom software.

Gold Sheetfilm Studies

Optimizing and understanding the imaging of a gold sheetfilm provides a controlled baseline prior to imaging floating structures of unique shapes. Imaging the gold sheetfilm with trace dopants in backscatter mode revealed ~25 nm circular grains at both 1.5 and 5.7 keV landing energy (Figure 2A and 2C). Since the landing energy controls the depth of e-beam penetration, the same observed grain size at the two landing energies suggests the grains were columnar in geometry. E-beam path simulations on 40 nm Au films with 1000 electrons reveals that 1.5 keV landing energy only provides signal from the top 5 nm while the 5.7 keV landing energy gets signal from almost the entire 40 nm volume. (Figure 2B and 2D) The fraction of signal from back scattered electrons gradually shifts from a sharp peak around 2.5 nm for 1.5 keV landing energy to a more even distribution across the 40 nm film for 5.7 keV landing energy. (Figure 2E) The average spatial distance of the backscatter event from the center of the e-beam also increases with landing energy, going from 2 nm average spatial spread at 1.5 keV to 12 nm average spatial spread at 5.7 keV.

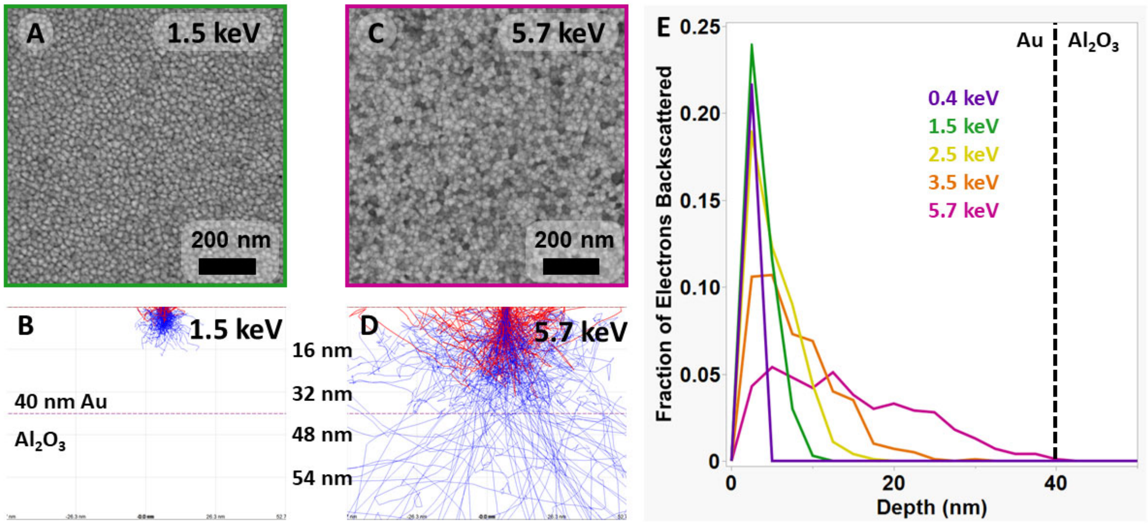

FIGURE 2. SEM of Au Sheetfilms A) Backscatter SEM imaging of the Au Sheetfilm at a landing energy of 1.5 keV. Roughly 25 nm diameter grains are seen. B) Electron pathway simulations show the backscattered (red) and buried (blue) electron paths for 1.5 keV landing energy in 40 nm of Au on Al_2O_3. C) Backscatter SEM imaging of the Au Sheetfilm at a landing energy of 5.7 keV. Roughly 25 nm diameter grains are seen. B) Electron pathway simulations shows the backscattered (red) and buried (blue) electron paths for 5.7 keV landing energy in 40 nm of Au on Al_2O_3. E) The backscattered electrons' distribution of depths based on the landing energy of the electron beam.

Floating Gold Structures in Dielectric

The size, shape, and proximity of nearby metal features can strongly influence the charging of floating metal features. The optimal landing energy to maximize contrast difference between the gold feature and the surrounding aluminum oxide dielectric can be simulated first without charging. The optimal contrast for backscatter imaging qualitatively looks to be at landing energies between 1.5 and 3.5 keV. This landing energy provides the sharpest feature boundaries, but the imaging becomes more complicated when charging effects are included.

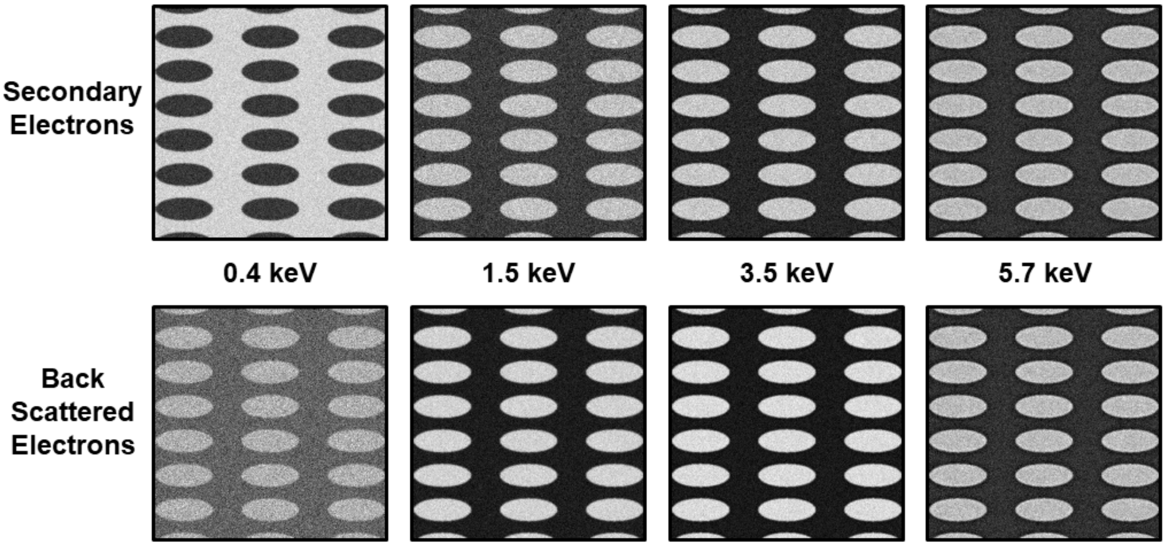

FIGURE 3. Simulated SEM images without charging effects for floating Au features in Aluminum Oxide.

Using a wafer build that can control the electron current leakage from floating metal structures in dielectric, the effects of shape and local structures can be explored. Imaging floating shapes with various degrees of curvature and sharpness reveals how the feature shape affects the charge build-up in imaging. Placing oval features floating at different distances from each other shows the effect of feature distance for the charge build-up. The experimental results can be correlated with simulations to provide understanding of the interaction between the e-beam and the floating features. This insight can inform the SEM imaging of floating features in hard disc drive recording head production and R&D.

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KEYWORDS

SEM, floating structures, metals, dielectric, SEM Image Simulation, HAMR

An Analysis Of Polymer Nanoparticle Size Distribution Using Cryo-EM And A Comparison To Other Techniques

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INTRODUCTION

Particulate contamination in semiconductor manufacturing processes is polydisperse in nature, with the typical distribution skewed mainly towards particle sizes < 20 nm. As advances are made in the lithographic patterning process, and critical defect size continues to shrink, particles as small as 5 nm can cause a killer defect. However, for sub-15nm nanoparticles, neither the most advanced wafer scanner (Surfscan SP7, for example) nor liquid particle counters can detect them during the production processes. Therefore, to decrease the possible defects, chip makers increasingly demand the most aggressive filtration capabilities that remove the particles that cannot be seen.

To evaluate the performance of advanced filters and mimic the behavior of natural polydisperse particles, we developed the fluorescent polystyrene nanoparticles (G25) method [1]. This technique is now confirmed as a robust test method for sub-10nm filters. At these dimensions, a correct understanding of the particle size distribution (PSD) of G25 becomes critical. Unfortunately, when the size of the polymer nanoparticles is less than 10 nm, it is challenging to get reliable size distribution data.

This paper describes the study of G25 particle size distribution (PSD) using different techniques such as the Atomic Force Microscope (AFM), the Scanning Mobility Particle Sizer[2] (SMPS), Dynamic Light Scattering (DLS), and Cryo-Electron Microscopy (Cryo-EM)[3]. Among these tools, Cryo-EM is confirmed as the most powerful structure determining technique that is well-suited to studying polymer nanoparticles in solution. Most importantly, the frozen-hydrated sample preparation allows the specimens to be kept and imaged in a state closest to how they naturally appear in water (native status). More specifically, the images show a snapshot of how the particles exist in solution. Furthermore, the high-resolution photos make it possible to detect the polymer particles down to 1 nm.

Based on the analysis from dozens of Cryo-EM images, we concluded that G25 is a polydisperse particle ranging from 1 nm to 40 nm. Furthermore, the most significant particle size population is around 10 nm. This finding agrees with DLS results (the number weighted PSD). The SMPS method shows the particle number "power function" increases with a decreasing particle size. Most people agree with this "power function" theory, but is it true? This paper will reveal the correct PSD of G25 and compare the four techniques which can be used for sub-10 nm nanoparticles analysis.

EXPERIMANTAL

Instruments:

- Thermo Scientific Talos Arctica Cryo-TEM
- FastScan AFM (Bruker)
- TSI Model 3936 SMPS
- Dynamic Lighter Scattering (DLS)

Samples:

- Thermo Fisher Scientific Fluorescent polystyrene latex (G25 PSL) beads, De-ionized water (DIW)

RESULTS AND DISCUSSIONS

Size distribution study with different methods

1. DLS results

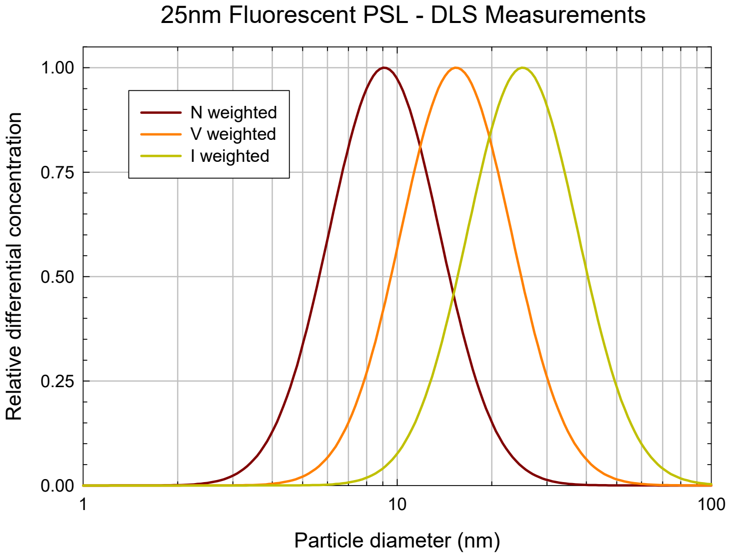

FIGURE 1. G25 particle size distribution collected with DLS. Green is Intensity weighted size distribution which can be converted into Volume (red) and Number (dark purple) weighted sized distributions.

DLS is one of the most popular light scattering techniques for measuring molecules, particle size, and size distribution because it is non-invasive and well-established. In addition, it allows particle sizes of down to 1 nm in diameter. However, it cannot provide good size distribution data for polydisperse nanoparticles. The scattering light intensity weighted size distribution (green curve) in Figure 1 shows the PSD for G25 where the average size is 25 nm. While this agrees with the vendor's datasheet, when converted to number weighted PSD (purple curve), the average size decreases to 9 nm and the peak shifts in the 1 nm direction (16 nm difference!). The peak shift indicates the particles are polydisperse. In addition, for contamination control in semiconductor processes, we count defect numbers. Only the number weighted size distribution needs to be considered. Any of the PSD discussed later in this paper are all number-weighted unless otherwise specified.

2. AFM test

The spherical PSL beads are suitable to be measured by the AFM technique because the AFM measures height. In this study, the wafer surface is used for the sample preparation; 100 5×5 um images were scanned and analyzed. Unfortunately, the AFM can only provide topographic photos, and it cannot differentiate which particles are the target ones. In addition, any dissolved non-volatile residue (NVR) in the solution could interfere with the results.

3. Scanning mobility particle sizer (SMPS) [2]

An ultrafine nebulizer and a scanning mobility particle sizer (SMPS) are used for collecting G25 particle sizes and its PSD. The aerosol PSD is measured using a SMPS system capable of measuring particles as small as 5 nm in size. In this technique, dissolved NVR in the sample will also form particles when the droplets from the nebulizer are dried. These residues can negatively increase the number of smaller sized particles. The key technique in this measurement is the nebulizer; it should have no more than one particle in each droplet. The nebulizer must produce small, uniformly sized droplets to prevent interference with the particle analysis. However, the dissolved non-volatile residues in the solution increase the number of small nanoparticles. A diluted sample will decrease this NVR interference. However, if the sample contains salts or surfactants, it cannot provide reliable data in a small particle size range (<8 nm).

4. Cryo-EM test

To better understand the PSD of G25, Thermo Scientific Talos Arctica Cryo-EM is used for collecting images of the nanoparticles in close to native status in water. Typical images of G25 are shown in Figure 2. This confirms that the particles are spherical.

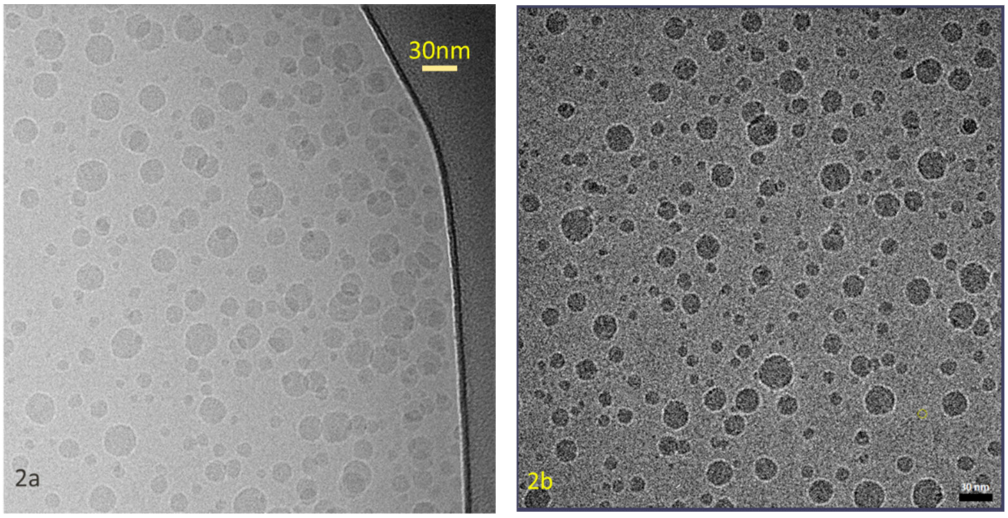

FIGURE 2. Two Cryo-EM images with different contrasts, the left image 2a is the original image; a high contrast image on the right (2b) makes measuring and finding the particles easy.

In Figure 2a, the black area is the grid for holding the ice film. As you can see, more particles are found close to the grid due to the thickness of the ice film. The water surface tension makes the film edge thicker than the center area of the film. Figure 2b shows relative uniform particles that are dispersed in the film away from the edge. Usually, the average of the ice film is about 100 nm. In Figure 2a, fewer overlapped particles are found in the area on the left because it is far from the edge. For the study of PSD, a total of 40 Cryo-EM G25 images were analyzed. The size distribution is shown in Figure 3.

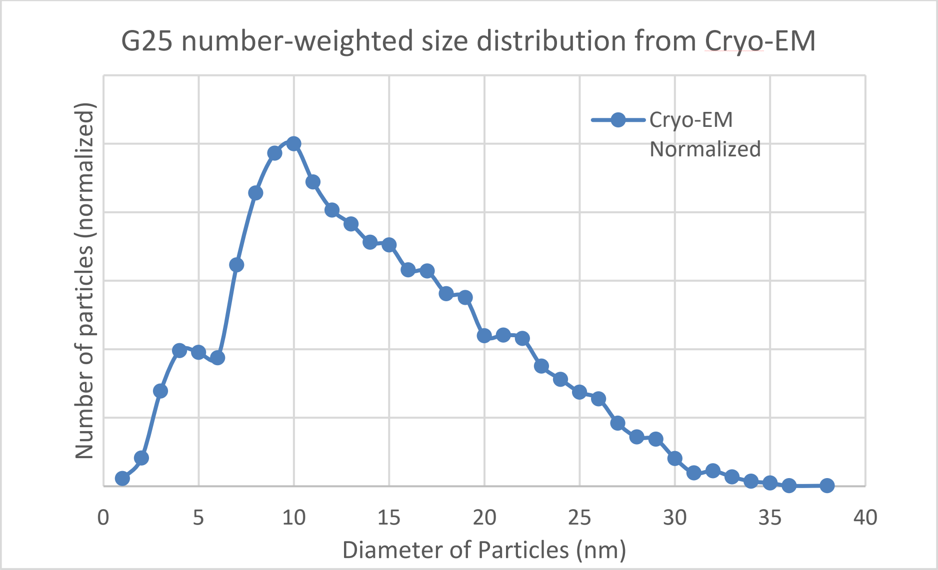

FIGURE 3. G25 particle size distribution based on Cryo-EM image analysis.

Discussions

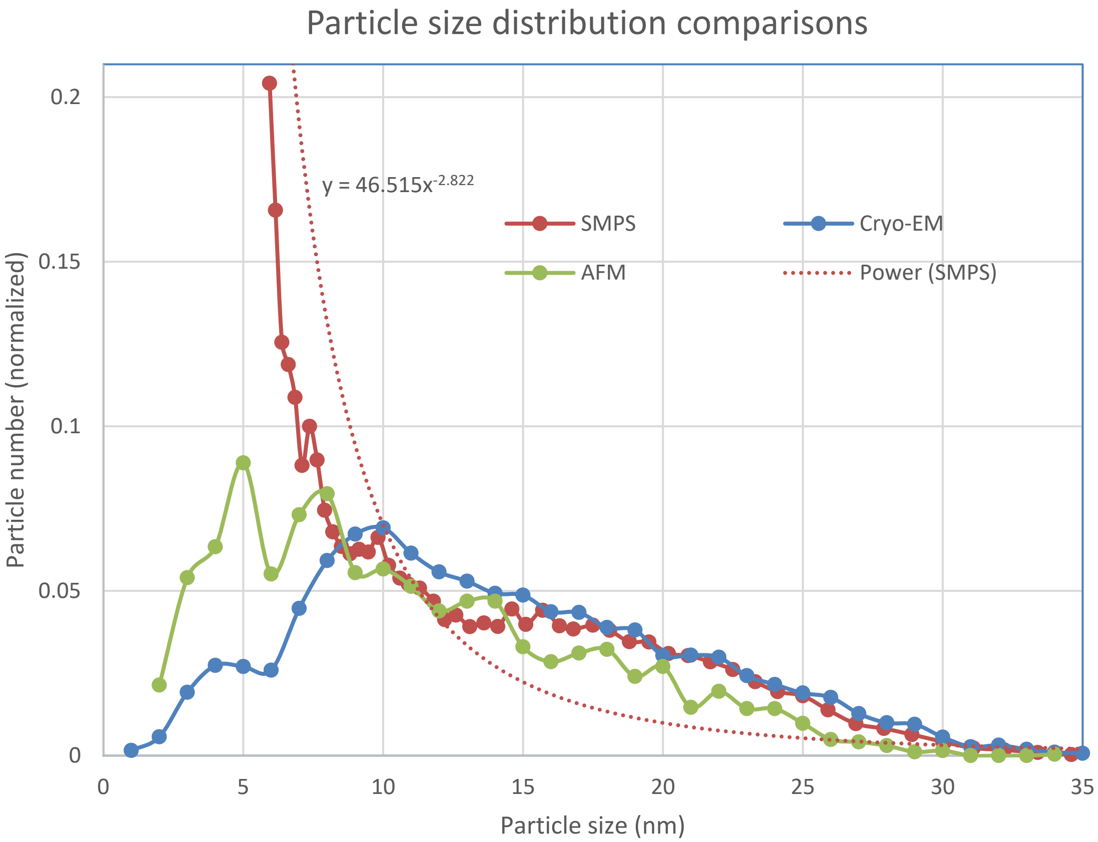

FIGURE 4. Overlapped graph of three PSD results of different techniques (Cryo-EM, SMPS, and AFM).

Among the four techniques, DLS is the most convenient and cheapest; it provides an average size of 9 nm for G25 particles. However, it does not provide reliable PSD data due to the sample's polydisperse nature.

Figure 4 shows a comparison of the other three test methods. Interestingly, three curves intersect at 8 nm. When the particle size is bigger than 8 nm, three results show the same trend. However, when the size is less than 8 nm, the trends show quite a large difference. For Cryo-EM and AFM, both results have a decreasing trend when the particle size is smaller than 8 nm. The SMPS technique shows the number of particles increases similarly to a power-function (red dot in Figure 4) as the size decreases. The reason for this dramatic particle number increase is due to the dissolved NVR in the solution that form particles when the droplets from the atomizer are dried. The G25 sample cannot avoid the dissolved NVR issue because the solution contains surfactants and some ions that act as stabilizers to the particles. The SMPS data could be misleading because the "power-function" theory is often incorrectly adopted when particles become smaller.

Although the AFM test method is also facing dissolved NVR problems, its PSD does not show the power-function curve. Dissolved NVR could form particles on the surface when the sample is dried that are mistaken by the AFM as G25 particles. The PSD data shows this interference differently than the SMPS method. In the smaller size range (< 8 nm) the AFM performs better than SMPS, it shows a similar trend as Cryo-EM does. However, there are some interferences. In addition, the AFM method is very time-consuming, and it cannot differentiate particles from residues.

Based on these results, we conclude that the three methods agree when size > 8 nm. However, only cryo-EM can show the correct results for smaller particles (<8 nm). This is because this methodology has no dissolved NVR issues. Therefore, Cryo-EM is the best method to measure the size of polymer nanoparticles. Also, it can monitor if the particles are aggregated or not.

As a summary, Table 1 shows a comparison of the four methods.

TABLE 1. Four technique comparisons

Techniques	Cryo-EM	AFM	DLS	SMPS
1. Detectable size	Sub-1 nm	1 nm	1 nm	3-5 nm
2. NVR interference	No	Yes	No	Yes, strong
3. PSD study	Excellent	Possible	Not good for wide dispersed sample	>8 nm, ok
4. Test times	long	Longest	Fast	Good
5. Particles in Native	yes	no	yes	No
6. Cost	Expensive	Fair	Inexpensive & easy	Inexpensive
7. Sample concentration	>100 ppm	ppt -ppb	>1 ppm	ppb

CONCLUSION

Four critical techniques that can detect sub-10 nm nanoparticles are studied and compared using polydisperse polystyrene beads (G25). DLS is the easiest method to get the average size. When the two peaks of I-weighted and N-weighed PSD have a difference, it implies polydisperse particles are in the system. An AFM may be used to analyze PSD for spherical particles; dissolved NVR will interfere with the results when the particles are smaller than 8 nm. SMPS is a practical and popular method for aqueous samples in the semiconductor industry. However, it is like the AFM method in that the dissolved NVR will affect the results. In the G25 case, SMPS results could be misleading when the size is less than 8 nm. Cryo-EM provides more accurate results and shows a snapshot of the particles in their natural state which is the best method to characterize small polymer nanoparticles. Interestingly, the results show when particle size is bigger than 8 nm, the three tools, except DLS, show similar results. In the small size range (<8 nm), Cryo-EM shows the best results.

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KEYWORDS

Polymer Nanoparticles, Particle Size distribution (PSD), Cryo-EM, Filtration, AFM, Contamination control, DLS, SMPS

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Actinic EUV Mask Inspection via Coherent Diffractive Imaging Using Tabletop High Harmonic Sources

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INTRODUCTION

As extreme ultraviolet (EUV) lithography is moving to high volume manufacturing, the fabrication and inspection of defect-free EUV masks remains one of the most critical and challenging issues in EUV metrology **[1-6]**. Although some inspection can be done using DUV or electron beams, non-actinic inspection techniques struggle with low spatial resolution and/or exaggeration or distortion of the actual impact of photomask defects on patterned wafers. For example, it has been demonstrated that a photomask defect detected by electron beams results in no impact on the patterned wafer **[1]**. Consequently, an EUV actinic inspection tool is extremely attractive for inspection of the printability of EUV mask defects, as well as for in-fab monitoring for possible defects emerging from extended use.

Several technologies can be used for actinic EUV mask inspection. First, traditional EUV zone plate microscopy can inspect EUV masks with relatively high sensitivity and throughput **[3]**. But they can only provide amplitude images, *i.e.*, no phase information, with resolution limited by the zone plate fidelity. Direct imaging with reflective optics is also possible, but with extreme demands on the optical figure and alignment **[4]**. In contrast, coherent diffractive imaging (CDI) is a lensless imaging technique that allows phase-contrast, aberration-free and high-resolution imaging of semiconductor samples, including EUV photomasks **[9-12]**. High-NA, diffraction-limited resolution can provide an unprecedented view of masks, making it possible to identify sub-threshold mask features that may evolve into printed defects. Furthermore, the phase information inherent in CDI imaging is very beneficial to numerical simulation tools for EUV technologies. CDI has been used with synchrotron radiation to produce high quality images of EUV photomasks **[2,5]**—however, these sources have limited access. High harmonic generation **[7,8]** is a promising alternative to synchrotrons that can provide bright and coherent EUV light at 13.5nm. By combining HHG and CDI, it is possible to implement actinic EUV mask inspection on a tabletop scale setup and at a reasonable cost. Although researchers have demonstrated simple CDI analysis of nm-scale features, as well as image reconstruction of um-scale features **[6]**, a versatile tabletop-scale tool for actinic EUV mask microscopy remains to be implemented.

We are developing such a tabletop actinic EUV mask inspection system. Currently, the system has demonstrated CDI imaging using visible-wavelength illumination through the EUV optical path and is in process of being integrated with an engineered coherent 13.5nm EUV HHG source.

CONFIGURATION OF THE TABLETOP ACTINIC EUV MASK INSPECTION SYSTEM

The system we are developing—the TEAMS (Tabletop EUV Actinic Microscope System)— is shown in Figure 1(a). The driving laser is a commercial ultrafast Ti:sapphire laser (KMLabs RAEA^{TM}), which generates ultrafast laser pulses at ~790nm wavelength, with 30fs pulse duration and 3mJ pulse energy at 5kHz repetition rate. HHG upconversion is accomplished using a KMLabs XUUS$_5$, using a waveguide filled with ~1 atm helium gas as the high harmonic upconversion medium to generate bright and coherent EUV light around 13.5nm. After filtering-out the pump laser, the system relies on multilayer mirrors to select the appropriate 13.5 nm wavelength, with bandwidth ~1 eV. A diagnostic beamline with a switchable mirror serves to optimize the coherent illumination. The configuration of the actual EUV imaging system is shown in figure 1(b). A Mo/Si multilayer curved mirror (CM) and flat mirror (FM) focus and direct the beam onto the mask at a 6° angle of incidence. Past imaging using the same source and focusing resulted in an illumination spot of ~1.4 µm diameter [11]. The reflected and diffracted EUV light is captured by an EUV CCD sensor, which was mounted 40mm below the EUV photomask. The movement of the EUV photomask and the EUV beam is accomplished by two sets of stages. First, the EUV photomask is mounted on a 2-axis 200-mm motion stage with ~1µm precision for coarse positioning. Second, the CM is mounted on a set of 3-axis piezomotor stage, with ~10s nm repeatability, which is responsible for scanning the beam over a small area to perform the CDI scan. The overall illumination geometry is estimated to have a ~40% efficiency from source to mask, and the spatial resolution, based on the NA of scattered light collection, is calculated to be <20 nm (actual resolution, not scaled for stepper demagnification).

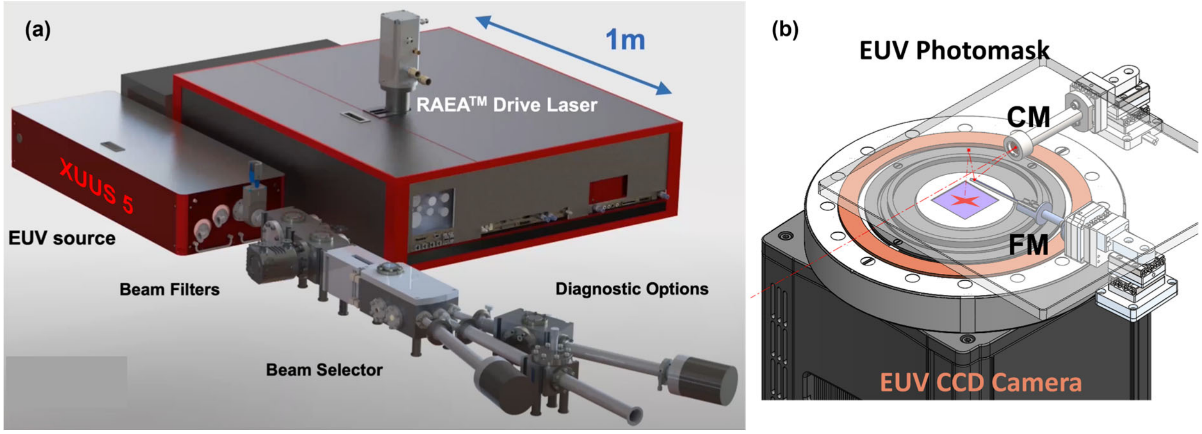

FIGURE 1. Configuration of the tabletop actinic EUV photomask inspection system. (a) A tabletop coherent EUV laser system via high harmonic generation. The inset shows a typical He harmonic spectrum. (b) A schematic of EUV photomask imaging microscope via CDI.

TEAMS SYSTEM PRELIMINARY DEMONSTRATIONS

CDI replaces image-forming optics with a computational algorithm that iteratively applies constraints in real and reciprocal space and reconstructs phase-sensitive and aberration-free images of samples with diffraction-limited resolution. Furthermore, CDI ptychography [9] has proven to be very robust for image reconstruction under a wide variety of conditions. In ptychography, the beam is scanned relative to a sample while keeping large area overlap between adjacent scan positions. Diffraction patterns are recorded on a 2D pixel-array detector at each position. This creates enough information redundancy in the dataset to allow for fast and robust reconstruction of the sample image as well as the illumination beam.

The reconstruction algorithms are wavelength agnostic, providing diffraction-limited resolution that scales directly with wavelength. This allows us to demonstrate and fine-tune the system initially using visible illumination. Figure 2(a) shows a reconstruction using He-Ne laser illumination at λ=632nm wavelength and a USAF 1951 test target. This image indeed faithfully reconstructs with an image resolution of 8µm. In a second demonstration, we used a diode laser at λ=450nm to image a semiconductor test sample provided by iMEC **[12]** with 3.6µm resolution, shown in Fig. 2(b). This sample has features with size close to the diffraction limit at the illumination wavelength -- here the image quality and resolution could be improved by a factor of 2-4 by increased SNR, i.e., longer exposures and camera cooling.

Progressively using shorter-wavelength illumination allows us to obtain accurate calibration parameters and procedures and to refine the CDI reconstruction algorithm. Our next step is to use EUV illumination. Since previous work using 13.5 nm illumination in a simpler, transmission-mode geometry demonstrated diffraction-limited 12.6 nm resolution, and since imaging using visible illumination has demonstrated the requisite field curvature correction, we anticipate obtaining near diffraction-limited resolution images in the near future.

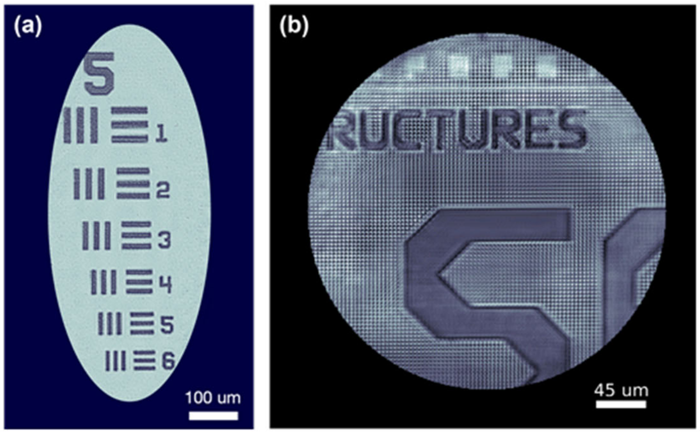

FIGURE 2. Preliminary demonstrations of our CDI microscope using visible lasers and test targets. (a) An amplitude image of a USAF 1951 test target taken with a He-Ne laser at 632nm wavelength. (b) An amplitude image of a semiconductor test sample from iMEC taken with a diode laser at 450nm wavelength.

SUMMARY AND FUTURE WORK

In summary, we have built a tabletop EUV photomask inspection system based on ptychographic imaging and a tabletop coherent 13.5nm laser source. We are in process of system validation and expect to perform actinic EUV photomask imaging and inspection in the near future.

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KEYWORDS

EUV, mask inspection, HHG, high harmonic generation, CDI, ptychography

Localization Microscopy for Process Control in Nanoelectronic Manufacturing

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INTRODUCTION

Optical microscopy beyond the resolution limit enables critical measurements in nanoelectronic manufacturing. At the state of the art, scatterfield microscopy is a mature method of quantifying target dimensions and overlay, combining prior knowledge of target structures, optical models, and microscope calibrations to achieve parametric uncertainty of less than one nanometer and total uncertainty of a few nanometers.[1] In comparison, localization microscopy is a maturing method of imaging and tracking with diverse applications,[2] combining prior knowledge of sparse structures, optical models, and microscope calibrations to achieve localization precision of less than one nanometer and total uncertainty of a few nanometers.[3,4,5] Although localization microscopy is largely unexplored in the context of nanoelectronic manufacturing, the method has significant potential for characterization of lithographic materials, localization of device features, and detection of interfacial defects, among other possibilities.[6,7] A critical issue to address, however, is the need for a traceable and total uncertainty of less than one nanometer, throughout a focal volume of considerable extent, to exploit the high throughput that is possible by optical microscopy.

In the localization analysis of a point source, random effects, such as from a finite count of signal photons and mechanical vibration of microscope parts, yield uncertainty components that can be far less than one nanometer,[8] limiting localization *precision*. However, systematic effects, such as from variation of magnification across imaging fields and experimental conditions,[9] and mismatch between model and experimental point spread functions, can become orders of magnitude larger, limiting localization *accuracy*. Such an extreme discrepancy between precision and accuracy would be intolerable to feature localization or defect detection for process control. Moreover, claims of localization traceability to the International System of Units (SI) are challenging to validate, further limiting the reliability of position data, and potentially confounding the registration of features across multiple nanofabrication and microscopy systems. The root cause of this problem is the lack of standards and calibrations that are fit for the purpose of achieving a traceable and total uncertainty of less than one nanometer in localization microscopy.

To address this issue, we are developing nanostructure arrays that provide reference positions throughout the focal volume of an optical microscope, enabling its calibration. A central goal of our work is to achieve accuracy and efficiency in the fabrication and measurement of such standards, which involves representative aspects of process control. In a previous study,[3] we tested the accuracy of electron-beam lithography to place nanoscale apertures in rectilinear arrays. Two lithography systems each used two interferometers to measure stage positions and correct for electron–optical aberrations within the patterning process. By localizing apertures and comparing arrays from the two

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systems, we estimated a difference of mean distance between apertures of one part in five thousand, or approximately one nanometer, and a standard deviation of the distances between apertures of a few nanometers from random effects during lithographic pattern transfer. In a recent study,[5] we validated our estimate of array pitch using critical-dimension atomic-force microscopy,[10] which is traceable to the SI, and we propagated scale uncertainty to establish a traceable and total uncertainty of less than one nanometer across an imaging field of a certain extent.

In the present abstract, we briefly summarize the traceable validation[5] of an aperture array that we fabricated by electron-beam lithography,[3] confirming fabrication accuracy and yielding a master standard that enables a new test of placement errors from focused-ion-beam machining. These results demonstrate progress toward bridging the gap between the common practice of localization microscopy and process control in nanoelectronic manufacturing.

RESULTS

We apply critical-dimension atomic-force microscopy to traceably measure the distance between apertures that we fabricated by electron-beam lithography.[3] In an initial test,[5] we analyze the sidewall positions around the bottoms of a representative pair of apertures (Figure 1a). Either by fitting elliptical models to or by directly centroiding the sidewall positions, the distance between the apertures is within one nanometer of the nominal value of 5000 nm. Sampling multiple pairs of apertures in the two lateral dimensions yields a traceable mean distance or pitch between the apertures of 5000.71 nm ± 0.54 nm (Figure 1b). This uncertainty is a 68 % coverage interval, building confidence in the placement accuracy of electron-beam lithography for a representative array, and yielding a master standard. Propagation of scale uncertainty and localization error yields a traceable and total uncertainty of less than one nanometer across an imaging field of more than 150 μm^2, which both sets a record and motivates improvement.

With this master standard in hand, we can calibrate our optical microscope[3-5,8,9] and apply the considerable area of its imaging field to traceably measure aperture placement with high throughput (Figure 2). This new measurement capability allows rapid tests of the machining of aperture arrays with a focused ion beam, eliminating the need for lithographic pattern transfer and facilitating rapid prototyping. However, without the interferometric measurements and internal corrections of stage positions of our electron-beam lithography systems, our focused-ion-beam system places apertures into arrays with significant errors across the patterning field (Figure 2a-c). Systematic effects are evident from the position errors, depending on process parameters such as raster scanning or random scanning of the focused ion beam (Figure 2c-d), and motivating further study. The localization data present the future opportunity for an external correction of such errors, to achieve both accuracy and efficiency of the machining process.

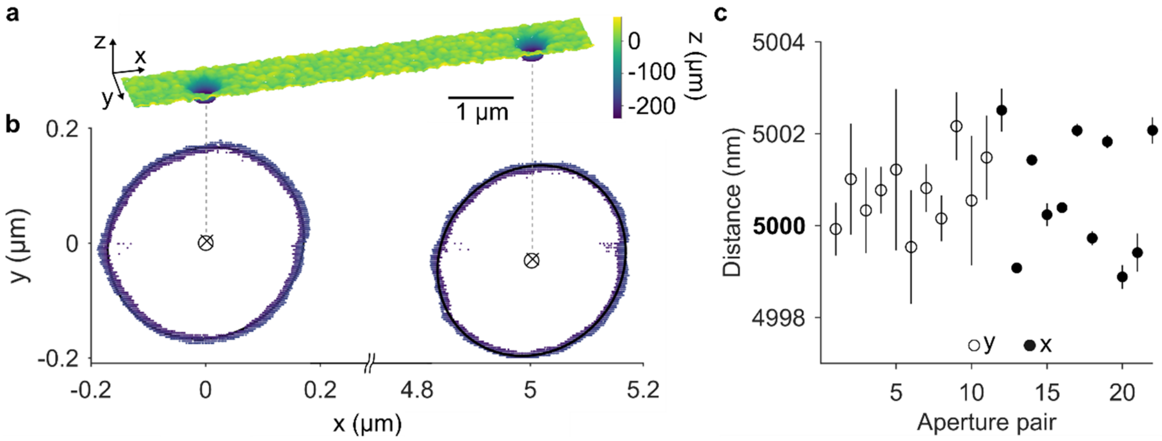

FIGURE 1. Validation of Aperture Array from Electron-Beam Lithography. (**a**) Critical-dimension atomic-force micrograph showing a three-dimensional image of a representative pair of apertures. (**b**) Plots showing two-dimensional reductions of the sidewall positions around the bottoms of the apertures. The color code is the same in (a) and (b). The central circles are the centroids that result from fitting elliptical models to the sidewall positions. The central crosses are the centroids that result from direct analysis of the sidewall positions. (**c**) Plot showing mean distances between multiple pairs of apertures along the y and x axes. Vertical bars are 68 % coverage intervals from replicate measurements. The nominal distance between apertures is 5000 nm.

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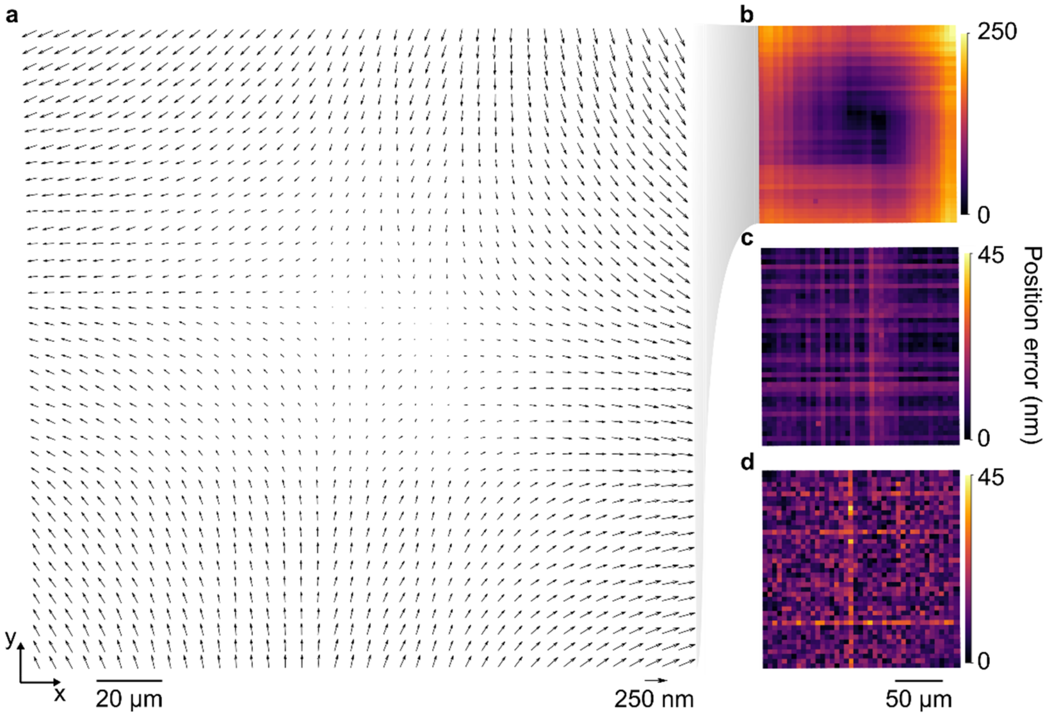

FIGURE 2. Test of Aperture Arrays from Focused-Ion-Beam Machining. (**a**) Vector plot showing representative position errors, with respect to an ideal array, for an aperture array resulting from a raster scan of the focused ion beam. The trend of the position errors indicates compression in y and expansion in x of the patterning field. (**b**) Plot showing magnitudes of position errors in (a). (**c**) Plot showing position errors of higher spatial frequency that remain after a partial correction by a Zernike polynomial model of position errors with lower spatial frequency in (a). (**d**) Plot showing representative position errors, with a spatial frequency that is comparable to that of (c), for a different aperture array resulting from a random scan of the focused ion beam.

CONCLUSION

In this abstract, we summarize our recent progress toward bridging the gap between the common practice of localization microscopy, in which localization precision is readily available, and process control in nanoelectronic manufacturing, in which localization accuracy is equally important. Our standards and calibrations enable the accurate localization of nanostructure placements, such as by electron-beam lithography and focused-ion-beam machining, demonstrating representative aspects of process control. Electron-beam lithography has applications to fabricating photomasks for nanoelectronic devices and reliable standards for localization microscopy. Focused-ion-beam machining has applications to repairing photomasks and editing circuits, and is in current use for the commercial production of aperture arrays with high efficiency but uncertain specification of reference positions, leading to the possibility of unreliable standards and erroneous calibrations. We identify this potential problem and propose a novel solution to it, leading the way toward better reliability and localization accuracy. We conclude by emphasizing the need to develop new standards for localization microscopy with lower uncertainty of scale in all three dimensions. This could enable a traceable and total localization uncertainty of less than one nanometer, throughout a focal volume approaching one million cubic micrometers, to make full use of the ultrahigh throughput of optical microscopy.

KEYWORDS

accuracy, localization, microscopy, optical, traceable

An Unconventional Tradespace of Focused-Ion-Beam Machining

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INTRODUCTION

Nanoelectronic manufacturing involves a broad variety of fabrication processes for making products of different value. At the state of the art, focused-ion-beam machining is commercially viable only for modifying select devices of high value, such as editing circuits[1,2] and repairing photomasks.[3,4] Beyond the nanoelectronic domain, however, this machining process has diverse applications, due to its ability to directly pattern complex nanostructures without serial lithography. In all of its applications, focused-ion-beam machining occurs within a fundamental tradespace of lateral resolution and volume throughput. A power-law dependence of lateral resolution on ion-beam current defines the conventional tradespace, such that fine features take much longer to mill than coarse features. This intrinsic constraint results in the conventional view of focused-ion-beam machining as slow and costly.

Previous studies[5,6] have used sacrificial films to mask the diffuse periphery of a focused ion beam, mitigating defects at the pattern edge and enabling a form of lateral super-resolution. However, it is unclear if a sacrificial mask presents any fundamental advantage for improving lateral resolution, in comparison to simply reducing ion-beam current. To answer this open question, we investigate the resolution–throughput tradespace of focused-ion-beam machining. We discover that a sacrificial mask enables patterning to occur with the lateral resolution of a low value of ion-beam current, and the volume throughput of a high value of ion-beam current. The throughput advantage could extend to two to three orders of magnitude, so that the principal benefit of the super-resolution effect is in the temporal domain, rather than the spatial domain. An advantage of this magnitude would be surprising, and the effect could be comparable to other nanofabrication processes that were disruptive to the conventional state of the art in their times, such as chemical amplification of resist materials,[7,8] and stepper systems for optical lithography.[9,10] To better understand this unconventional tradespace and surprising advantage, we summarize the first comprehensive and systematic study of this topic,[11] integrating four concepts for the most widely available type of electron–ion beam system with a gallium source.

RESULTS

Sacrificial Masking Film

First, we deposit a sacrificial film of chromia, Cr_2O_3, onto substrates of silica, SiO_2, and apply scanning electron microscopy, X-ray diffraction, and atomic force microscopy to characterize the mask. The measurement results show that the chromia mask dissipates charge under irradiation of an electron beam, is primarily amorphous, and has nanometer roughness, respectively (Figure 1a, i-ii).

In-Line Resolution Metrology

Second, we develop a novel method for in-line metrology of ion-beam resolution by scanning electron microscopy within an electron–ion beam system (Figure 1b, iii-iv). The method enables reproducible focus of the ion beam and provides an initial characterization of effective patterning resolution.

Complex Test-Structures

Third, we mill complex test-structures in silica through the chromia film with a beam of gallium cations and sacrifice the chromia by wet etching down to an interface with a new selectivity. We measure the resulting surface topography by atomic force microscopy after each fabrication step, extracting milling depths and edge widths from parametric models of surface profiles and propagating uncertainty through Monte-Carlo simulation (Figure 1c, v-vi).

Resolution–Throughput Tradespace

Fourth, we quantify vertical resolution of approximately 1 nm and lateral super-resolution factors that range from approximately two to six, which we also predict theoretically without adjustable parameters. We find an improvement of volume throughput for equivalent resolution that exceeds a factor of 40 with minimal extrapolation and in potential excess of a factor of 500 for our lowest value of ion-beam current (Figure 1d, vii-viii, Table 1).

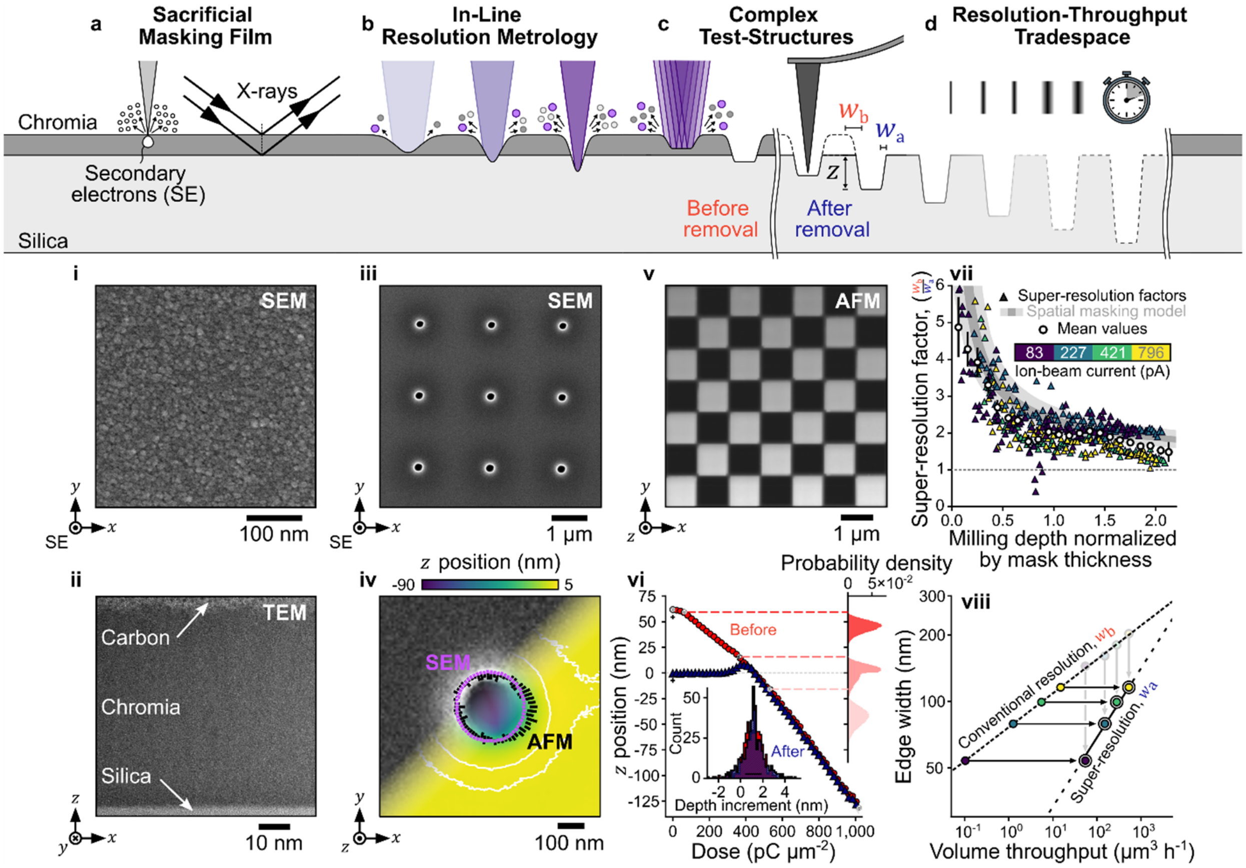

FIGURE 1. Experimental Overview and Key Results. (**a**) Sacrificial masking film. (**i**) Scanning electron micrograph (SEM) and (**ii**) transmission electron micrograph (TEM) showing the film. (**b**) In-line resolution metrology. (**iii**) Scanning electron micrograph and (**iv**) atomic force micrograph (AFM) showing structures to test lateral resolution. (**c**) Complex test-structures. (**v**) Atomic force micrograph showing structure to test vertical response and (**vi**) corresponding plot showing vertical response as a function of ion dose. (**d**) Resolution-throughput tradespace. (**vii**) Plot showing super-resolution factor, which we calculate as the ratio of edge width before and after removal of the mask, as a function of milling depth. (**viii**) Plot showing edge width as a function of volume throughput. Bars and crosses are 95 % coverage intervals. Uncertainties in (viii) are smaller than the data markers.

TABLE 1. Lateral Resolution and Volume Throughput

	Before Removal of Mask		**After Removal of Mask**		**Factor of Improvement**	
Ion-Beam Current (pA)	**Lateral Resolution (nm)**	**Volume Throughput (µm^3 h^{-1})**	**Lateral Resolution (nm)**	**Volume Throughput (µm^3 h^{-1})**	**Lateral Resolution (–)**	**Volume Throughput (–)**
83 ± 1	144.4 ± 0.2	54.5 ± 0.2	53.9 ± 0.4	0.10 ± 0.02	2.678 ± 0.016	528 ± 28
227 ± 1	160.7 ± 0.2	151.0 ± 0.2	79.2 ± 0.2	1.25 ± 0.04	2.029 ± 0.006	119 ± 4
421 ± 3	180.1 ± 0.2	280.7 ± 0.2	99.3 ± 0.6	5.52 ± 0.22	1.814 ±0.010	51 ± 3
796 ± 4	202.5 ± 0.2	529.8 ± 0.4	112.9 ± 0.2	12.72 ± 0.22	1.794 ± 0.004	42 ± 2

Uncertainties are 95 % coverage intervals. Insignificant figures are present to avoid significant rounding errors.

CONCLUSION

In this abstract, we summarize several advances to the state of the art of focused-ion-beam machining.[11] New theory enables engineering design of a sacrificial masking process, which was previously empirical, allowing its prediction and optimization for device fabrication. Theoretical predictions generally agree with experimental results, quantifying the extent to which a mask can improve the tradespace of lateral resolution and volume throughput. The improvement is so large as to be potentially analogous to the gain mechanism of chemical amplification of resist materials, in which effective thresholding improves contrast in photolithography, or increases in sensitivity improve areal throughput of electron-beam lithography.[8] These results suggest that sacrificial masking could enable not only ultrarapid prototyping of complex devices, which is relevant for research and development, but also commercial manufacturing of device arrays that would conventionally require hundreds to thousands of hours of machine time. This transformation is potentially similar to the deviation of stepper systems away from the limiting trend of a power law between lateral resolution and areal throughput for diverse lithography processes.[10] Future work might optimize this unconventional tradespace, not only in the domain of nanoelectronic manufacturing, but also for producing microscopy standards,[12] diffractive optics,[13] electromagnetic metasurfaces,[14] and nanofluidic molds.[15]

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KEYWORDS

focused-ion-beam machining, resolution, throughput, chromia, silica

023

X-ray CD: Powerful metrology solution for HAR memory structure

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Lam Research Corporation

INTRODUCTION

As memory chip manufacturers move to more advanced technology nodes, the features that need to be etched and filled are increasingly narrow and have higher aspect ratios. High aspect ratio (HAR) etch continues to be the most critical and difficult step in the entire flow. These HAR structures have micron level depths with angstrom-level requirements for precision, which makes it extremely challenging for metrology to provide robust, non-destructive, and accurate in-line process control solutions. To solve these problems, we investigated 3 different CD-SAXS world leading suppliers and demonstrated the powerful x-ray tool capability. X-rays can penetrate the structure and provide information such as tilt, CD vs depth, overlay shift, twisting and more with the demanded accuracy, for HAR samples which are few microns deep and even with multiple tiers. In this poster, we will provide introduction of x-ray CD solution with different tool sets. The correlation results look promising between different tools and with reference metrology.

Results and Discussion

The methods we used is transmission critical dimension small angle x-ray scattering (CD-SAXS). The incoming X-ray beam is incident on the sample and a 2D detector collects the intensity of the diffracted beam as a function of the diffraction angle (2θ). The spacing between diffraction peaks is a measure of the pitch of the structure. The angular dependence of intensity – as the sample is rotated around φ – gives a measure of the vertical features such as CD vs depth and is illustrated in Figure 1.

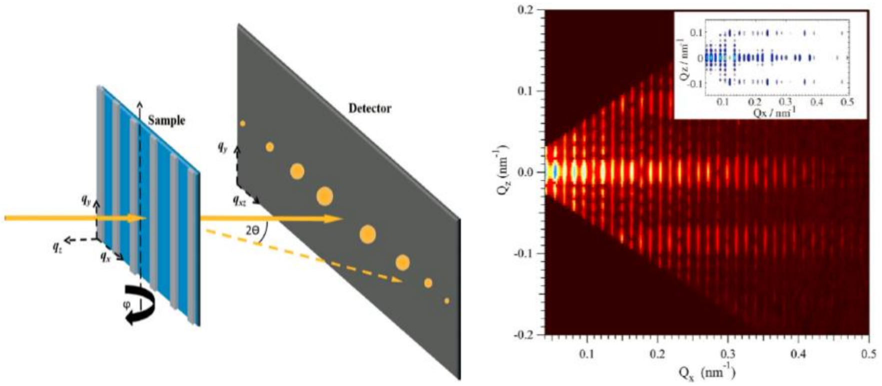

FIGURE 1. CD-SAXS method utilizes the variable-angle transmission scattering from a small beam size to provide detailed shape and dimensional data with sub-nm precision. It is non-destructive.

Samples tested include hard mask open (HMO) etch, 1-tier memory hole (MH) etch, 2-tier MH etch, and DRAM structures. In this poster, the results from Lam internal HAR samples are discussed. Figure 2 shows center line shift (CLS), and CD verse Depth on 1-Tier 3D NAND post memory hole measured on different CD-SAXS tools. The correlation is up to 0.99. CLS shows direction change at different depths. In this case, CD-SAXS is capable of measuring tilt of top and bottom tiers, joint displacement, litho-overlay with sub-nm precision.

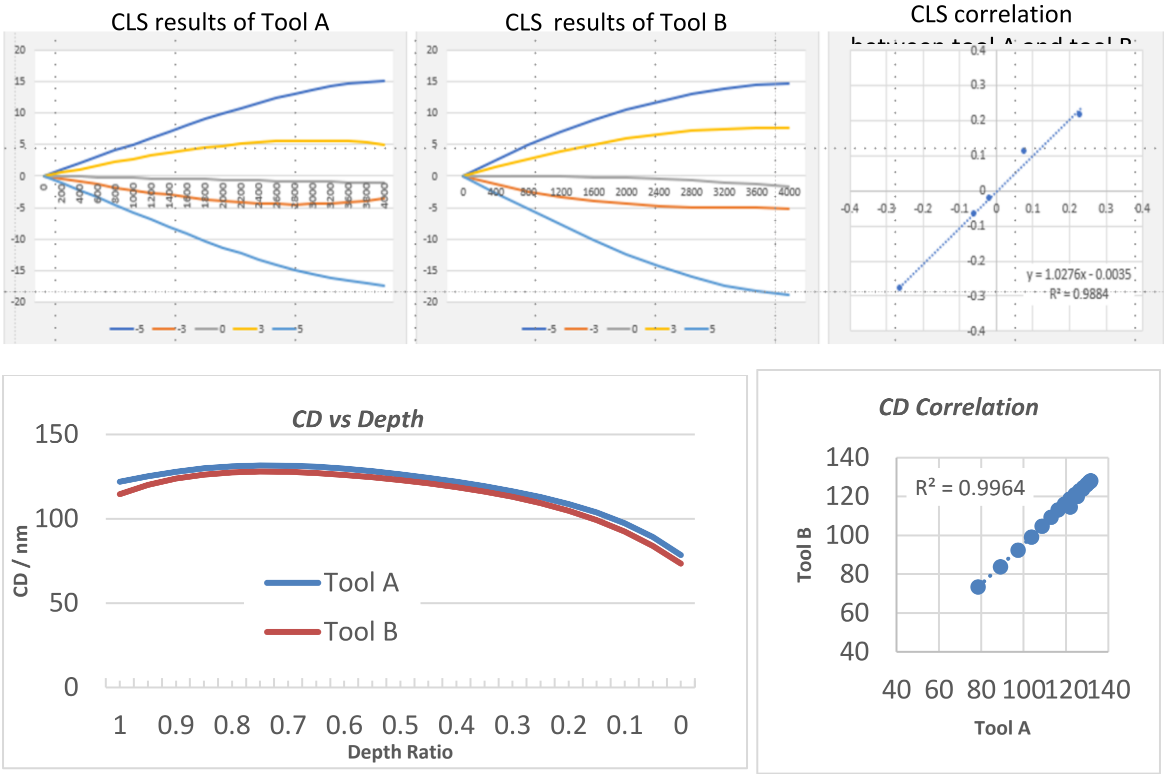

FIGURE 2. 1-Tier 3D NAND post memory hole global tilt and profile measurements using different tools. Tilt, center-line shift (CLS, and CD vs. depth is obtain with excellent correlation to xSEM).

XCD as non-destructive method offers sub nanometer precision in 3D-NAND Memory hole profile, CLS and global tilt measurement. In the next few years, we expect to see significate improvement in both performance and throughput. We will keep investigating this method on more and more challenging applications.

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KEYWORDS

CD-SAXS, High aspect ratio memory hole

Slicing Through Thin Samples at Atomic Resolution

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INTRODUCTION

Since the discovery that semiconductor device performance can be improved by extending the Si channel in 3D, the demand for metrology and defect studies in 3D has increased steadily. The standard and still valid approach is 3D volume reconstruction via tomography. However, the spatial resolution in the reconstructed volume is usually around 1nm. Lately, there is a growing need for sub-nm resolution to aid metrology of layers of 1nm thickness. In addition, while traditionally tomography reconstruction concerned 150-300nm thick samples, advanced devices require 3D information from 30-50nm thick samples. The most popular use-cases concern the elucidation of the (atomic scale) roughness of interfaces and the metrology of layers hidden between other materials. Therefore, we need to look for solutions that can provide 3D information from thin samples at, preferably, atomic resolution.

RESULTS AND DISCUSSION

Following the discovery that the primary information recorded by Integrated Differential Phase Contrast (iDPC) concerns mainly the volume defined by the focus depth of the Scanning Transmission Electron Microscopy (STEM) probe[1], automated collection of through focus iDPC has been introduced as a means to collect a series of images from a sample, each of them representing mainly a slice sub-volume of the material defined by the defocus value in terms of the depth from the surface of the sample and by the depth of focus depth in terms of the slice thickness. With the introduction of the SCORR probe corrector, full probe correction (up to A5 aberration) at 35-40mrad convergence is possible, leading to very small depth of focus. At such conditions, each iDPC image has sub-Angstrom resolution in the x-y plane for accurate metrology, representing the projection of a few nm in z direction.

Elucidation of Hidden Layers

One example of the usefulness of through focus iDPC, is the elucidation of the Si-channel and the gate dielectric layer in gate-view cuts even though some over-hanging gate metal layers are still left during Focus Ion Beam (FIB) lamella preparation. High Angle Angular Dark Field (HAADF) STEM and bright field Transmission Electron Microscopy (TEM) images are overwhelmed by the signal from the metal layer at the top of the sample, offering thus very little or no information from the Si channel or the gate dielectric underneath it. Figure 1 demonstrates an example of elucidating hidden layers. An overview of the area of interest is shown on the left-hand side. The HAADF image clearly shows the remnant gate metal obscuring the channel region (annotated using a red rectangle). On the right-hand side, two high magnification images of the channel region show the same area imaged using HAADF STEM (top) and iDPC (bottom). The Si lattice in the iDPC image is s clear that one can determine the smoothness of the top of the Si fin with atomic resolution.

The next step in exploring the potential of through focus iDPC was to examine a more complicated structure: a finFET device where the gate and a S/D contact were included in the same lamella. Figure 2 shows 2 distinct images taken with 32nm defocus difference. Small 3D models have been added at the bottom left corner of each image to

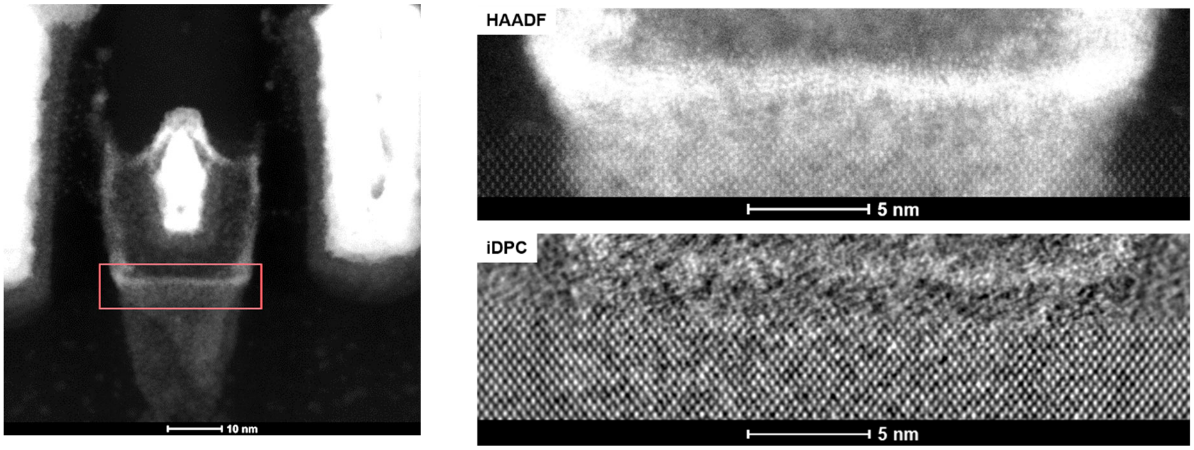

FIGURE 1. Left: HAADF STEM image overview of a gate view finFET sample. Some part of the metal gate still remains and obscures the channel/gate dielectric interface (highlighted using a red rectangle). Right Images of the Si fin top – gate dielectric – gate region using traditional HAADF STEM (top) and iDPC (bottom)

indicate where we expect the beam to have been focused on each frame. In the left-hand side frame, the beam is focused on the top of the sample. The Si fin (centre), a defect area on the fin, the metal gate (right) and the Source Trench Isolation (STI, bottom right) are clearly seen. The shadow of the SiGe epi is also clearly seen but its presence in the background does not deteriorate the quality of the image of the materials on the top of the sample. The defect on the Si fin disappears after about 8nm of additional under focus (image not shown here). After about 32nm of defocus, the iDPC reveal the SiGe S/D epi surrounding the Si fin with both the fin and the SiGe imaged at atomic resolution even though the image defocus is 32nm. Some interesting details are revealed about the sample at this depth: 1) SiGe dislocations starting from a void in the SiGe are clearly imaged and 2) a void is imaged within the SiGe epi. If one follows all the intermediate images, the variation in the void cross section with defocus demonstrates a void that is much larger at the SiGe/gate interface and is getting smaller as we probe deeper in the material. The Hf

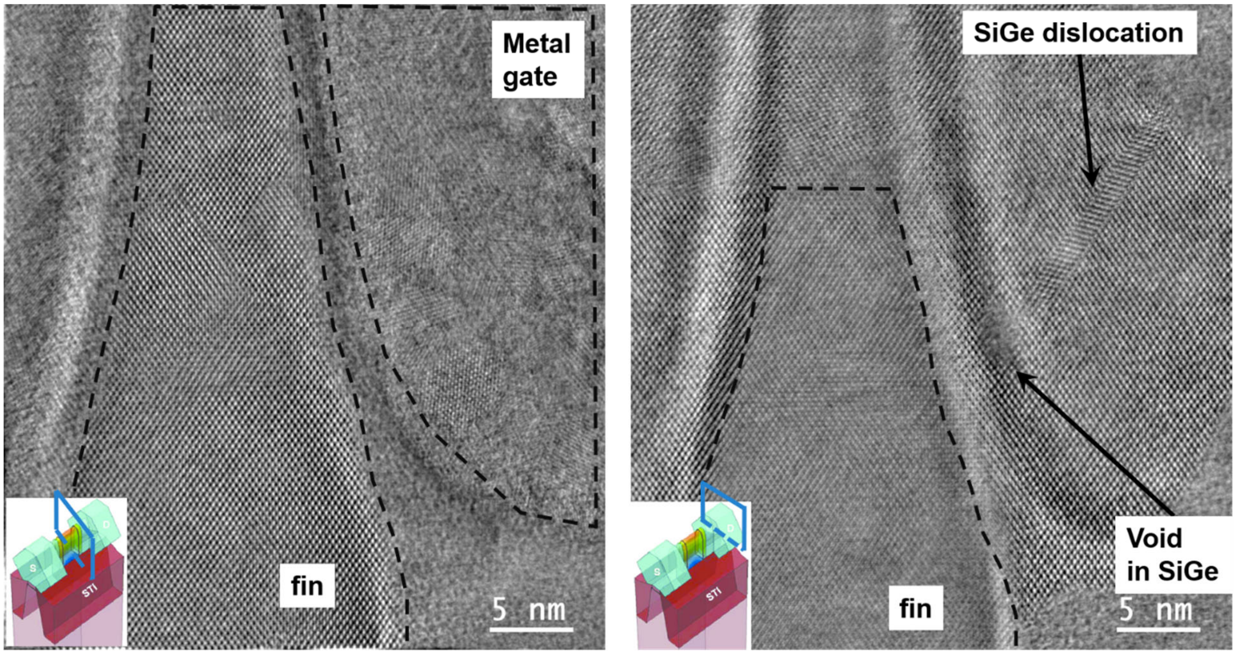

FIGURE 2. Left: iDPC image from the top of the sample showing the Si fin and the metal gate very clearly. The shadow of the SiGe epi can also be see but does not deteriorate the clarity of the metal gate; Right: iDPC image at 32nm focus difference (under focus) to the left image, showing clearly the SiGe epi, a dislocation in the SiGe epi and a void within the SiGe.

oxide gate dielectric is situated above the SiGe epi and in those areas low frequency contrast creates a bright and a dark shadow in the right-hand side image. The origin of this contrast variation is not fully understood yet but it fortunately does not affect our ability to image the underlying SiGe epi at atomic resolution.

CONCLUSIONS

Through focus iDPC has been presented here as an alternative method to electron tomography for studying the 3D structure of TEM samples. Even though full volume reconstruction has not been included, this method reveals cross sections of the samples at different depth with sub-angstrom resolution which key for accurate metrology. In this paper we have shown how this method can be used to image interfaces below other materials and that successive cross sections can be imaged without the under- or over-laying layers inhibiting imaging. Due to the excellent resolution on each slice, we have managed to accurately depict a void in SiGe epi located, in the sample, underneath the metal gate. Finally, it is worth mentioning that all images reported here were recorded with a beam current of 30pA and dwell time below 5μs. This means that the overall dose to the sample was kept at a minimum.

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KEYWORDS

3D visualization, depth sectioning, iDPC, metrology

Defect Inspection in Semiconductor Image Using Histogram Fitting and Neural Networks

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INTRODUCTION

We first present a method for detecting defects in an image with a homogeneous background. From the observation that the intensity histogram of such an image has log-normal distribution, we fit a Gaussian function to the log histogram twice. First, we perform a first fit over the entire domain to find the interval of background intensity. In the background interval, a second fit is performed to find the shape of the distribution function when the image has no defects. An outlier that does not decrease like the tail of a Gaussian function is judged to be defects. We also present two ways for converting an image with structure to an image with a homogeneous background. The first way to remove structure is possible when computer aided design (CAD) data is available. An image with a homogeneous background can be obtained using the signed distance function (SDF) generated from a binary CAD. If CAD data is not available, we present a second way to check if the image has a linear or complex structure and to remove the linear structure from the image. Neural networks are used to find defects in an image of complex structure.

PROPOSED METHODS

We first propose a method for detecting defects in an image with a homogeneous background. It is much more useful to have design information such as CAD data when performing defect inspection. Therefore, we divide the situation into two cases: with CAD data and without CAD data.

Double-fit Method

This section describes a statistical technique for finding defects in an image with the range [0, 1] with a homogeneous background. Let $H(x)$ be the smoothed log scaled histogram of intensity of such an image. We observed that $H(x)$ looks like a Gaussian function. Therefore, we fit a Gaussian function to $H(x)$ twice to find the shape of the log scaled histogram of an image background. The first fit is done by minimizing the following weighted L^2 norm on the interval [0, 1] to find the background intensity:

$$\min_{\xi,\mu,\sigma} \int_0^1 \left(H(x) - \xi e^{-\frac{(x-\mu)^2}{2\sigma^2}} \right)^2 e^{-\frac{(x-\mu_0)^2}{2\sigma_0^2}} \, dx \,,$$

where $\mu_0 = \operatorname*{argmax}_x H(x)$ and σ_0^2 is the variance of $H(x)$. Let (ξ^*, μ^*, σ^*) be the solution of the first fit. To fit the background part more accurately with a Gaussian function, we perform a second fit with the first result:

$$\min_{\xi,\mu,\sigma} \int_{\mu^*-\sigma^*}^{\mu^*+\sigma^*} \left(H(x) - \xi e^{-\frac{(x-\mu)^2}{2\sigma^2}} \right)^2 e^{-\frac{(x-\mu^*)^2}{2(\sigma^*)^2}} \, dx \,.$$

Let $(\xi^{**}, \mu^{**}, \sigma^{**})$ be the solution of the second fit. We now introduce an r inflated Gaussian function $Z(x) = r\xi^{**}e^{-\frac{(x-\mu^{**})^2}{2(r\sigma^{**})^2}}$ to determine the defect region. If a pixel value x satisfies that $|x - \mu^{**}| > \max(\sigma^{**}, 0.2)$ and $H(x) > Z(x)$, then x is considered a defect.

Case with CAD data: SDF Method

Let C be the binary CAD data well aligned with the image to be inspected. From the CAD data C, the SDF ϕ can be obtained as

$$\phi(x) = \begin{cases} -d(x, \partial\Omega), & if\ x \in \Omega, \\ d(x, \partial\Omega), & if\ x \notin \Omega, \end{cases}$$

where Ω is the region with a value 1 in C and $d(x, \partial\Omega)$ is the distance from x to $\partial\Omega$. In order to remove the structure in the background of the image, we consider the level curves of SDF ϕ. An image with a homogeneous background is obtained by zeroing the average along the level curve of $\boldsymbol{\phi}$. Then we apply the double-fit method to detect defects.

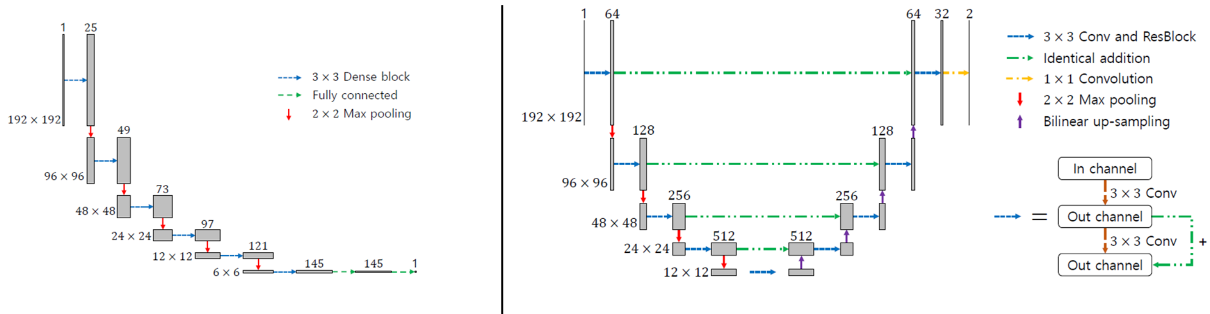
Case without CAD data: Hybrid Method

When the CAD data is not available, we first determine whether an image has a linear or complex structure. For the linear structure case, we remove the linear structure by subtracting the median value of the average intensity and those at both ends on the line with the dominant angle. Then apply the double-fit method to detect defects. For the complex structure case, we crop the image into five pieces and then find defects by using the binary classification neural network and segmentation neural network.

To determine whether an image has a linear or complex structure, we find the dominant angle θ^* from the edges in the image. We obtain an image u_{θ^*} on the rectangular domain by rotating the image u by $-\theta^*$ and filling the blanks generated by the rotation with the intensities at the ends of the horizontal line. The first right singular vector of an image with a horizontal linear structure is parallel to the all-ones vector $\mathbf{1}$. If the angle between the first right singular vector of u_{θ^*} and the all-ones vector $\mathbf{1}$ is less than 4°, the image is considered to have a linear structure. We call it RSV method.

If the image is determined to have a complex structure, we crop it into five pieces and pass each through the classification network. For the piece judged to have defects in the classification network, the RSV method is applied again since the piece of the image can have a linear structure. The piece determined to have a complex structure passes through the segmentation network to find defects.

Figure 1 shows the architecture of two networks. The classification network takes a grayscale image as input and returns the probability that the input image is defective. Binary cross entropy loss is used. The network architecture is based on the DenseNet [2]. The segmentation network takes a defective image as input and returns defective regions. The per-pixel weighted cross entropy loss is used to train the network. The network architecture is based on the U-Net with ResBlock [1]. Adam is used to minimize the loss function with parameters $\beta_1 = 0.9$, $\beta_2 = 0.999$, $\epsilon = 10^{-8}$ and learning rate 0.001.



Classification network architecture

Segmentation network architecture

FIGURE 1. The architecture of two networks.

Experimental Results

Since there is no testing database for semiconductor defects, we used the image in the literature. In the double-fit method, inflation ratio $r = 1.25$ was used for the threshold. If there are more than five defects, we judge that the double-fit method over-detects the defects. In this case, an increased inflation ratio $r = 1.4$ was used for the threshold to reduce the number of detected defects.

Figure 2 shows the defect inspection results. We show the input image, ground truth, results of our SDF method, and results of our hybrid method. In the RSV method, the angle between the first right singular vector and all-ones vector **1** says that the left five images have a linear structure and right five images have a complex structure. The IoU score is computed as

$$\mathrm{IoU}(A, B) = \frac{|A \cap B| + \epsilon}{|A \cup B| + \epsilon}.$$

Here, $\epsilon = 10^{-6}$ in both numerator and denominator prevents division by zero and ensures $\mathrm{IoU}(\varphi, \varphi) = 1$ for the empty set φ.

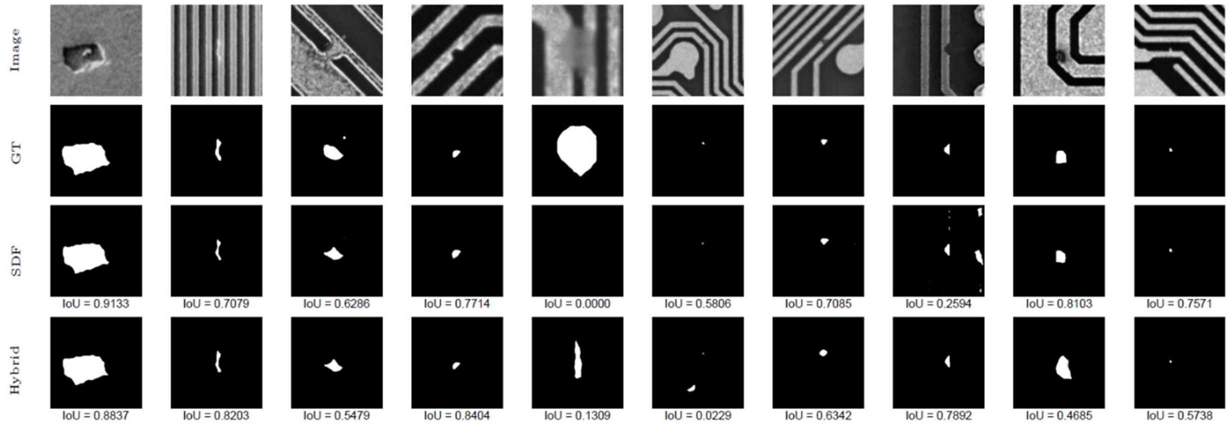


FIGURE 2. In the RSV method, left five images have a linear structure and right five images have a complex structure.

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KEYWORDS

Defect inspection, double-fit method, right singular vector, neural networks

Modeling and Model Validation for Electron Beam Nanometrology

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INTRODUCTION

Manufacturing of nanometer-scale devices often demands highly accurate dimensional measurements. The most recent *International Roadmap for Devices and Systems*[1] calls for metrology tool uncertainty in 2022 of less than 0.33 nm for widths of isolated printed lines. Instrumental effects in metrology tools are significant at this size scale. For example, in the scanning electron microscope (SEM), this is smaller than the beam size and much smaller than the beam spread within the sample. Schematically, we may think of the measurement as the production of a signal (e.g., intensity vs. position in an image): $\text{signal} = f(\text{instrument, sample})$. The signal is a function, f, of the instrument and the sample. If we knew f and the instrument and sample parameters, we would be able to calculate the signal that the instrument would produce. Alternatively, if some sample parameters such as a desired feature dimension are unknown, the measurement attempts to infer these by finding parameter values that make the calculated signal match the measured one. Errors in fixed input parameters or in the model function propagate to cause errors in the inferred measurement values. In this presentation, we describe the simulator that we use to interpret SEM measurements, uncertainties in the physics employed in its models, and a model-validation project that we are starting at the National Institute of Standards and Technology (NIST).

THE SIMULATOR AND MODELS

In the SEM, the interaction physics is complex enough that it is usually described by a simulator rather than a simple analytic function. A Monte Carlo simulator, JMONSEL, has been used at NIST to analyze SEM images of FinFET (Fin Field Effect Transistor) fins to infer their widths and shapes.[2] The operation of such a simulator is

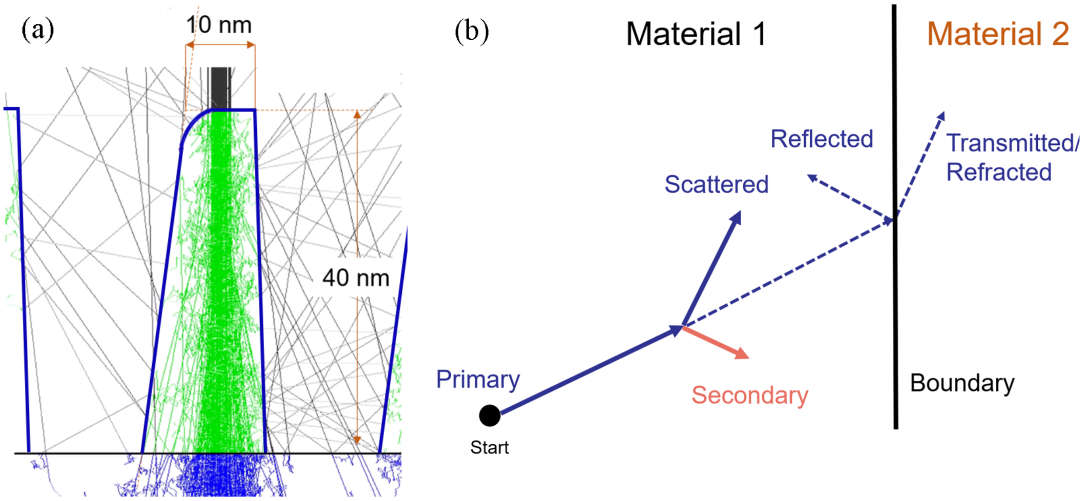

FIGURE 1. (a) Simulated trajectories (green: within a fin; black: vacuum; blue: substrate) of 15 keV electrons in a FinFET fin/space pattern. (b) One of the steps that compose the trajectories in (a). The steps terminate with a scattering event or boundary crossing, whichever is first.

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illustrated in Fig. 1. Electrons produced in a simulated electron gun are each tracked through a series of trajectory steps (Fig. 1a) until a stopping condition is met. The signal is estimated from electrons counted by a simulated detector. The trajectories in Fig. 1a comprise individual steps like those in Fig. 1b. The electron's initial motion, characterized by an energy and direction, continues until interrupted by a scattering event or boundary crossing. The frequency, location, and outcome of these events are drawn from probability distributions specified by the model physics. The kinds of events simulated in JMONSEL include elastic scattering from atoms, inelastic scattering with secondary electron generation, scattering from optical phonons, trapping, boundary scattering, and detection.

MODEL UNCERTAINTIES

JMONSEL models elastic scattering for incident energies up to 300 keV with relativistic Mott differential cross sections computed by ELSEPA,[3] using either the muffin-tin or isolated atom potentials as in NIST's Standard Reference Database 64.[4] This may be the most widely accepted model. It is, however, a binary scattering model. At low energy there are expected to be errors associated with the transition between binary and phonon scattering. Secondary electron generation is modeled with the full Penn algorithm.[5] It uses a Lindhard[6] free electron gas dielectric function. Nguyen-Truong compares inelastic mean free paths from about a dozen models, his own and the full Penn algorithm among them.[7] Results agree above a few hundred electron-volts, but they differ by factors of two or more at energies below 50 eV. Most authors treat boundary scattering with either a classical (width >> electron wavelength) or sharp (width = 0) quantum mechanical barrier model. JMONSEL permits intermediate barrier widths, but for most materials the correct value is not known. The extremes differ by about 10 % in simulated secondary electron yield for normally incident electrons, but the difference increases near grazing incidence.

These model differences are large mainly below about 100 eV, but this means they may be important for secondary electrons. These have energy $E < 50\ \text{eV}$, and their varying yield is responsible for contrast in the SEM. Ideally, we would compare the modeled yield to good measured values to determine which models are more realistic. Unfortunately, there is large scatter in measured yields from different laboratories (Fig. 2).

MODEL VALIDATION APPROACH

Secondary electrons are operationally defined as those with $E < 50\ \text{eV}$. Because of their low energies, their escape depths are of the order of 1 nm. Consequently, their yield is sensitive to the presence of thin contaminant layers, surface roughness, or other variations in the surface state. Since many of the yields measured for Fig. 2 were not performed in ultra-high vacuum (UHV), much of the lab-to-lab variation could be due to differences in surface cleanliness. Even the measurements performed under UHV conditions often had limited surface cleaning, for example sputter-cleaning but no annealing of sputter damage. The existing data are primarily yield vs. energy. There is very little available yield vs. incident angle (topographic yield) data at the low energies typically used for surface

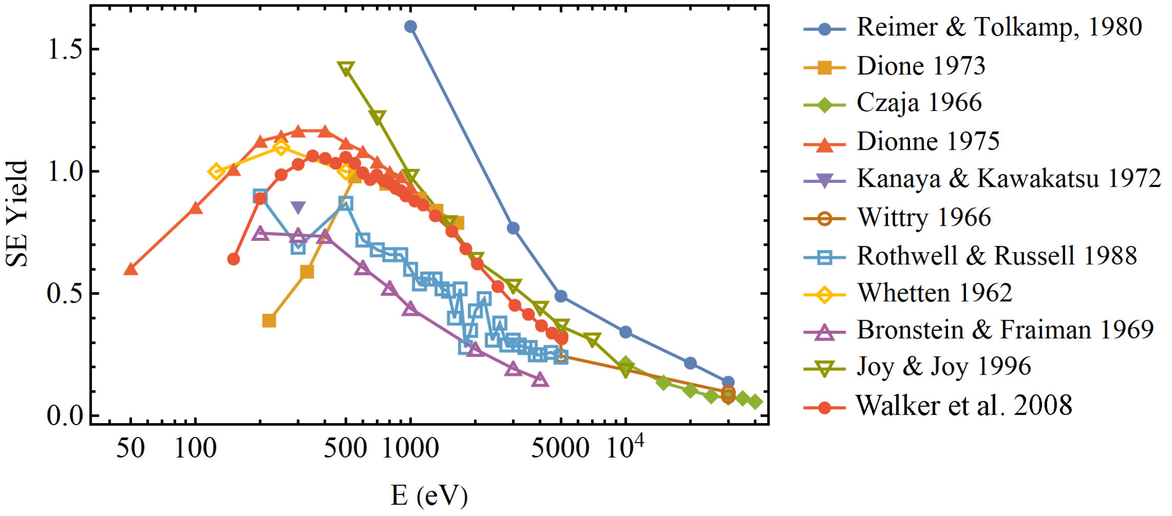

FIGURE 2. Secondary electron yields on Si vs. the energy of normally incident electrons, plotted using values tabulated in Joy's database[8] (from which the references are available in more detail) except for the Walker et al. result published subsequently.[9]

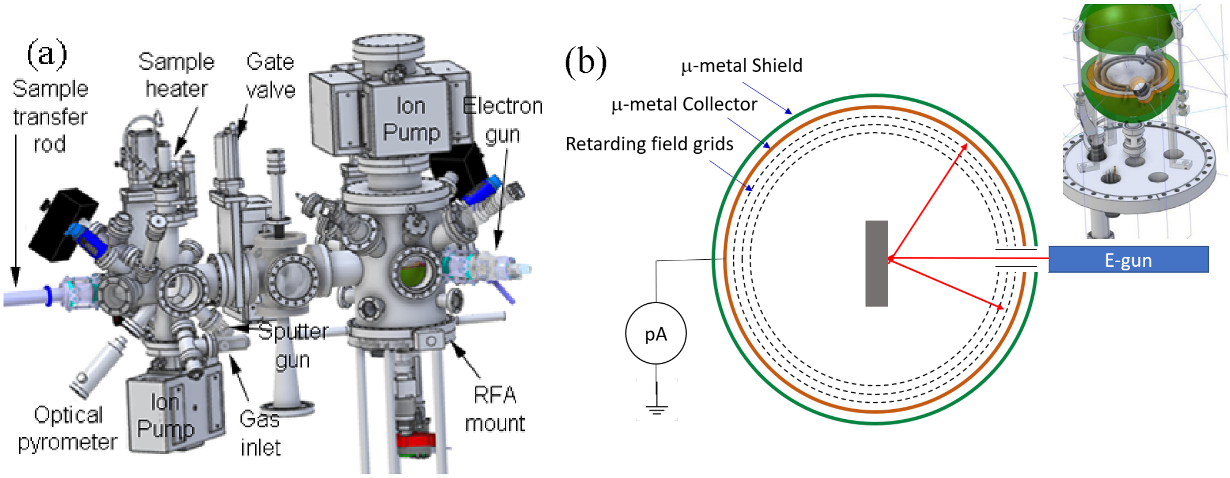

FIGURE 3. (a) Ultrahigh vacuum system with sample preparation and measurement chambers left and right of the central gate valve. Pumps include two high-compression turbo pumps on the far side (not shown). (b) Schematic cross section and 3D rendering of the spherical retarding field analyzer in the measurement chamber.

dimensional metrology. Topographic yield variation often produces much of the observed contrast in SEM images. We are beginning assembly of a yield measurement apparatus (Fig. 3) to fill these gaps.

The sample preparation section of the UHV chamber (Fig. 3a) will be equipped with a sputter ion gun, a leak valve to admit reactive gas for cleaning of carbonaceous contaminants, and a sample heater to produce temperatures suitable for annealing samples or for reactive cleaning. The measurement section will have a facility for Auger electron spectroscopy to provide feedback by measuring surface contamination. Cleaned and annealed samples will be placed into the spherical retarding field analyzer (RFA) shown in Fig. 3b (cross-sectional schematic and 3-D inset). The sample will rotate to change the incidence angle from normal to near-grazing. The RFA is designed to make the detection efficiency as invariant as possible under these changes in sample orientation. Currents will be independently measured from the collector, grids, and sample. The ratio of scattered to total current (i.e., beam current) is the yield. Grids or the sample may be biased to form a high-pass filter, the pass energy of which may be swept. With this instrument, yields and energy spectra will be measured as functions of incident energy and angle of incidence for comparison with model predictions.

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KEYWORDS

Scanning electron microscopy (SEM); electron interaction physics modeling; electron yield measurement; metrology

A Metrology Scanning Electron Microscope for Traceable Measurements

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INTRODUCTION

The increasing need for traceable nanometer-level metrology [1,2] has led to the development at the National Institute of Standards and Technology (NIST) of a specialized, metrology scanning electron microscope (M-SEM) having a metrology stage measured by a laser interferometer system. The purpose of the M-SEM is to carry out traceable calibrations of pitch and linewidth on standard reference samples using nanometer-level positioning of the sample under the electron beam in the SEM. The M-SEM will also be used for customer measurements on other reference materials such as those used in integrated circuit and nanotechnology development and production. This paper introduces the metrology, measurement and control system design, uncertainty budget, preliminary results, and the design of a planned reference artifact.

THE METROLOGY SEM

The M-SEM uses laser interferometers for sample displacement measurements traceable to the International System of Units (SI). The X-Y sample-stage position is measured while synchronously recording the secondary or backscattered electron output signal of the SEM. The M-SEM has a large sample capability (200 mm and 300 mm wafers and 6" photomasks) with 100 mm by 100 mm measurement coverage in the center. With variable landing energy and variable vacuum capability, the SEM can measure a large and diverse set of samples without conductive coatings. The field emission electron gun has better than 1 nm ultimate spatial resolution. The M-SEM is housed in a special laboratory incorporating an air-suspension vibration-isolation slab and a clean enclosure, thus achieving high-end SEM performance.

The 40 pm resolution homodyne interferometer system with phase sensitive photo detectors uses fiber-optic delivery of the laser light directly to the measurement axes. This results in a reduced optical path complexity, lower thermal drift, and a smaller footprint, enabling the interferometer optics to mount directly on the SEM sample chamber. High planarity mirrors are mounted on the SEM column and motion stage in both X-Y directions for differential measurement of sample position with respect to electron optical column, as shown in Figure 1. The interferometer system provides sub-nanometer non-linearity and will track velocities up to 1 m/s, with real-time compensation, and positional accuracy levels of $10^{-6}0^{-6}$.

A computerized measurement and control system was developed to operate at high data throughput. Fast scanning of the SEM minimizes the inter-frame drift due to environmental effects. The maximum data acquisition rate for the combined SEM column detector, the SEM horizontal and vertical raster scan signals and the X-Y laser stage position is 3 MHz. The SEM scan and detector data are collected using a data acquisition hardware while the stage position data are simultaneously acquired through a custom-programed field programmable gate array (field programmable gate array(FPGA)) board that interfaces to the interferometer hardware. Complete synchronization of the hardware (and thus data acquisition process) is achieved by generating a master clock signal within the FPGA which, in turn controls the analog SEM column data acquisition. The system accepts measurement scripts to programmatically move, image, and sample the SEM column data while executing control of the SEM through a custom programable keyboard emulator.

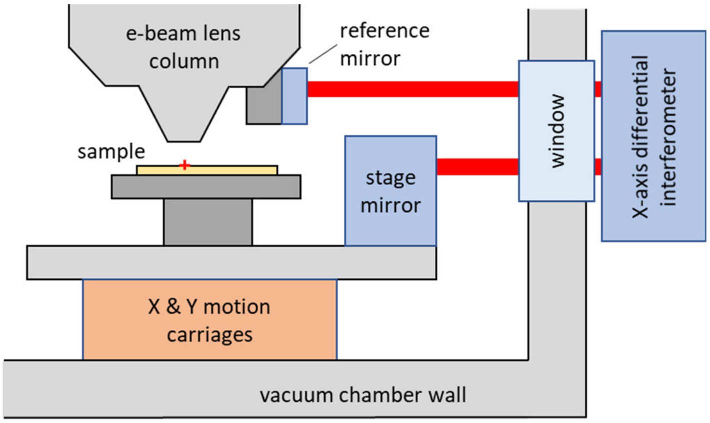

FIGURE 1. M-SEM block diagram showing laser interferometer beam path for the X-axis. The Y-axis components are not shown for clarity.

MEASUREMENTS

Two measurement methods are implemented: 1) Image magnification calibration, where a set of images at constant magnification are collected as a feature is moved systematically within the field of view by translating only the interferometrically-measured sample stage. The position of the feature within the SEM image field (pixel coordinates) is correlated with the interferometer-measured X-Y position of the sample in order to calibrate the field magnification scale or pixel size. 2) Spot mode metrology, where the primary electron beam is stationary and the sample is moved under the beam while recording secondary electron detector signal and X-Y position of measurement stage. The spot mode method is applicable to long distances, in principle up to the full 100 mm measurement range.

Preliminary spot-mode measurements have been made on grating artifacts with 500 nm, 700 nm, and 1 μm pitches by traversing their full 100 μm fields. A representative estimated uncertainty budget for average pitch measurements from these data is shown in Table 1. Individual uncertainty components are combined as root sum of the squares. The uncertainty arising from the measurement of the 100 μm distance is $[(5\times10^{-7} \times 100\ \mu\text{m})^2 + (1\ \text{nm})^2]^{1/2} = 1$ nm; a relative uncertainty of 1×10^{-5}. (All uncertainties are reported with a coverage factor k = 1.) However, the overall average pitch measurement uncertainty is overshadowed by the sample-related components totaling 30 nm, a relative uncertainty of 3×10^{-4}. The sample uncertainty for this preliminary measurement was dominated by the crude, unmeasured alignment of the sample with the measurement axis resulting in a large cosine error uncertainty.

TABLE 1. Uncertainty Budget for 100 μm scan average pitch measurement along the X-axis.

Source	Uncertainty			Notes
	(×L)	(nm)	Type	
Instrument				
Interferometer scale	$< 5 \times 10^{-7}$		B	laser frequency & alignment
Periodic nonlinearity		< 1	B	fringe interpolation error
Abbe error		< 0.1	B	1 mm Abbe offset; ± 0.1 μrad pitch and yaw (L < 100 μm)
Thermal drift		< 0.1	B	primary e-beam drift in 1 s measurement time (L = 100 μm)
Total	$< \mathbf{5 \times 10^{-7}}$	**< 1**		
Sample				
Grating alignment to measurement axis	$< 3 \times 10^{-4}$		B	cosθ; θ < 25 mrad
Line position determination uncertainty		3	A	includes both sample and measurement variability
Thermal expansion	6×10^{-6}		B	temperature = (20 ± 2) °C ; $\text{CTE}_{\text{Si}} = 3 \times 10^{-6}\ \text{K}^{-1}$
Total	$< \mathbf{3 \times 10^{-4}}$	**3**		

Shown in Figure 2 is the design of a NIST scale calibration artifact under development. It is part of a larger chip dedicated to integrated circuit dimensional metrology. Many chips have been created on 300 mm Si wafers using photolithography. A large number of critical dimension SEM measurements have been carried out already demonstrating high uniformity of dimensions die to die. This will facilitate batch certification by measuring a statistically representative sample with the M-SEM.

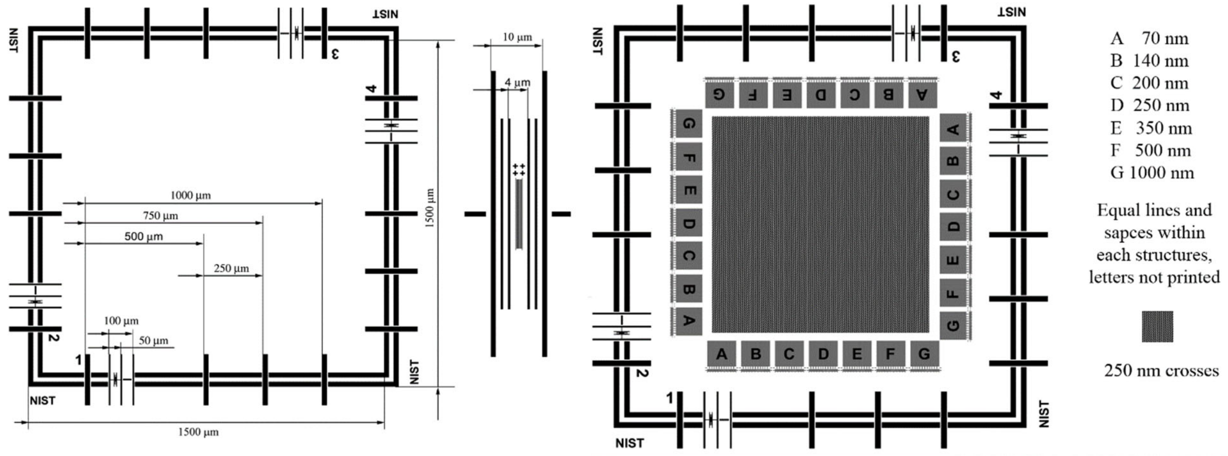

FIGURE 2. NIST Standard Reference Material under development for accurate, traceable scale calibrations for SEMs, atomic force microscopes and optical microscopes. With suitable computational methods, it is also useful for non-linearity and stray beam/sample tilt measurements. It has pitches ranging from 1.5 mm to 70 nm.

FUTURE WORK

The high repeatability and accuracy of the M-SEM facilitates faster development of new measurement methods especially useful for nanometer-scale measurements and the calibration of standard reference materials. The high-speed laser interferometer makes it possible to compensate for stage drift and vibration, potentially allowing accurate beam positioning within 1 nm. The fast digital imaging and real-time corrective composition of SEM images developed for the M-SEM have shown significant improvement over traditional fast or slow image acquisition.

SUMMARY

At present, the metrology SEM is used to scan line pitches for a traceable measurement. The final adjustments to the instrument and measurement methods are being carried out to verify measurement uncertainty values and prepare measurement scripts for calibration of customer samples.

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KEYWORDS

SEM, X-Y stage, laser interferometer, nanometer measurement, standard reference material (SRM)

Oxidation of Copper in the Presence of Graphene

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INTRODUCTION

Copper is a commonly used metal in the advanced semiconductor industry where its oxidation needs to be prevented to ensure low resistivity at nanometer-scale pitch interconnect levels in integrated circuits (IC).[1] Therefore, the development of an ultrathin barrier to protect Cu is important to the manufacture of ICs. Typical barrier materials that are used in the industry include Ta, TaN, SiN and SiCN, but as Cu interconnect dimensions decrease, diffuse surface scattering of electrons becomes dominant and Cu resistivity increases.[2,3] Graphene has been shown to be a promising barrier material to reduce surface scattering and thereby resistivity in Cu.[4, 5] Furthermore, numerous studies suggest single crystal continuous graphene can make Cu more resistant to thermal oxidation and wet corrosion.[6,7] However, single-crystal graphene synthesis is limited by high temperature growth conditions and slow kinetics, which prevents its implementation and scalability in ICs. On the other hand, scalable graphene deposited in a manufacturing environment is typically polycrystalline and defective in nature and hence its performance as an oxidation/corrosion barrier largely depends on the grain size and defectivity.[8, 9] The purpose of this study is to understand the oxidation behavior of Cu with polycrystalline graphene in ambient environment during thermal, water exposure, and laser-induced oxidation.

RESULTS AND DISCUSSION

We investigated the oxidation of polycrystalline Cu with mono- to bi-layer graphene deposited on top of it using a unique, selective, low temperature (<400°C) process. Thermal oxidation was performed in an ambient environment oven at 200°C. Water exposure oxidation was done at room temperature by allowing a droplet of water to dry on the surface of graphene-Cu. Finally, laser oxidation was induced by increasing laser power or number of scans during Raman measurements being performed in ambient environment at room temperature. Various metrology methods were employed to study the changes in graphene-Cu including, but not limited to, Raman spectroscopy, SEM, TEM, XPS, and reflectivity. It was discovered that these three oxidation methods led to different Cu oxide phases as measured by Raman (Table 1, Figure 1a) and visualized by planar SEM (Figure 1b-d). As expected, thermal oxidation of graphene-Cu led to predominantly Cu_2O phase present only at the grain boundaries of graphene (Table 1, Figure 1c).[8, 9,10, 11] Interestingly, room temperature laser-induced oxidation led to significant CuO phase formation (Table 1, Figure 1b), which is typically not accessed until high temperature (>200°C) thermal oxidation,[12] suggesting that there may be some catalytic effect imposed by the presence of graphene on Cu. Similarly, water droplet oxidation of Gr-Cu shows the presence of both Cu_2O and CuO, whereas water oxidation of bare Cu does not form significant CuO. Intercalation and dissociation of water under graphene has been reported in the literature,[13,14,15,16] which could explain the preferential oxidation of underlying Cu to the CuO phase in the presence of graphene and moisture. In addition, top-down SEM elucidates the presence of highly crystalline CuO nanostructures on the Gr-Cu laser-oxidized sample (Fig. 1b). Overall, this work shows that graphene in the presence of water can catalyze the growth of CuO on the surface of Cu and understanding this phenomenon is important for the implementation of graphene as a protective barrier for Cu. Increasing quality of graphene can help reduce this effect as the water intercalation likely occurs at defect sites such as grain boundaries and sp^3-bound carbon. In addition, this is the first study of laser oxidation of Gr-Cu at low laser power where we use the energy derived from the laser power to exacerbate the growth of CuO. Hence, limiting the exposure of Cu to moisture is of critical importance in preventing CuO_x growth in interconnect fabrication.

TABLE 1. Copper oxide phase and Raman signal. [11]
Key: VS = very strong, S = strong, M = medium, W = weak, VW = very weak Raman signal.

Film	Oxidation method	unknown 69 cm^{-1}	Cu 93 cm^{-1}	Cu_2O 107 cm^{-1}	Cu_2O 148 cm^{-1}	Cu_2O 215 cm^{-1}	CuO 285 -299 cm^{-1}	CuO 335 cm^{-1}	CuO 621-649 cm^{-1}
Cu	Thermal	-	M	M	S	S	VW	-	S
Cu	Water	-	S	-	W	M	-	VW	-
Cu	Laser	-	-	-	-	-	-	-	-
Gr-Cu	Thermal	-	-	W	W	W	-	-	-
Gr-Cu	Water	-	S	-	W	W	S	W	W
Gr-Cu	Laser	S	S	-	W	W	VS	S	S

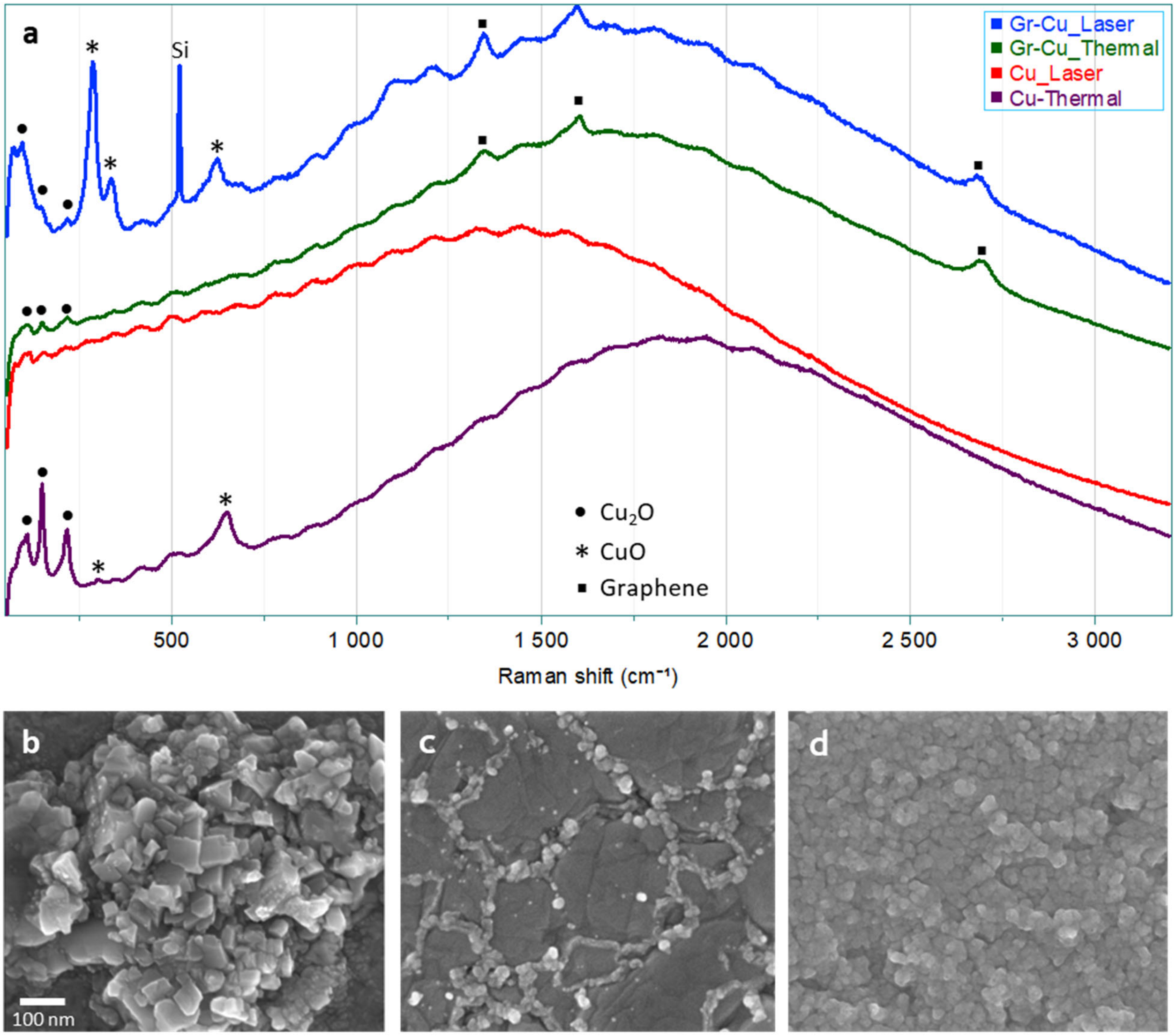

FIGURE 1. a) Representative Raman spectra of graphene on Cu (Gr-Cu) and reduced Cu oxidized by laser and thermal oxidation. Top-down scanning electron micrographs of b) laser-oxidized Gr-Cu showing large CuO crystals at the location of the laser beam; c) Cu_2O crystals protruding from Cu at the grain boundaries of graphene in thermally oxidized Gr-Cu; and d) reduced Cu after thermal oxidation showing a film of Cu oxide on its surface. All SEM images were collected by Lam Research.

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KEYWORDS

Graphene, copper, copper oxide, barrier, oxidation, intercalate, water dissociation, interconnect, integrated circuit

Studying Diamond Content In Microwave Nanocrystalline Diamond Film By XRD And Ellipsometer

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INTRODUCTION

Nanocrystalline diamond (NCD) film is widely used in carbon hard mask applications and as insulator layer in power devices. Smooth (small grain) NCD film with high hardness is highly desired and proper metrology method to optimize the film becomes critical.

As NCD grain size was made smaller, current metrology method with Raman spectroscopy was found to be lack of sensitivity [1, 2]. Just using the ellipsometer as a quick way to determine how close the film was to a diamond film could be wrong since the high refractive index (like that of diamond) could also come from high amorphous carbon content.

A comprehensive set of metrology techniques was developed with X-ray diffraction (XRD), ellipsometer and Atomic Force Microscope (AFM) for the NCD film diamond crystal phase, diamond content purity, and surface morphology characterization. As a result, the NCD film crystal phase, purity, and surface morphology could be identified unambiguously and quickly. The comprehensive metrology developed can be applied to characterization of other high value thin films as well.

APPROACH DESCRIPTION

The Microwave Plasma CVD Chamber (M-Chamber) NCD films were first investigated by XRD and ellipsometer measurement. To positively and effectively identify the diamond crystal phase of NCD films, grazing angle XRD was implemented with optimized measurement condition. Grazing angle XRD was used because stronger film intensity and less background noise from substrate.

Since the XRD peak intensity would only come from crystalline diamond and not amorphous carbon, XRD total intensity and ellipsometer measurement thickness were correlated to check NCD films diamond content purity: a linear correlation would clearly indicate the constant diamond content purity of the NCD films.

The surface morphology of different deposition condition M-Chamber NCD films were also investigated by AFM. AFM results were used to investigate different process condition effect on the film surface roughness.

EVALUATION OF THE RESULTS

Figure 1.a shows XRD spectra of commercial, Singapore lab and six different deposition condition M-Chamber NCD films at Applied Materials Santa Clara site. Diamond peak (111) and (220) were shown clearly. XRD total intensity, ellipsometer measurement thickness, XRD grain size of above two peaks were calculated and listed in Table1. Figure 1.b shows a good linear correlation between XRD total intensity and ellipsometer thickness, which means the measured NCD films are all very pure.

Different process condition played an important role in the final product of NCD films. Figure 2. shows different process condition effect on the film surface roughness. Rms data and grain size data of XRD were listed under each AFM images. Film surface tends to be smoother with smaller grain size of different process conditions.

In conclusion, robust comprehensive metrology techniques were developed and applied to high value M-Chamber NCD films. Such metrology solutions can be applied to characterize other high value thin films, which will be extremely important to help tune the process.

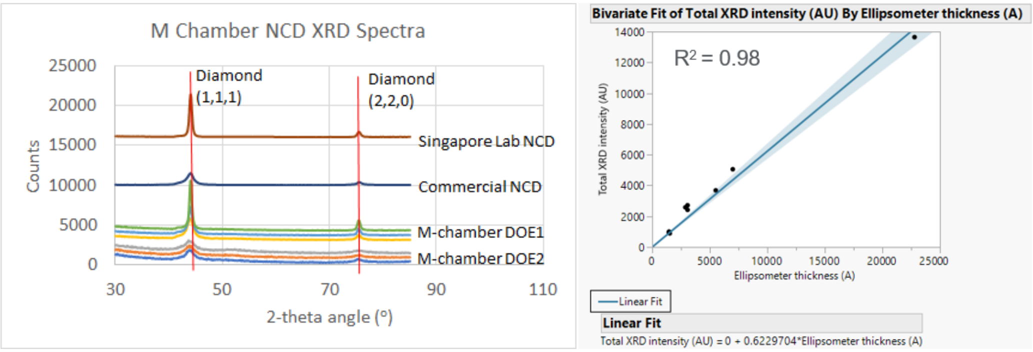

FIGURE 1- (a) XRD Spectra of M-Chamber NCD films. (b) XRD total int. vs. Ellipsometer thickness.

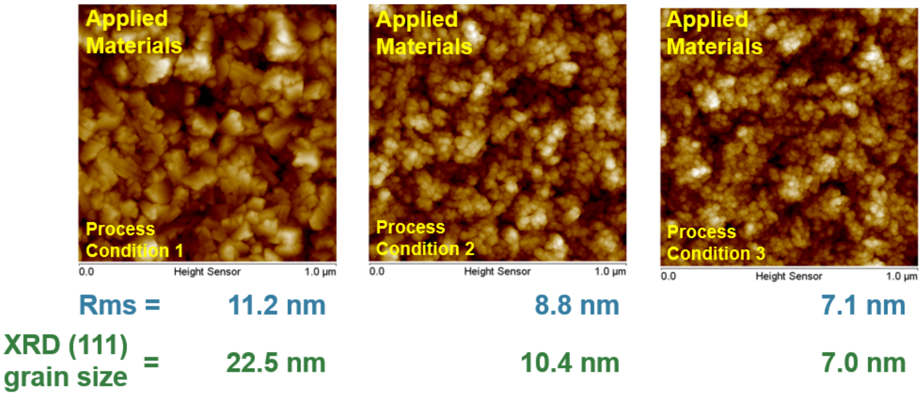

FIGURE 2- AFM study process condition effect on surface roughness & XRD (111) grain size correlation.

TABLE 1. XRD total intensity, ellipsometer thickness and XRD grain size

Sample ID	Ellipsometer Thickness (A)	Total XRD Intensity	Grain Size (A) (111)	Grain Size (A) (220)
NCD1-S14	3068	2716	225	226
NCD1-S15	3069	2418	104	216
NCD1-S16	2882	2582	70	121
NCD2-S15	1435	949	51	67
NCD2-S17	1525	892	46	44
NCD2-S23	1460	1003	39	31
SL-NCD	7000	5060	189	159
Comm. NCD	22797	13646	66	133
Comm. NCD 2	5521	3686	253	203

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KEYWORDS

Nanocrystalline Diamond (NCD), X-ray diffraction (XRD), Ellipsometer, Atomic Force Microscope (AFM)

Quantifying & Controlling 3D Device Processes With Mass Metrology

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INTRODUCTION

As traditional scaling is facing more complexity & challenges, there has been significant increase in semiconductor devices that are moving towards vertical integration/scaling. This trend presented significant challenges on process monitoring & control, where traditional metrology is limited by thickness/ complexity and/or the lack of visibility of these processes. Without such monitoring & control mechanism, process development and learning cycle will be significantly hampered. In effort to address such challenges, many semiconductor device manufacturers have utilized mass metrology. Mass metrology enables quantification of any wafer processes (etch, deposition, oxidation, clean, etc) and is agnostic to the visibility / complexity of the process and stacks. More importantly, as mass metrology does not require any modelling, it enables R&D customers to monitor, control & test their processes to reduce learning cycle time as well as optimizing their costs. In this paper, we will present applications/use-case of mass metrology on Gate All Around (GAA) processes to address challenges in the associated processes.

WAFER PROCESSING STEPS

In GAA architecture, nanowire formation are some of key wafer processing steps. As illustrated in Figure 1, some of these key steps involve deposition of complex stacks, blind-etch, recess where clear end-point is not available. Multiple layers of Si-SiGe poses significant challenge for precise quantification of total thickness deposited, which will affect subsequent Fin etch process. Similarly, SiGe Recess is expected to affect subsequent Spacer etchback process. As described in Results section, for these processes, delta-mass enables 3 key use-cases:

1. Outlier detection to identifying process excursion/deviation at high precision
2. Feedback process control to improve chamber control/matching
3. Feedforward process control to improve consistency of device structure

The following section will describe above mass metrology use-cases on the relevant GAA processing steps.

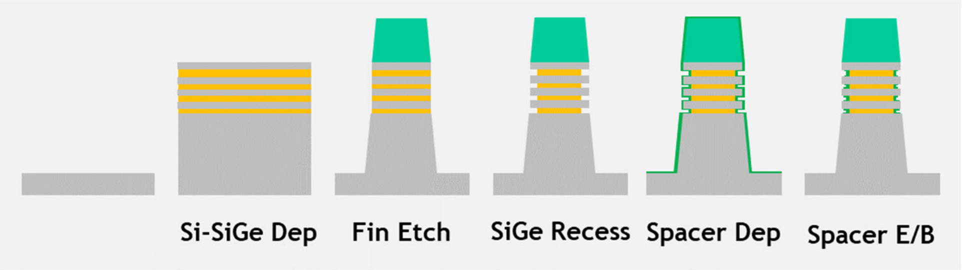

FIGURE 1. Illustration of GAA wafer processing steps quantified with mass metrology

Results Of Mass Metrology Measurement On GAA Processes

As incoming wafer variation has important influence on the downstream processes, one of the key initial steps measured with mass metrology is the Nanosheet stack deposition process. With reference to Figure 2, the range of variation in nanosheet stack deposition is ~1%. In turn, this variation subsequently influenced the Fin-etch process with clearly identified correlation between the deposition and etch process. Based on this correlation, one over-etch outlier is identified with likelihood of taller fins. With understanding of this correlation, a clear capability to feedforward deposition delta-mass to fin-etch should enable process control avoiding outlier / significant-deviation.

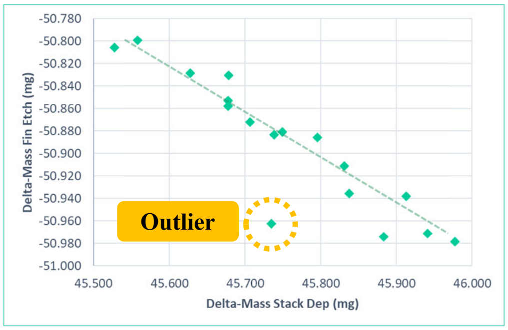

FIGURE 2. Clear correlation between delta-mass of stack deposition & fin etch enables outlier identification & potential of feedforward process control

Subsequent key process measured with mass metrology is SiGe recess. One of the critical control parameters in this process is the depth of recess where sufficient recess must be made to accommodate spacer deposition in later steps. However, due to the complexity of stack, challenges in processing and monitoring have been abound. Referencing Figure 3a, inline monitoring of SiGe recess was able to identify that one of the wafers had significant over-etch of SiGe by 600µg resulting in enlarged cavity. A further outlier was detected on wafer 12 during inner spacer etchback process, where incorrect recipe setting resulted in complete removal of inner spacer & further recess of SiGe. This over-etch profile is visible through comparison of Figure 3b (Wafer 13 – normal) and Figure 3c (Wafer 12 – overetch). Such inline monitoring capability will provide invaluable feedback for improved learning cycles in process development as well as swift-reaction to outlier occurrence in production environment. Finally, feedback control loop to improve chamber stability, performance and matching is one of the key advantages of enabling mass metrology on these obscure processes.

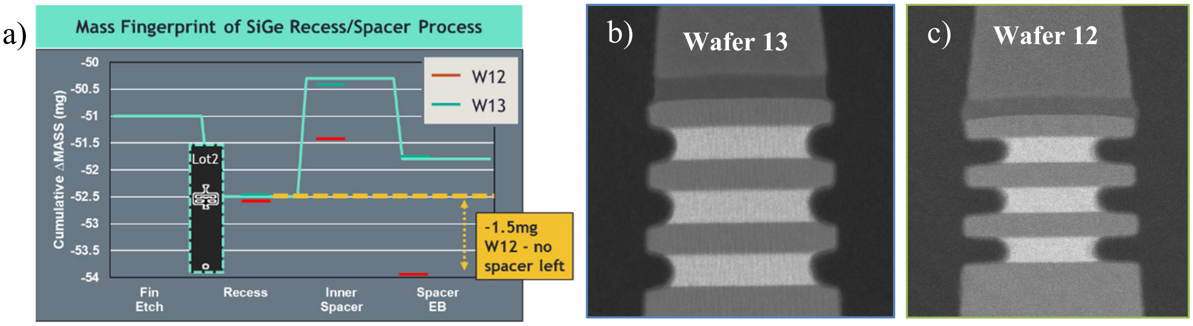

FIGURE 3. a) Tracking of cumulative delta-mass in GAA key processes (Fin-etc, SiGe recess, Inner Spacer Deposition and Etchback) with outlier identified in SiGe Recess and Inner spacer etchback, b) Cross-Section view of normal nanosheet (wafer 13), c) Cross-section view of over-etched nanosheet (wafer 12)

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KEYWORDS

Vertical scaling, GAA, 3D-Integration, Metrology

Operando Metrology for Real Time Monitoring of Complex Optical Stacks

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INTRODUCTION

We have used reflectometry to perform accurate real-time *operando* characterization of complex optical stacks grown at 400°C by Plasma Enhanced Chemical Vapour Deposition on 300 mm wafers. The dedicated *in situ* reflectometer, which operates in the UV-visible range, permits unambiguous identification of a few percent thickness deviation of individual layers in 16-layers stacks, too complex for accurate *ex situ* ellipsometry analysis. In addition, we demonstrate that the optical reflectance at room temperature, which is the target characteristic of such stacks, can be precisely determined by *operando* analysis fed with accurate optical index at room and process temperatures. These results pave the way for fast inline monitoring of optical materials and stacks by means of *operando* metrology.

OPERANDO METROLOGY

We used Applied Materials Producer PE-CVD equipment to grow thin materials for optical filters applications, and more precisely: silicon oxide, silicon nitride and amorphous silicon. Each chamber of the tool comes with two sides, which permit to process two wafers simultaneously. Each side is equipped with *operando* ISM metrology module that acquires reflectance data every 100 ms all along the deposition process. The ISM uses predetermined values of optical properties (at 400 °C) for the substrate and the deposited materials to model the reflectance data at each acquisition step and to evaluate the thickness of each layer throughout its deposition. This method is particularly appropriate for the monitoring of complex optical stacks because it measures layers one after the other therefore only fitting one unknown parameter at a time. To investigate ISM measurements accuracy, the calculated thicknesses have been compared to *ex situ* ellipsometry tools for single layer measurements and TEM analysis for stack depositions. In both cases, the ISM accuracy was better than ±1 nm. The ISM module was also used to detect systematic differences between the two chamber's sides (Figure 1). This metrology tool enables fast detection and efficient correction of process deviation even during the deposition of complex multi-layered stacks. It could further lead to automated process control.

Optical filters are designed to exhibit a specific reflectance profile. Being able to access room temperature reflectance spectrum of a processed stack during its deposition is then extremely useful to confirm the deposited product is conform to initial specifications. Because the ISM module operates at 400 °C, additional work is needed to extract room temperature reflectance from the measured data. Extensive temperature ellipsometry measurements have been performed on each deposited materials to characterize precisely their optical properties from room temperature up to 400 °C. Then optical simulations have been developed using ISM measured thicknesses and the previously determined room temperature optical properties to emulate room temperature reflectance spectrum of the deposited stack. We assessed the accuracy of those simulations by comparing them to *ex-situ* reflectance measurements carried out on a lab spectrophotometer (Figure 2). We found an excellent agreement between *in situ* and *ex situ* measurements (average error < 0.6%). However, uncertainty on material optical properties will affect the simulation. After a preliminary step of temperature ellipsometry on the deposited materials, the ISM module can therefore be used to access a stack room temperature reflectance profile.

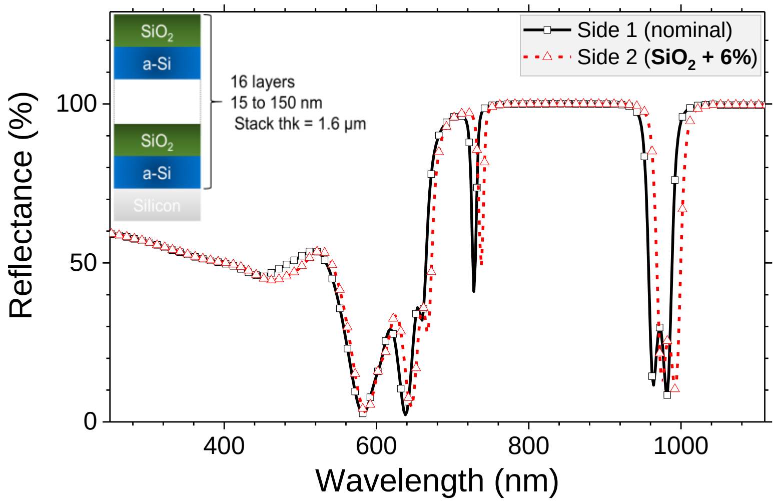

FIGURE 1. *Ex situ* spectro-reflectance measurement of complex optical stacks grown on the two sides of the process tool. The shift between the two data sets is due to a systematic 6% difference in the silicon oxide thicknesses as revealed by *operando* ISM analysis.

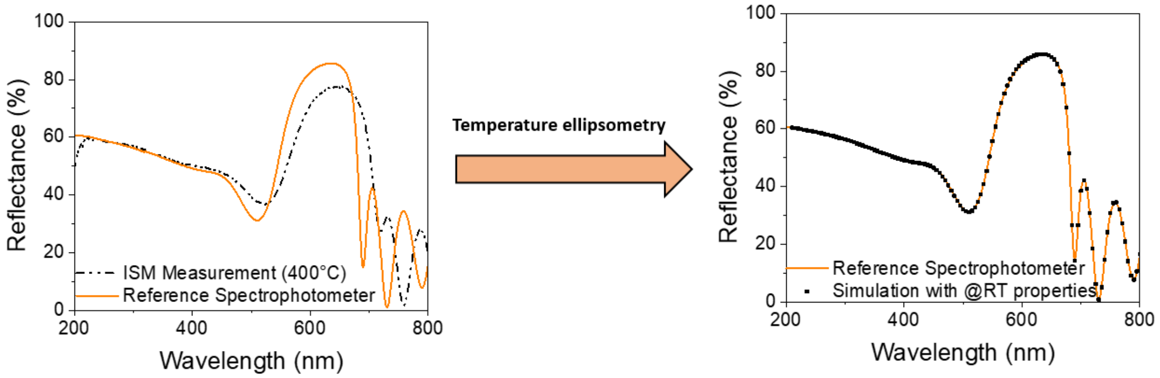

FIGURE 2. *Ex situ* spectro-reflectance measurement of complex optical stack compared with *operando* ISM measurement and simulation from ISM determined thickness. The method described here enables room temperature reflectance spectrum determination from *operando* metrology only.

These first results are encouraging regarding the ISM module ability to characterize complex stacks throughout their deposition process. However, work is still ongoing to extend the use of this module to depositions on more complex substrates and patterned wafers. The main difficulty regarding those structures is to model their optical behaviour accurately. Several theoretical models have been developed to emulate multi-layered structures using only complex reflectance[1, 2] and could be appropriate for *operando* metrology.

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KEYWORDS

In Situ, ellipsometry, reflectometry, PECVD deposition, thin-films, optical filters

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WITHDRAWN

WITHDRAWN

Liquid-metal-jet and High-resolution X-ray technology for nanoelectronics characterization and metrology

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INTRODUCTION

Recently the interest in x-ray source technology has been intensified since several critical semiconductor metrology methods such as optical based scatterometry is starting to run out of steam [1]. Furthermore, with introduction of advanced strain engineering and 3D structures in manufacturing new challenges for semiconductor metrology are emerging. Proposed solutions involve a variety of techniques including x-ray-based methods, however a main problem with most of those is the very low throughput since conventional X-ray tubes are very limited in x-ray output such as flux or brightness.

As illustrated in Fig 1a, a conventional X-ray tube generates X-rays when highly energetic electrons are stopped by a solid metal anode. The fundamental limit for the X-ray power generated from a given spot size is when the electron beam power is so high that it locally melts the anode. This damage or destroys the anode which replacement of anode or sometimes the whole x-ray source. The liquid-metal-jet anode (MetalJet) technology solves this thermal limit by replacing the traditional anode by a thin high-speed jet of liquid metal (see Figure 1b). Melting of the anode is thereby no longer a problem as it is already molten. Moreover, the high speed of the jet (in the range of 100 m/s) effectively transports the heat away and ensure an optimal surface constantly being regenerated for the electron impact. Thereby, significantly (currently about 70x) higher e-beam power densities can therefore be applied.

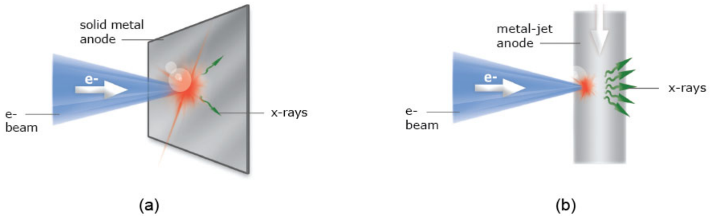

FIGURE 1. The principle of a solid anode X-ray tube (a) and a liquid-MetalJet X-ray tube (b).

We recently introduced two products that will improve the throughput and resolution needs of the semiconductor industry. MetalJet E1+ operates at 160kV and 1000W power on a 30 µm X-ray spot using 24keV energy alloy. Also, we introduced Nanotube N3 that operates at 160kV and provides a 150nm resolution for high resolution imaging needs.

APPLICATIONS

CD-SAXS

Research on critical dimension small angle X-ray scattering (CD-SAXS) using synchrotron x-ray sources show that this technology could potentially complement and replace optically based CD tools as critical dimensions and pitches become smaller and more complicated. CD-SAXS can be performed both in reflection and transmission geometry. Reflection geometry normally means that the measured area on the wafer becomes relatively large due to the low incidence x-ray angle. To overcome this a transmission geometry is normally used and in order to be able to penetrate the wafer with sufficient number of x-rays, photon energies higher than 20 keV are normally needed to get enough photons through the wafer for non-synchrotron CD-SAXS. Early results with the MetalJet source technology with indium K-α emission at 24 keV show great promise towards meeting the requirement needs of the semiconductor industry [2,3]. For more details on CD-SAXS results utilizing MetalJet technology see e.g. [4].

HRXRD

Various X-ray Diffraction (XRD) [5] techniques can benefit significantly from the high brightness achievable with the MetalJet X-ray source technology. This is becoming even more important as device structures are going from planar to 3D as well as when device design involves the introduction of a variety of carrier mobility enhancement engineering such as channel alloying e.g. SiGe and/or strain, one of the few ways to measure and enable control of this is via high resolution x-ray diffraction (HRXRD) and high-resolution reciprocal lattice mapping (HRRLM). Current state of the art solid x-ray sources are orders of magnitude from achieving throughput even close to what the industry is requesting [6] highlighting the need for a scalable X-ray source technology such as MetalJet sources.

XRR

X-ray reflectivity (XRR) is a method used to determine thickness, density and roughness of thin films. The high brightness and small spot of the MetalJet enable faster throughput and/or smaller measurement area. The shorter wavelength of Ga Kα compared to Cu Kα may also enable more accurate measurements of especially extremely thin layers for e.g. high-k gate stacks.

X-ray Microscopy

The highest available resolution in lab-based X-ray microscopes is achieved with zone-plate based projection microscopes [7] Such microscopes, however, typically use Cu Kα radiation which is not so well suited to resolve copper structures in silicon due to poor contrast between copper and silicon. As illustrated by Fig. 6, the Kα of Ga used in MetalJet sources, is just above the K-absorption edge of Cu [8] and thus much better suited to create a sufficient contrast between copper and silicon. First x-ray microscopy instrument using the MetalJet for Cu interconnect inspection was recently presented [9]

μXRF

Micro X-ray Fluorescence (μXRF) is used in the semiconductor industry to e.g. measure composition and layer thicknesses as well as detect contaminants. The x-ray beam is normally focused on the sample using capillary lenses or collimators. The higher brightness and subsequently a higher flux of X-ray on the sample provide by MetalJet could enable e.g. more measurement point on the wafer as well increased measurement precision and accuracy due to improved x-ray count statistics.

XPS/HAXPES

X-ray photoelectron spectroscopy (XPS) is readily used for measurements of a wide range of semiconductor parameters such as thickness, composition, bonding states, interface quality and surface condition. In standard XPS tools X-ray sources with characteristic photon energy around 1.5 keV are used. But recently the first lab based hard energy XPS (HAXPES) system utilizing the MetalJet source was introduced to the market [10]. The main benefit of using a higher photon energy is the possibility to probe deeper into the bulk of a sample. This expands the number of applications areas and reduces surface effects. This has potential in for examples nondestructive characterization of a full gate stack.

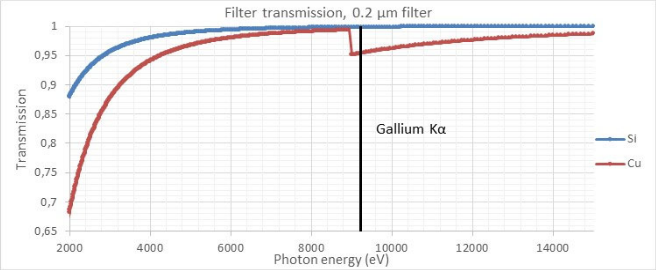

FIGURE 2. X-ray transmission trough a 0.2 μm filter of silicon and copper. The black line indicates the Kα of gallium [8].

Nano-CT

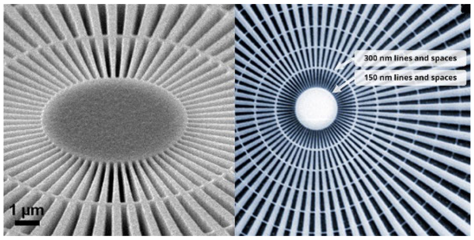

FIGURE 3. SEM micrograph of a Siemens star and an X-ray projection radiograph is shown on the right.

The Excillum NanoTube N3 enables industry-leading resolution and stability in geometric-magnification X-ray imaging systems with no need for manual tuning. The Excillum NanoTube N3 is based on advanced electron optics and the latest tungsten-diamond transmission target technology. Automatic e-beam focusing, and astigmatism correction ensures that the smallest possible, truly round spot is achieved every time, every day.
The NanoTube N3 also has the unique feature of internally measuring and reporting the current spot size. In addition, advanced cooling and thermal design results in extreme stability over long exposures. This enables an unprecedented true resolution of 150 nm lines and spaces.

In the publication we will discuss how MetalJet based x-ray tubes are reliable, robust high-end alternative to other lab-based X-ray sources and we will discuss some results that our customers shared that show the value of these sources in X-ray labs and industry worldwide.

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KEYWORDS

CD-SAXS, nano-CT, electronic inspection, XPS, micro-XRF, MetalJet, liquid anode, Nanotube

Temperature Dependent Thermal Conductivity Measurements of Thin Oxide Films Via Steady State Thermoreflectance

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INTRODUCTION

Continued dimensional scaling of materials in integrated circuits have resulted in major challenge in power dissipation and thermal management. These characteristic length scale reductions at all tiers of devices lead to temperature increases which accelerates the degradation of performance and reliability of very large scale integration (VLSI). As technology nodes push to the < 5 nm length scale [1], these thermal problems become more pronounced due to metal interconnect scaling resulting in reduced thermal conductivities, interfacial thermal resistances, and novel ultra-low-k amorphous dielectric layers that have intrinsically low thermal conductivities. Taken together, the increased, and often *unknown*, thermal resistances of lower dimensional materials that are comprising devices present a major bottle neck to performance and reliability of devices in continued device scaling. Without accurate knowledge of the thermal properties of the interfaces and materials at these reduced dimensions, these thermal mitigation challenges will become insurmountable as the field pushes to smaller technology nodes and to vertical architectures reliant on 2D and interface-dense heterogeneously integrated composites.

We describe a new method and commercialized measurement platform for measuring the thermal conductivity and thermal resistance of thin films and interfaces based on pump-probe thermoreflectance. As described in the following section, Steady State Thermoreflectance (SSTR) is a unique and powerful metrology to measure the thermal conductivity of wafers, the thermal conductivity and thermal resistance of thin films, and interfacial thermal resistance (ITR) at heterogenous boundaries [2]. Through our patented fiber-optically-integrated design [3], *Laser Thermal,*[4] has streamlined SSTR measurements through the development of SSTR-F (Steady State Thermoreflectance in Fiber). Here, we demonstrate the ability of SSTR-F to measure the thermal conductivity of low-k dielectric oxide thin films on silicon wafers over a temperature range from room temperature to 200 °C.

STEADY STATE THERMOREFLECTANCE IN FIBER (SSTR-F) – A NEW THERMAL METROLOGY AND MEASURMENT PLATFORM

Pump-probe thermoreflectance techniques have become an academic standard for the measurement of thermal properties of thin films and interfaces. Over the past two decades, time-domain thermoreflectance (TDTR) and frequency-domain thermoreflectance (FDTR) have demonstrated great advances in their power to resolve nanoscale thermal resistances. These techniques rely on laser-based heating (pump) and sensing temperature-dependent reflectivity changes (i.e., thermoreflectance) of the surface of materials with a secondary probe laser. By monitoring the probe-measured thermoreflectance changes as a function of time (TDTR) or pump-modulation frequency (FDTR), and comparing the measured data to solutions to the transient heat equation, the thermal resistances of nanoscale materials are determined with proper knowledge of the material's specific heat and density.

Recently, we have developed a new thermoreflectance technique – Steady State Thermoreflectance (SSTR) [5] – as a nanoscale thermal conductivity and thermal resistance measurement platform that monitors the steady state thermal response of materials over small volumes, thus providing a direct measure of thermal conductivity without any need to assume the specific heat or density of the material or thin film. SSTR utilizes a low frequency modulated pump beam to heat a sample for a long enough time for the pump-induced temperature gradient to reach steady state. The probe beam then monitors the thermoreflectance of the sample during these steady state conditions as a function of pump power. The resultant data of thermoreflectance vs. power is then fit to the Fourier Law to extract the thermal conductivity of the wafer or thin film of interest. The steady state temperature gradient is established over the pump-induced heater volume (c.f., Fig. 1a), and the lack of thermal transients over this heated volume greatly simplifies the measurement and reduces assumptions in the analysis, thus reducing measurement uncertainty. In prior works, we have used SSTR to measure the thermal conductivity of wafers with thermal conductivities from 1.3 - ~2,000 W m^{-1} K^{-1} [5], ITR across thin film interfaces [5], thin films with thermal conductivities as low as 0.05 W m^{-1} K^{-1} [6], buried substrates and sub-surface defect layers [7, 8], and thermal conductivity of wide-bandgap thin films (GaN and AlN) and their anisotropy [9-11]. Figure 1b shows a summary of room temperature thermal conductivity measurements of a range of materials using SSTR as compared to their accepted literature values. This demonstrates the versatility of SSTR for thermal conductivity measurements.

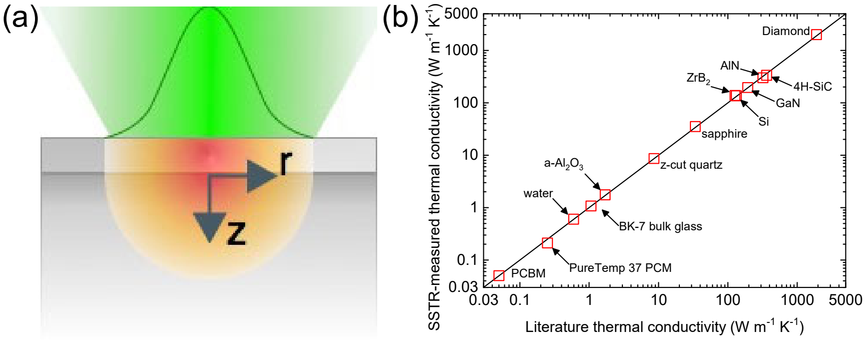

FIGURE 1. (a) Principle of SSTR measurement. Focused low-frequency modulated pump laser heats a near-surface sample volume to induce steady state conditions, while a secondary probe laser monitors the temperature response during steady state as a function of heat flux. (b) Thermal conductivity of a variety of material measured with SSTR as a function of accepted thermal conductivity form the literature.

Due to complexity in their optical design, implementation and thermal analysis, TDTR and FDTR are largely academic-lab-based metrologies and not suitable for non-expert users. The simplified measurement principle and analysis of SSTR overcomes these implementation limitations, through the patented fiber-optically-integrated design [3] by *Laser Thermal,*[4], we have developed SSTR-F (Steady State Thermoreflectance in Fiber). SSTR-F offers a highly repeatable and reproducible (better than 1%) thermal conductivity measurement tool that does not require the optical and thermal expertise required to maintain, use and analyze traditional TDTR and FDTR measurement platforms. In the following section, we demonstrate the use of SSTR-F to measure the thermal conductivity of thin dielectric films on silicon substrates.

THERMAL CONDUCTIVITY OF THIN DIELECTRIC FILMS ON SILICON SUBSTRATES USING SSTR-F

Using SSTR-F, we measure the thermal conductivity of a series of oxide thin films on silicon wafers. Prior to SSTR-F measurement, we coat the samples with a thin (~80 nm) film of Al to serve as an opto-thermal transducer. In practice, due to the steady state nature of the SSTR-F measurements, we are minimally sensitive to the thermal mass of the Al (heat capacity and thickness) as compared to TDTR or FDTR, which is a typical major source of uncertainty in TDTR and FDTR. We report on the thermal conductivity of oxide films with thicknesses of 98, 229, 287, 431, and 867 nm. For the thinnest three samples, SSTR-F measures the thermal resistance of the oxide layer in addition to the ITR at each adjacent oxide layer interface (Al/oxide and oxide/Si). Thus, following our prior work [12], we use the thermal resistance of this thickness skew and fit a series thermal resistor model to these data to determine the thermal conductivity of these amorphous oxide films. This approach is depicted in Fig. 2a, and the thermal conductivity of these samples is tabulated in Table 1. For the thickest two oxide samples, the thermal resistance is dominated by that of the oxide, and thus we report on direct measurements of the thermal conductivity of these films, tabulated in Table 1. The uncertainties in our measured values are calculated from spot to spot variation and propagation of uncertainty in the assumed parameters in our analysis, discussed in detail in our prior works [5, 7-11]. These SSTR-measured values agree well with our prior measurements of the thermal conductivity of amorphous thin film dielectrics on silicon using TDTR that we have reported previously [12-15].

Finally, we use SSTR-F to measure the temperature dependent thermal conductivity of the oxide thin films from room temperature to 200 °C. These data on the thin film oxides, shown in Fig. 2b, show a relatively constant trend with temperature, typical of an amorphous material.

TABLE 1. Thermal conductivity of oxide thin films

Film thickness nm	Thermal conductivity W m^{-1} K^{-1}	Uncertainty W m^{-1} K^{-1}
Determined from series resistance analysis on 98, 229 and 287 nm samples	0.96	0.04
431	0.96	0.04
867	0.96	0.03

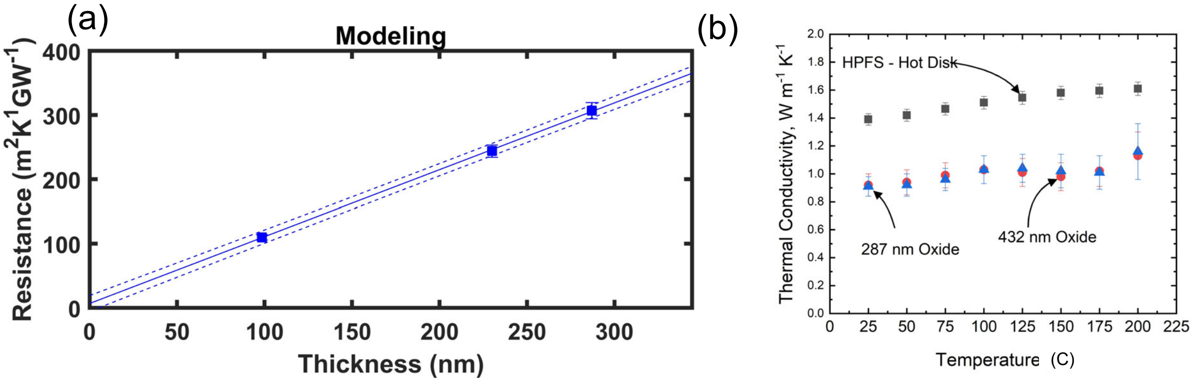

FIGURE 2. (a) Measured thermal resistance of the 98, 229 and 287 nm oxide films as a function of oxide film thickness. A series resistor thermal model is used to extract the intrinsic thermal conductivity of the oxide thin films, as described in our prior work [12]. The resultant thermal conductivity of the oxide films are tabulated in Table I. (b) Temperature dependent thermal conductivity of the 287 and 431 nm films from room temperature to 200 °C. The thermal conductivity of a control sample of high purity fused silica (HFPS Corning #7980) was measured via both SSTR-F and TPS Hot Disk.

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KEYWORDS

Thermal conductivity, low-k dielectric, pump-probe thermoreflectance, steady state thermoreflectance (SSTR), thin film thermal resistance, interfacial thermal resistance

Non-Linear Optical Critical Dimension Metrology

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INTRODUCTION

Process control and metrology of semiconductor devices rely heavily on linear optical light scattering, e.g. scatterometry and Optical Critical Dimension Metrology (OCD). In this presentation, we propose a completely new approach to semiconductor metrology based on *non-linear* optical scattering: NL-OCD. In this technique, Second-Harmonic Generation (SHG) is used to detect and measure nanometer-scale changes in critical dimensions for advanced device nodes. Results are presented demonstrating high sensitivity of SHG signals to dimensional changes in Gate-All-Around (GAA) test structures. Like OCD, NL-OCD is a fast, non-destructive measurement, making it suitable for inline process monitoring and metrology. Unlike linear scattering, SHG is a local, near-field effect that is highly sensitive to small dimensional changes. We envision NL-OCD helping to extend the use of optical scatterometry and OCD to future generations of semiconductor devices.

SECOND HARMONIC GENERATION FOR DIMENSIONAL METROLOGY

Linear light scattering, or scatterometry, is one of the workhorses of semiconductor fabrication: it is non-destructive, precise and cost-effective for inline process monitoring and dimensional metrology. Scatterometry has been extended both to UV and IR wavelengths, each with its own merits and applications.[1] Surprisingly, extending scatterometry for dimensional metrology by using *non-linear* optical processes has not been previously suggested or explored. In this work, we present the first results demonstrating the sensitivity of non-linear light scattering to changes in critical dimensions for gate-all-around test structures.

In our present work, we use Second-Harmonic Generation (SHG) of light as a probe of device geometry. The experimental layout is shown in Fig. 1. Femtosecond light pulses at about 800 nm (red light) are focused onto a 20µm spot on the surface of the sample. Almost all of these red photons are scattered linearly—standard light scattering—and the wavelength does not change; however, occasionally two red photons combine at the sample to produce a blue photon at 400 nm. This is highly dependent on the local structure of the sample: smaller structures can generate much more SHG light than larger structures.[2]

A schematic diagram of how device structures create SHG light is shown in Fig. 2: Nanometer scale three-dimensional features of the Gate-All-Around structure act as small SHG emitters. While the wavelength of the light is large compared to the emitters, there is a local concentration of the electric field inside the structures. These high electric fields—on the order of 0.1 to 1 V/nm, generate strong SHG signals that depend on local geometry and beam polarization. Therefore, NL-OCD is a *near-field, localized* measurement of the device geometry. The input beam spot size, 20 µm, combines the signals from tens of thousands of devices—each one an individual emitter of SHG. Unlike normal (linear) OCD, SHG is generated equally well on randomly placed devices as it is local to the individual structure and does not rely on any sort of periodic "grating" effect. Therefore, we expect that NL-OCD will be able to be used on actual product for both memory and logic devices, and not necessarily require test structures.

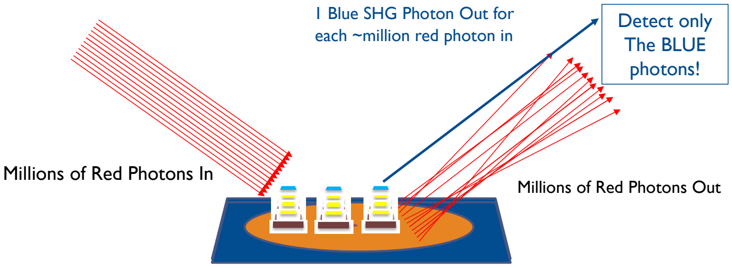


FIGURE 1. Linear and non-linear scattering of light. Input beam is red light (800 nm) from a pulsed laser; the detector filters out red light, accepting only blue light (400 nm) with a defined polarization (S or P). The blue photons are created by SHG in small features in the sample. There is no significant background signal from the bulk materials.

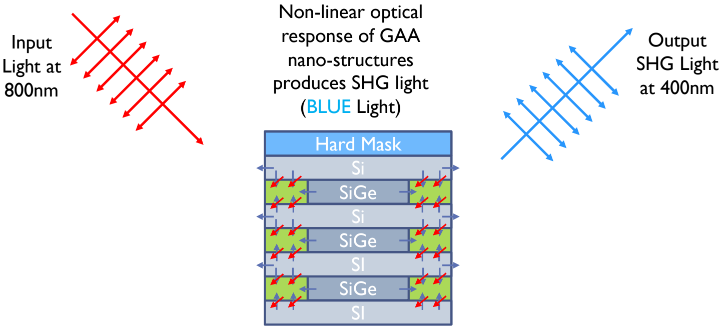


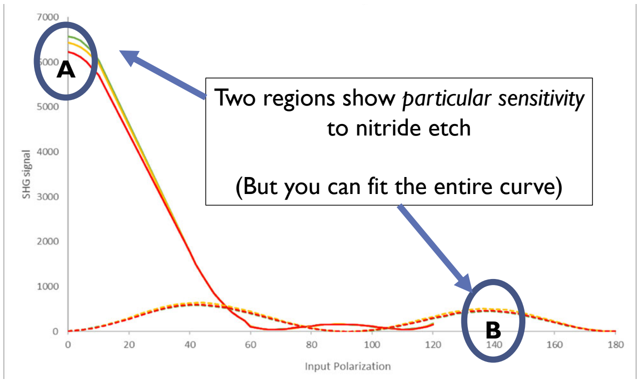
FIGURE 2. Schematic diagram showing SHG in nanoscale devices. SHG is created in regions of very high electric fields, which are located in or near the 3D Gate-All-Around (GAA) structures. These structures act like miniature emitters for SHG. Changing the polarization of the input beam excites different modes of the emitters.

Typical polarization scans of the SHG signal vs input polarization are shown in Fig. 3. These curves can be used to detect changes in dimensions, such as the sensitivity to inner-spacer etch shown in Fig. 4. This sensitivity can be used as a line monitor to detect process variations in etch or deposition, for example. The geometry of the test structures is shown in figure 5.

Like OCD, NL-OCD is not a direct imaging technique. Therefore, it requires a model to translate SHG signals into precise physical dimensions. Modeling for OCD is complex and time-consuming, in large part due to "prior-layer" effects: OCD signals depend not only on the structure of interest, but on previous layers that are not of interest. Also, there is not a one-to-one correspondence between the scatterometry signal and a single geometric parameter—they are all coupled together. One advantage of NL-OCD is that previous layer effects are small, since the signal is generated almost entirely by the structures of interest. Instead of looking for a small change on a large background, NL-OCD is looking at a relatively large signal on a low background. Because SHG is a local, near-field effect, the signal strength and polarization is more-or-less directly coupled to device geometry. Nevertheless, we anticipate significant work will be required to interpret SHG signals to produce precise, unique metrology results. As a production line monitor, however, models are not necessarily required to detect process changes in etch or deposition.

CONCLUSIONS

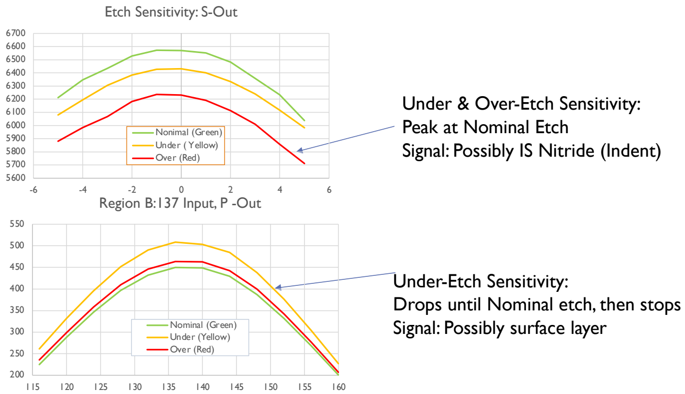
NL-OCD is a completely new technique for advanced semiconductor metrology and line monitoring. It uses SHG, Second-Harmonic Generation, as a local, near-field probe of small device geometry. Advantages of the technique are high-sensitivity to small geometry changes, no need for periodic test structures and low background signal from previous layers. Being a new approach to metrology, significant work will be required to develop this technology into a complete metrology product, but early results are promising.



Two regions show *particular sensitivity* to nitride etch

(But you can fit the entire curve)

FIGURE 3. SHG intensity vs. input polarization for the Test Structure shown in Figure 3. The two curves are for P and S output polarizations.



Under & Over-Etch Sensitivity:
Peak at Nominal Etch
Signal: Possibly IS Nitride (Indent)

Under-Etch Sensitivity:
Drops until Nominal etch, then stops
Signal: Possibly surface layer

FIGURE 4. SHG sensitivity to nitride inner-spacer etch. The SHG signal at points A and B in Fig. 4 are shown as a function of nitride etch.

GAA Test structures

120 nm pitch

11.5 nm indent (SiGe etch)

11.5 nm TiN deposit for
inner spacer

Desired Etch: 0 to 12 nm
(under-to-over etch)

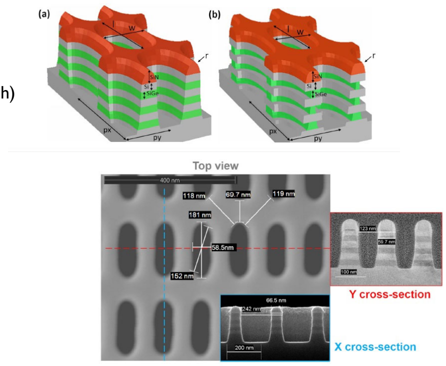


FIGURE 5. Gate-All-Around (GAA) test structures used for NL-OCD feasibility tests. These test structures are fabricated specifically to evaluate different metrology techniques for Gate-All-Around geometry.

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KEYWORDS

Semiconductor, metrology, OCD, Gate-All-Around, scatterometry, Second-Harmonic Generation, non-linear optics

EUV Imaging Reflectometer for Non-Destructive Compositional Mapping of Nanoelectronics

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INTRODUCTION

With the introduction of extreme ultraviolet (EUV) lithography, many next-generation semiconductor devices now have features and interfaces fabricated with near-atomic-level precision. This drives a critical need for high-resolution, non-destructive metrology techniques capable of structural and compositional characterization.

Coherent EUV beams can enable new nanometrology techniques with potential to image with higher resolution than current approaches, thus supporting future nodes of EUV lithography. The short wavelength of the incoherent EUV light (10 – 100 nm) used in lithography makes it possible to reduce the printable feature sizes in accordance with the Rayleigh criterion; that same advantage is equally applicable to microscopy, where the smallest resolvable transverse feature size, as well as sensitivity to depth-features (such as layer thickness and surface roughness), are determined by the used wavelength [1]. In addition, EUV light penetrates through many materials that are opaque to visible light, allowing non-destructive imaging of buried interfaces and structures [2]. Finally, EUV light has an exquisite elemental sensitivity that can be utilized for compositional measurements. Calculation of optical properties of an arbitrary material in the EUV spectrum is straightforward as long as its density and atomic composition are known, making the wavelength range suitable for study of newly developed materials.

Traditional microscopy using EUV light is challenging, as no refractive optics exist in this region of the spectrum, and diffraction-based optics are lossy and imperfect. Fortunately, computational imaging approaches provide a powerful way to circumvent this problem. Ptychographic coherent diffractive imaging is a robust lens-less imaging technique, in which a coherent beam is scanned over an object at partially overlapping positions, and the resulting diffraction patterns are recorded. The overlap provides information redundancy, which allows iterative computational algorithms to reconstruct the reflectance or transmittance image of the object from the diffraction patterns [3,4]. The object is reconstructed in both amplitude and phase, the latter of which gives enhanced sensitivity to the material composition and the topography of the object being imaged.

Here, we present an EUV coherent diffractive imaging reflectometer that fully harnesses the strengths of EUV imaging. By collecting ptychographic phase-and-amplitude-reflectance images of an object at multiple incidence angles, our microscope generates complex reflectance curves as a function of both incidence angle as well as transverse location on the sample. This information can then be used to solve for the depth-dependent composition of chosen regions on the sample in a manner akin to traditional reflectometry, but with higher resolution and enhanced material sensitivity from the phase. Our microscope is illuminated by coherent EUV high harmonic beams [5], allowing it to utilize the high spatial resolution and chemical specificity inherent to EUV light from a tabletop setup. This technique achieves non-destructive compositional mapping at high resolution, which is a capability not covered by many existing techniques, that either require cross-sectioning or ion milling of the sample, or only measure over an averaged area across the object and thereby have poor spatial resolution.

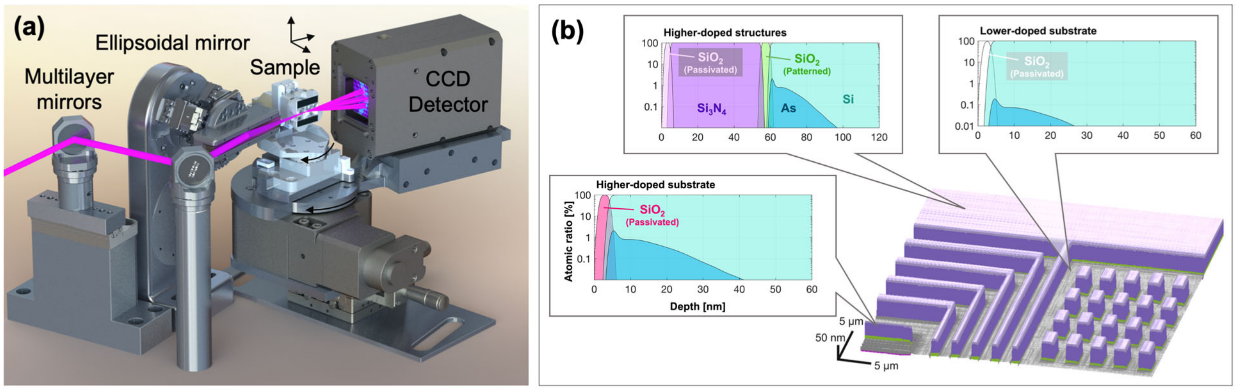

FIGURE 1. Demonstration of EUV imaging reflectometry. (a) Experimental setup. Out of a comb of EUV wavelengths from high harmonic generation, a single harmonic is selected by multilayer mirrors. The beam is then focused by an ellipsoidal mirror onto the sample. Diffraction patterns for ptychography are collected at multiple incidence angles on a CCD detector. (b) The reconstructed sample, showing the transverse structures and the depth-dependent composition for multiple lithographic regions.

IMAGING OF A LITHOGRAPHY SAMPLE

We demonstrated EUV coherent diffractive imaging reflectometry on a lithography sample provided by Interuniversity Microelectronics Centre (Imec) [6]. It has 50 nm tall Si_3N_4 structures on top of Si substrate with regions of 0.1 or 1 atomic percent arsenic doping (5×10^{19} and 5×10^{20} atoms/cm^2 respectively) that vary independently of the surface structures.

To generate the EUV illumination via high harmonic generation, 0.79 µm wavelength Ti:sapphire laser was focused into an argon-filled hollow-core optical fiber. The residual driving laser was filtered out using two Si super-polished substrates oriented near Brewster's angle for the 0.79 µm wavelength, as well as two 200 nm thick aluminum filters. The microscope setup is shown in Fig. 1(a). The 29.3 nm harmonic was selected out using a pair of SiC/Mg multilayer mirrors. This beam was then focused onto the sample using an ellipsoidal mirror to a spot size of around 10 µm × 10 µm at normal incidence. The sample and the CCD detector were mounted on a stage stack that allows for in-plane scanning of the sample, as well as control of the incidence angle of the illumination.

Five ptychographic reconstructions were obtained for incidence angles between 21° and 25° from grazing in 1° increments. The image stack contained reflectance vs. angle information for each region of the sample. The images were then segmented into different lithographic regions, and numerical optimization was performed to find the depth-dependent compositional model of the sample that matches the obtained reflectance curves.

The full reconstruction of the sample is shown in Fig. 1(b). The image shows a 3D rendering of the sample, which combines the transverse information obtained from a single ptychographic image and the depth-dependent compositional information solved using the reflectance vs. incidence angle information. The depth model solved for separate regions are shown in the inserts. Notably, in the final solved-for model, we obtained confidence intervals of <1 nm for surface topography and layer thickness parameters, and these parameters agreed well with correlative metrology that was performed using atomic force microscopy, secondary-ion mass spectrometry, and scanning transmission electron microscopy. The transverse resolution for the reconstructed image was estimated to be 64 × 172 nm.

CONCLUSION

We have demonstrated EUV coherent diffractive imaging reflectometry, a novel technique for compositional mapping of nanoelectronics. Our technique is non-destructive; while compositional analysis does rely on an initial guessed model of the sample, no cross sectioning or milling is required. The technique also has high spatial resolution, which means that it can be used even on non-periodic nanostructures, and allows identification of any fabrication defects and contamination, which can be included or avoided in the compositional analysis as needed. The technique has a balance of transverse resolution (10s of nm), depth precision (<1nm), and field-of-view (10s of µm), which is well suited for measuring nanoelectronics.

We expect this technique to be useful for metrology of a range of nano-electronic systems and parameters. For example, we expect the technique to be able to measure density of semiconductor-relevant materials integrated within a system; density can be altered in nano-systems due to phase changes or strain from neighboring layers, and this can be difficult to measure, especially in a spatially-resolved manner. The technique could also be used for identification and characterization of unexpected layers, contamination, or etching that arise from fabrication.

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KEYWORDS

EUV Metrology, Coherent Diffractive Imaging, Ptychography, High Harmonic Generation, Reflectometry.

Half Wavelength Contact Acoustic Microscopy (HaWaCAM): a novel semiconductor metrology technique

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INTRODUCTION

Ever more functionality and processing power is being integrated on the same semiconductor area. As a consequence the device structures have become 3D. Also, 3D NAND stack heights keep increasing. Metrology is needed to cost effectively fabricate said devices at very high throughput. Currently, optics-based equipment is the non-destructive inspection workhorse of the semicon industry. Unfortunately, this modality is hampered by the presence of optically opaque layers and limited detection depths ($<O(1\ \mu m)$) at resolutions (wavelength) of ~0.2 – 1.5 µm. Several methods are being researched to detect and characterize buried nanoscale structures in hard solid samples. One of those techniques is acoustics based. Acoustical waves are not hampered by optically opaque layers. Also, the penetration depth of acoustic waves may be >>10 µm depending on the frequencies used. Moreover, the pulsed/broadband nature of acoustic measurements combined with the easily measurable phase of acoustic signals means obtaining a 3D representation of a sample is relatively straightforward.

Traditional acoustic microscopy uses a single element transducer and operates in pulse-echo mode [1]. Typical frequencies range between 0.05 – 1 GHz. The most common transduction mechanism utilized in said transducer is piezoelectric in nature. The aperture size of the single element is usually >> 1 wavelength. Hence, a geometric lens is used to focus the acoustic beam and to obtain a good lateral resolution. A liquid coupling layer (eg. water) is used to couple the acoustic waves into the sample. The curved shape of the lens in combination with piezomaterial radii of >0.1 mm lead to coupling layer thicknesses >> 10 µm. The necessity of the coupling layer limits the acoustic frequencies used in acoustic microscopy for semicon applications in two fundamental ways:

1) The sound attenuation in the liquid (water) coupling layer follows a quadratic frequency dependency. At 1 GHz the attenuation in water is 0.22 dB/µm at 20°C, however at 4 GHz this increases to 3.5 dB/µm.
2) The solid materials used in the semiconductor industry often have much higher acoustic impedances (eg 17.4 MRayl for Si) than those of practical coupling liquids (eg. water 1.5 MRayl). Thus, the transmission coefficients at the transducer-liquid couplant and liquid-sample interfaces are generally low. Next to low signal levels, this also means dealing with spurious multiple reflections polluting the received signals.

Furthermore, the presence of a strong geometric lens in conventional acoustic microscopy causes a limited focal depth. Thus, to create a high quality 3D sample representation scanning in x,y and z directions is needed.

Here, we present a novel method for high frequency acoustic metrology of buried structures in solid samples. In contrast to traditional acoustic microscopy solid-solid contact with the sample is used without the need for liquid coupling layers. This allowed for higher frequencies (4 GHz) and only scanning in x and y dimensions was needed.

SIMULATION AND EXPERIMENTAL SETUP

HaWaCAM Concept And Prototype Device

The half wavelength contact acoustic microscopy (HaWaCAM) instrument consisted of a GHz piezotransducer mounted on top of a probe. The probe interfaces with a sample without the use of liquid couplants. The probe featured a blunt tip. A certain static force was applied to the probe to ensure that the tip-sample contact diameter was O(half a wavelength) without causing damage to the sample. HaWaCAM operation is as follows: the transducer transmits a GHz acoustic wave into the probe, which then travels through the probe and the tip-sample interface into the sample. The acoustic wave is scattered by subsurface features and the scattered energy travels back up toward the surface of the sample, through the tip-sample interface and is converted into electrical signals by the transducer. All acoustic wave propagation effects occur in the linear regime. Custom probes with a 4 GHz circular symmetric piezotransducer integrated on top of the probe tip were developed. AlN piezomaterial was used. The probe tip was blunt (tip radius > 10 µm). See Fig. 1a for a schematic image and Fig. 1b for a zoomed image of a realized probe.

FIGURE 1. A) schematic image of HaWaCAM concept. B) SEM image of an actual realization of the tip.

Modeling, electronics, algorithms samples

To design the HaWaCAM instrument a number of models were used: the 1D KLM model [2], custom analytical models and COMSOL finite element modeling. The electronic signal chain was as follows: an arbitrary waveform generator generated a linear chirp (-6 dB bandwidth 1.7 – 5.9 GHz, length 5 ns), which was amplified and routed via a custom designed switching board to the piezo-element. The switching board was able to switch within 15 ns from transmit to receive mode. The signals received by said piezoelement were routed via the switching board to a preamplifier and digitized by an oscilloscope. Per measurement location 400 traces were averaged – the acoustic measurement time was 0.4 ms. The post-processing algorithms consisted of a number of steps: chirp compression, corrections for trigger jitter and variations in the static force, imaging based on a wavenumber-frequency domain mapping [3], time windowing, frequency filtering and f-k_x filtering. Two samples were measured. The first (see Fig. 2A) consisted of silicon with 1D feature arrays buried below a 9.7 µm SiO_2 top layer. The second (see Fig. 2B) consisted of silicon with 2D arrays of features buried below 5 µm PMMA.

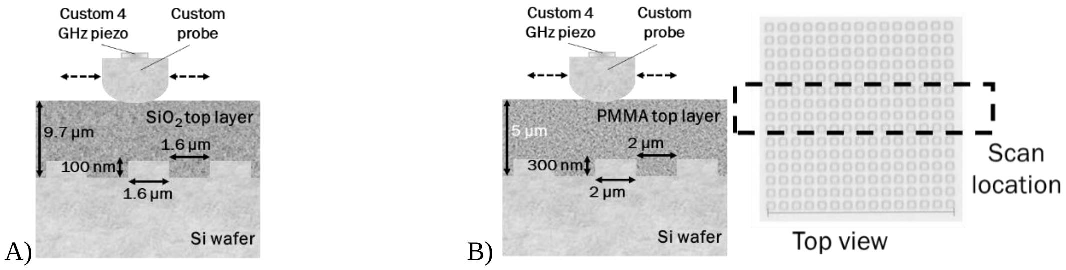

FIGURE 2. A) 1D grating buried below SiO_2 top layer. B) 2D matrix grating buried below PMMA top layer.

RESULTS AND DISCUSSION

Fig. 3 shows the measured time signals with the probe in air (blue), with the probe on top of a feature (green) and with the probe off feature (red) for the sample consisting of a 1D grating buried below a SiO_2 top layer (see Fig. 2A). The time axis is zoomed to around the tip-sample interface echo.

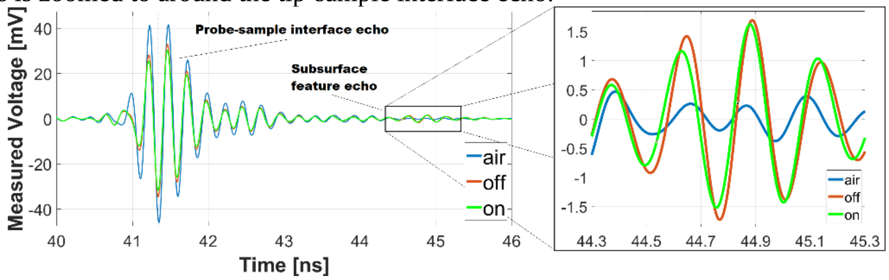

FIGURE 3. Measured pulse-echo signals in air, on a feature and off feature, for the sample shown in Fig 2A.

As Fig. 3 shows there was no subsurface echo, if the probe was in air. If the probe touched the sample, a subsurface feature echo was present. Said echo arrived ~3.3 ns after the tip-sample echo, which corresponded well with an SiO_2 thickness of 9.7 µm and an acoustic wave speed of SiO_2 of 6000 m/s. If the probe was on top of a feature the subsurface echo arrived earlier compared to the case that the probe was off feature. The ~20-25 ps arrival time difference corresponded well with the subsurface feature geometry and the acoustic wave speed of SiO_2.

Fig. 4 details measurement results obtained on the sample containing the matrix grating buried below 5 µm of PMMA. To obtain these results the postprocessing algorithm described earlier and a cross-correlation operation to extract the local time differences as a function of the X and Y coordinates relative to a reference signal was applied.

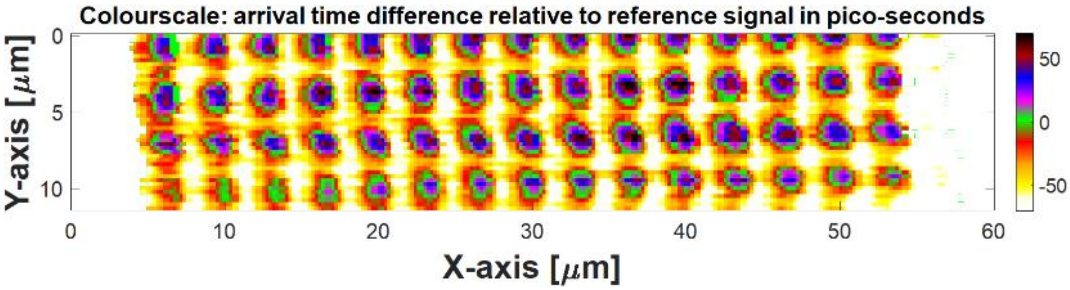

FIGURE 4. The arrival time difference of the subsurface grating echoes relative to a reference. The colour scale indicates the time differences in ps. See Fig. 2B for the sample description.

Fig. 4 shows a clean representation of the 4 rows of subsurface features present within the scan area (see Fig. 2B). The peak-to-valley time differences between the on and off feature echoes was ~140 ps. This corresponded well with twice the arrival time difference between the middle of a through between features and a top corner point of a feature (assumed PMMA compressional wave speed: 2750 m/s).

Compared to traditional acoustic microscopy, HaWaCAM requires no coupling layer. Thus higher frequencies and resolutions can be reached, as the attenuation in solids typically has a linear frequency dependency whereas that in liquids is nonlinear. Also, the use of wavenumber-frequency domain mapping means it is also faster: only an x,y-scan is needed for a 3D image in contrast to the x,y,z scan required for regular acoustic microscopy. Currently, the acoustic measurement time is ~0.4 ms/point, but it is expected that this measurement time may be increased by up to an order of magnitude after optimization. Please note that the mechanical measurement time is currently O(s) per point. This is not fundamental, it was simply not optimized yet. Taking into account our experience with Atomic Force Microscopy systems we expect mechanical measurement speeds of 0.1 – 1 ms per point to be feasible.

CONCLUSION

In this work a new technique for GHz acoustic metrology of subsurface structures in solid samples was presented. The method uses solid contact between the probe and sample, thus requiring no coupling liquids. This enables the use of higher frequencies (4 GHz – wavelength 0.75 µm in PMMA, 1.5 µm in SiO_2), compared those commonly used in conventional ultrasonic microscopy (< 1 GHz). The technique is not hampered by optically opaque layers, features a penetration depth of O(10s of µm) and is nondestructive/nondamaging.

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KEYWORDS

Half Wavelength Contact Acoustic Microscopy, HaWaCAM, GHz acoustic metrology, solid contact.

Accelerating Accuracy and Speed of Packaged-Device Nanoscale Characterization and FA Using a Novel LaserFIB Workflow

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INTRODUCTION

Microscopy at various length scales is a core technique required for characterization of package materials, interconnects, and defects, from their earliest research stages to product development, manufacturing and failure analysis (FA). Features must be observed that are both nanoscale and site-specific. The ability to achieve this becomes challenged by the emerging and growing trend of heterogeneous integration, which makes packages more complex. Packages are continuously becoming larger in their footprint, while at the same time, more complex and often including 3D architectures with higher I/O densities and shrinking of package interconnect size and pitch. Combined with the existing nanoscale and site-specific requirements, this complexity has created added demands on targeting, navigation, and access to a desired region of interest which could reside at varied locations potentially deep within a relatively large 3D volume. Doing this efficiently requires leveraging the relative strengths of different instruments and doing so in a coordinated fashion. This paper presents a correlated microscopy-based workflow consisting of non-destructive 3D X-ray microscopy (XRM) and a focused ion beam scanning electron microscope (FIB-SEM) equipped with an integrated femtosecond laser (referred to as LaserFIB) to perform four steps: visualize, target, access, analyze.

INTRODUCTION TO 3D MICROSCOPY TECHNIQUES

Introduction to the X-ray Microscopy (XRM) technique

3D X-ray microscopic imaging offers the ability to visualize internal features non-destructively. Compared to microCT, XRM uses an optically-coupled scintillator design to deliver 'Resolution-at-a-Distance' with submicron-scale spatial resolution even within relatively large (50+ mm) packages.[1] Furthermore, recent developments of deep learning AI-based X-ray tomography reconstruction are now being employed as a new way to accelerate XRM characterization by collecting fewer projection radiographs – increasing scan speed up to a factor of 10X, while maintaining submicron-scale information.[2] But compared to electron microscopy-based approaches, limitations still exist regarding spatial resolution and acquisition time, and these motivate the use of a correlative approach with other instruments.

Introduction to FIB-SEM with integrated fs-laser

Focused ion beam scanning electron microscopes (FIB-SEM) combine the strengths of nm-scale imaging and analytics and the ability to access site specific locations beneath the surface. However, the milling rates achievable with a FIB limit the volume of material that can be removed in a practical timeframe to depths on the order of ~100 microns for Ga ions, and several hundred microns for Xe ions. This presents a problem for new advanced packages. The recent introduction of a femtosecond laser ablation system integrated with the FIB-SEM instrument overcomes this problem by extending the milling capability to much deeper (mm) and faster (seconds to minutes) dimensions, while also serving as the critical bridge between the XRM and FIB-SEM techniques to fully benefit from the strengths of each as is described in the following 4-step workflow.[3]

Experimental Methods: A 4-Step Workflow for Rapid and Accurate Characterization of Buried Defects

To date, current approaches for accessing features, defects, or failures deep within semiconductor packages typically involve physical cross sectioning by mechanical sawing, grinding and polishing, broad ion beam, focused ion beam (usually Ga or Xe), or standalone laser ablation systems. These approaches do not provide the combination of speed, targeting, and end-pointing accuracy required to address increasingly complex devices with the desired throughput and success rate.

A new alternative is presented below, combining hardware and software technologies into a unique solution for nanometer-scale imaging and analysis at site-specific locations in 3D space within complex packages and devices, accomplished in a matter of hours.[4] The 4-step workflow consists of: visualize, target, access, analyze. The steps are described below and in Fig. 1, with the enabling hardware and software along with processing times presented in Table 1.

Visualize: 3D X-ray microscopy is used to provide a non-destructive view of the defect after fault isolation but prior to any physical cross sectioning. This helps to understand the nature of the defect at the micron scale while maintaining the feature in its native state. This step is now accelerated by AI-based tomographic reconstruction.

Target: Using the XRM data, the position of the buried defect is determined relative to the sample surface (as viewed by optical or SEM imaging, or in this case FIB-SEM). This involves data registration (tilt, pixel scaling, X-Y-Z positioning) based on either natural or artificial surface fiducials. An approach using a laser-patterned surface fiducial is depicted in Fig 1b and 1c. Once the defect is targeted with relation to the surface, laser milling geometries and protocols are defined, accounting for taper of the laser cut and final polish using the gallium focused ion beam.

Access: The ability to access specific regions deep within a sample, with micron-scale positioning accuracy, is a unique capability of ultrafast laser ablation. The ultrashort pulses ensure minimal damage (athermal) to the surrounding material and enable milling to proceed orders of magnitude faster than using either Ga or Xe FIBs. Often more than one step of laser milling will be employed – the first for a fast rough cut, and additional step(s) at lower laser power for fine polish. Following laser milling, the Ga FIB can be used to remove any redeposition and provide a quick final polish of the exposed cross section at the region of interest.

Analyze: Once exposed on the face of a cross section, nanometer-scale characterization of the feature or defect can be completed using SEM. The operator has full access to the range of SEM and FIB capabilities including different detectors or analytics.

An example based on characterizing a defect in an OLED device is depicted in Fig. 1.[5] While this paper describes a 4-step workflow for cross-sectional observation of deeply-buried regions, variations on this process can be realized to produce other geometries including TEM lamella, atom probe tomography samples, or nanoscale XRM samples for locations deep within a sample. In each instance, the fs laser integrated on a FIB-SEM instrument serves as the missing link that enables the 4-step workflow for nanoscale analysis or sample preparation anywhere within semiconductor packages, using XRM data as a roadmap to target the 'needle in a haystack'.

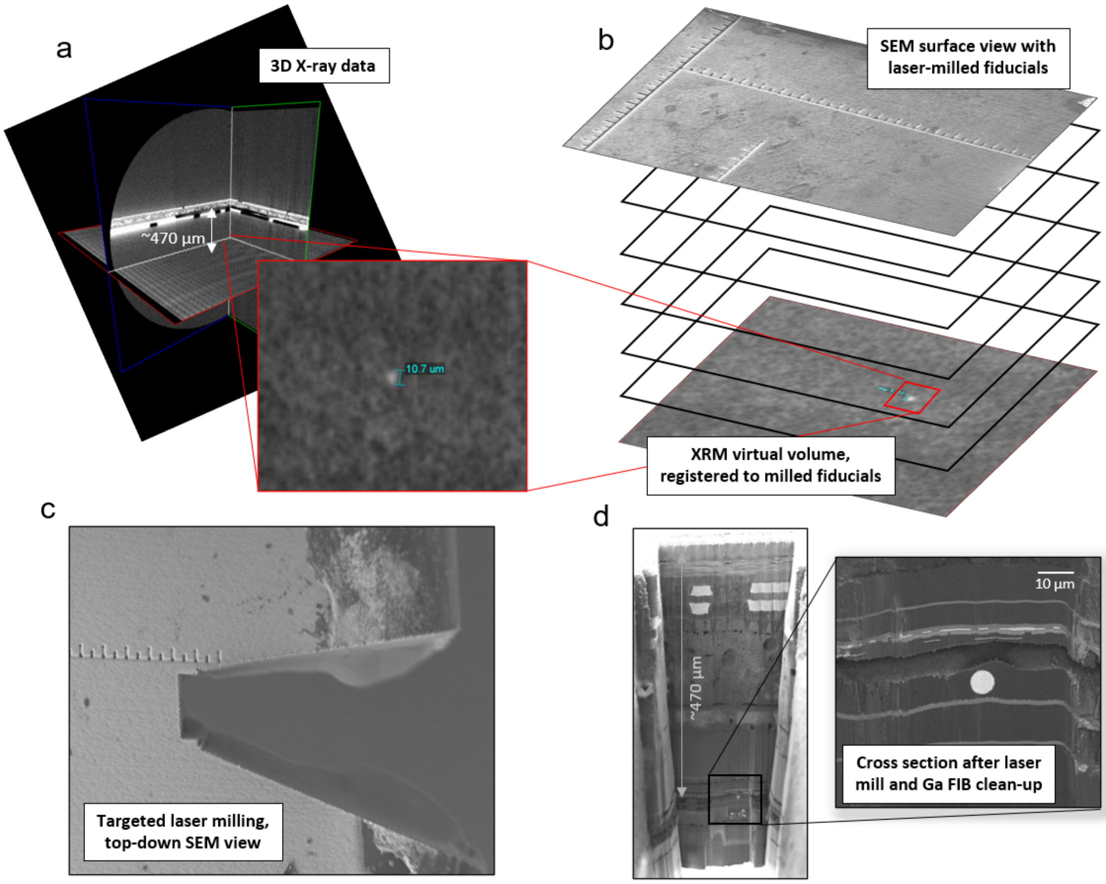

FIGURE 1. The 4-step workflow. a) Visualize: A defect is visualized by the XRM data, shown here residing ~470 microns deep in the sample in a virtual cross-sectional slice. b) Target: The location of the defect is targeted in depth (relative to the top surface of the XRM data overlaid to the SEM view) and lateral position (relative to a ruler grid fiducial pattern that has been pre-machined in the sample surface). c) Access: The same fiducials are used to define the location for fs laser milling to gain rapid and targeted access to the defect. d) Analyze: After laser milling and several minutes of FIB polishing, the defect is visible for nanoscale analysis.

TABLE 1. 4-step workflow summary

Workflow Step	Enabling Technology	Process Time	Resolution / Accuracy
Visualize	Xradia Versa w/ DeepRecon Pro	1 - 2 hours	single micron resolution
Target	Atlas 5 on ZEISS Crossbeam	10 minutes	<5 micron positioning
Access	LaserFIB: laser and Ga FIB	30 minutes	nm-scale endpointing
Analyze	ZEISS Crossbeam	5+ minutes	single nm resolution

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KEYWORDS

X-ray, FIB-SEM, laser ablation, correlative, microscopy

Machine learning-assisted characterization of hafnia-based ferroelectric thin films

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INTRODUCTION

The recent discovery of ferroelectricity in CMOS compatible hafnia-based dielectrics has led to a resurgence in interest in ferroelectric field-effect transistors (FEFETs) for use in advanced microelectronics, which had previously been considered unviable technology [1]. This technology has the potential to enable merging logic and memory functions in a single device, addressing some of the most demanding hardware requirements for new computing paradigms, which is driven by data-centric applications. If the semiconductor industry can deliver technology to support this new paradigm it could result in the next wave of exponential growth in the semiconductor industry, potentially evolving it into an over-a-trillion-dollar business [2].

Previous literature reports have demonstrated that the non-centrosymmetric orthorhombic phase is responsible for ferroelectricity in these materials, however in thin-film form, their microstructure can vary greatly in terms of phase distribution (main phases present in this material are ferroelectric non-centrosymmetric orthorhombic $Pca2_1$, centrosymmetric orthorhombic $Pnma$ and $Pbca$, monoclinic $P2_1/c$, tetragonal $P4_2/nmc$, and cubic $Fm\bar{3}m$ phases), grain radius (2–50 nm), orientation, and grain boundaries. All of these film properties may depend on the processing scheme used. As a result, establishing the links between process, microstructure, and performance for this type of material has remained challenging [2–4].

The microstructure of these films has been studied with a wide range of advanced microscopy techniques to understand the correlation between microstructure and ferroelectricity. In-situ scanning transmission electron microscope (STEM) and high-resolution transmission electron microscopy (HR-TEM) were utilized to investigate the evolution of microstructure and domain dynamics in real-time during electrical biasing [5–7]. Nano-beam electron diffraction (NBED) as an advanced TEM technique can be employed for obtaining local diffraction information of material with nanoscale resolution over length scales as large as 1-2 µm and high spatial resolution with an electron beam diameter as small as 1 nm, enabling detailed investigation of grain size, phase, and orientation [8, 9]. Additionally, 3-dimensional analysis such as atomic-scale tomography can provide further details of grain structure and interfacial properties within these thin-film materials [7]. Coupling these techniques with computer vision capabilities can automate and accelerate microstructure analysis and consequently establish a more accurate process-structure-property (PSP) relationship of these advanced materials. Here we discuss two machine learning approaches i.e., supervised and unsupervised learning to automate the characterization of the crystal structures and orientation of hafnia-based ferroelectric thin films using electron diffraction patterns.

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SUPERVISED LEARNING

Literature has shown that Convolutional Neural Networks (CNN) can be used as a supervised learning method for analysis of TEM diffraction patterns (DP) data [10]. CNN is a class of deep neural network, most commonly applied for supervised computer vision tasks [11]. For supervised learning, a large labeled dataset of DP's is required. As acquiring a large dataset of experimental DP's and manually labeling them can be a cumbersome task, simulation software such as CrystalKit and Landyne can be used to simulate the DP's for various crystal structures and zone axis to be used for training a CNN. The trained CNN, then, can be applied to identify the crystal structures and zone axis in the experimental DP's. **Figure 1** shows examples of the simulated DP's of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) material.

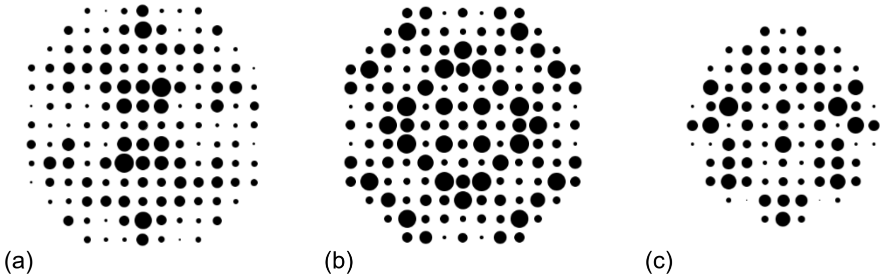
(a) (b) (c)

FIGURE 1. Simulated diffraction patterns of HZO (zone axis: [001], high voltage: 300 kV) (a) Monoclinic (space group 14), (b) tetragonal (space group 137), and (c) orthorhombic (space group 29)

UNSUPERVISED LEARNING

There are challenges in applying the supervised learning approach such as difficulty in generating the labeled experimental data required for training purposes, and lack of knowledge about the crystal structures and orientations of the manufactured HZO materials required for the simulation of the diffraction patterns. Therefore, unsupervised learning can be implemented to face these challenges. In this approach, unlabeled data can be used to find clusters in the dataset corresponding to the various crystal structures and orientations. For this purpose, methods such as K-means and non-negative matrix factorization (NMF) can be used [12]. K-means makes inferences from datasets using only input vectors without referring to labelled outcomes, and groups similar data points together to discover underlying patterns. To achieve this objective, K-means looks for a fixed number (k) of clusters in a dataset [13].

Nano-beam electron diffraction technique can be employed to generate a large dataset of diffraction patterns that can be used as a training dataset. Then unsupervised learning approach can be utilized to find the clusters in the DP's associated with different crystal structures and their orientations. **Figure 2** shows an NBED scan of the semiconductor materials and few examples of the DP's contained in the scan.

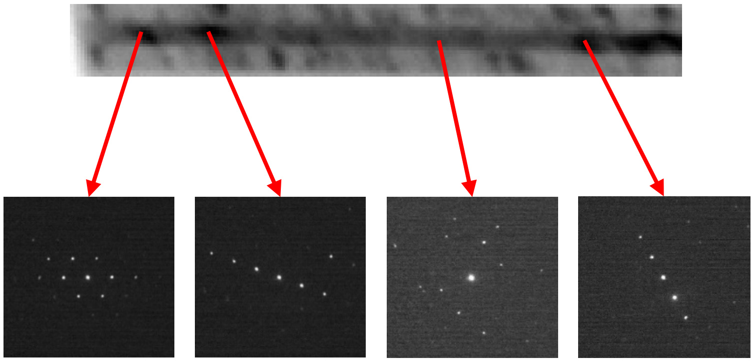

FIGURE 2. NBED scan and diffraction patterns

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KEYWORDS

Computer vision, ferroelectric field-effect transistor, neuromorphic computing, supervised machine learning, unsupervised machine learning

Recommissioning the Length Scale Interferometer at the National Institute of Standards and Technology and Application to Length Traceability for Nanoelectronic Manufacturing

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INTRODUCTION

Many principles of dimensional metrology and instrument design are applicable across all length scales, from macroscale parts measured using coordinate measuring machines (CMMs) down to nanoscale features imaged using electron microscopy. Some approaches to traceability to the International System of Units (SI) meter—such as the use of the silicon lattice spacing to calibrate high resolution transmission electron microscopy—are unique to metrology at the nanoscale. However, methods such as displacement interferometry are applicable across a wide range of length scales and have been incorporated into many types of measurement systems. In some cases, it is possible to use methods and instruments that were designed or intended for measurements over larger distances for applications at the microscale or even nanoscale. This type of linkage across different length scales can enable cross-validation of different metrology techniques. The National Institute of Standards and Technology (NIST) Length Scale Interferometer (LSI) is an instrument originally intended for dimensional metrology of line scales up to 1 m. It has been previously used to support calibration of several generations of the NIST photomask standard—beginning with the NIST Standard Reference Material (SRM) 474. This standard can also be measured by nanoscale techniques such as atomic force microscopy (AFM) or scanning electron microscopy (SEM). We are in the process of recommissioning the LSI and validating its performance at the microscale against these historical data in support of future applications to nanoelectronic manufacturing. While there could be applications in the form of direct LSI measurements on relevant samples such as photomasks, it is more probable that we will use the LSI to provide internal calibration support and cross-validation of traceability for other NIST instruments, such as AFM and SEM, that are more readily applicable to nanoscale measurement applications.

THE NIST LENGTH SCALE INTERFEROMETER

From 1889 until 1960, the International System of Units (SI) meter was defined by the meter bar, which was a physical artifact kept at the International Bureau of Weights and Measures (BIPM) outside of Paris, France. National Metrology Institutes (NMIs) such as NIST, then the National Bureau of Standards (NBS), disseminated the meter to their constituencies by means of comparisons between their own national standards and the meter bar. To perform these comparisons, NMIs would use optical comparators that were custom-built by each organization for the purpose of comparing linear scales such as the meter bar. The NIST apparatus for this purpose incorporated dual optical microscopes that could move relative to the scale bars that were mounted on a platform underneath the microscopes.

The platform could accommodate two bars side-by-side, so that the operator would be able to measure the difference between the two scale bars.

In 1960, by international agreement, the definition of the meter was modified to be based on the vacuum wavelength of the 605 nm spectral line of Krypton. Subsequently, the definition was revised again in 1983 to be given by a fixed value of the speed of light and the realization of the SI second. The invention of the laser in 1960 quickly led to the feasibility of reliable displacement interferometry over distances exceeding one meter, and the 633 nm helium-neon laser became a commonly used secondary standard for realization of the meter. The NIST LSI was first commissioned in 1966, combining 633 nm displacement interferometry with a photoelectric microscope and line-centering position feedback for partially automated measurement of one-dimensional scales [1]. A simplified schematic of the NIST LSI is shown in Figure 1. The major subsystems and components are shown in a block diagram format.

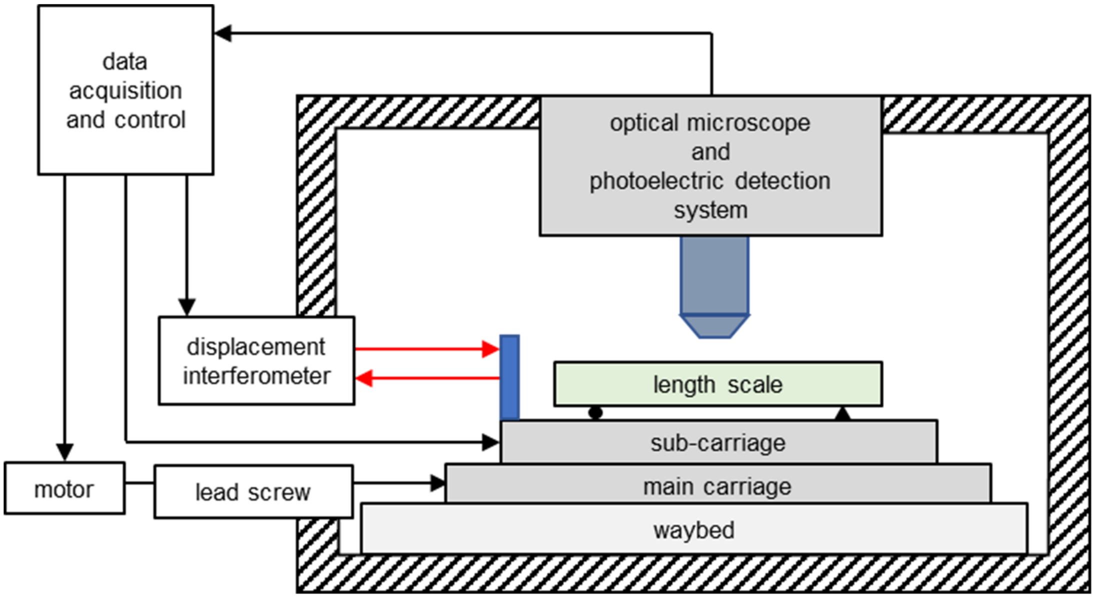

FIGURE 1. Simplified schematic of the NIST LSI.

The LSI was in regular use from 1966 until 2015, and it underwent multiple upgrades and augmentations during this time. However, in 2015, the LSI became non-functional, requiring many repairs and upgrades or complete replacement. Since the LSI had still performed in the top tier of NMIs in the most recent of the interlaboratory comparisons, NIST decided to work with and extend the existing system. This effort is ongoing and NIST is expecting to recommission the LSI in 2022.

LSI Monitor/Control Samples: Long End of Range

The principal original intended application of the LSI was the traceable calibration of linear scales such as those used during the artifact era of meter realization. To monitor and maintain the performance of the LSI over this range, various control samples were used. Two of the most important ones are a 1 m invar scale and a 508 mm steel scale. The 1 m scale has been in use since 1965 and has a measurement history dating back to the commissioning of the instrument. The 508 mm scale has been in use since 1982. A commonly used approach to measurement uncertainty involves the separation into components that are evaluated using purely statistical methods, which is called a type A evaluation, and components that are evaluated by other methods such as prior measurements, physical models, or heuristic arguments, referred to as a type B evaluation [2]. In the most recent working configuration of the LSI, the reproducibility of measurements over these distances was approximately in the range of 30 nm to 50 nm (coverage factor $k = 1$). This is a type A evaluation. Type B evaluations were used to estimate the length-dependent relative standard uncertainty component, which was approximately 5.0×10^{-8}. When the repair and upgrade of the system is complete, we will validate and hopefully improve upon this level of performance.

LSI Monitor/Control Samples: Short End of Range

The relative strength of the LSI is over longer measurement distances, but it is capable of measurements over ranges as short as a few micrometers. Short-range monitoring was less important, due to the much smaller length dependent contributions. However, a variety of scales and samples were used for short-range monitoring. One of these was a 4 µm pitch interval on one of the first generation NIST chromium-on-silica photomask standards–SRM 474. The history of LSI measurements on this interval, shown in Table 1, began in 1984 and extended through 1997. As part of the ongoing repair and recommissioning of the LSI, we are planning to perform this measurement again soon and would expect to obtain good agreement with the prior history as part of the performance validation.

TABLE 1. Short range monitoring of LSI performance: 4 µm interval on SRM474.

Year	Offset from 4 µm Nominal	Expanded Uncertainty (*k* = 2)
1984	-20 nm	± 3 nm
1989a	-18 nm	± 3 nm
1989b	-19 nm	± 3 nm
1990a	-21 nm	± 2 nm
1990b	-14 nm	± 3 nm
1995	-20 nm	± 3 nm
1996a	-15 nm	± 1 nm
1996b	-15 nm	± 1 nm
1997	-15 nm	± 2 nm
2022	--	--

Most of the planned updates to the LSI have been implemented, but repairs of the temperature control system are still in progress. Whereas temperature related effects are important contributors to the uncertainty over long ranges, not so for the short-range measurements on SRM 474. We expect the reproducibility of the line-centering mechanism to be the dominant uncertainty component for measurements in this range.

Although the unique strengths of the LSI are more relevant to measurements between 100 mm and 1000 mm, this system can also be effectively utilized for applications in dimensional nanometrology that are relevant to nanoelectronic manufacturing, as the SRM 474 measurement history illustrates. Several vendors of commercial scale and magnification standards have previously relied on LSI calibrations for their traceability path to the SI meter. Additionally, by measuring one axis at a time, the LSI was used to provide scale traceability for the two-dimensional grid photomask standard SRM 5001 [3]. We are also currently working on several NIST internal projects in nanoscale dimensional metrology and are planning to utilize LSI measurements for these applications. Beyond cross-validation of the traceability of AFM and SEM measurements, the LSI might also support scale calibration of optical microscopy (OM) and localization analysis, with potential applications to nanoelectronic manufacturing.

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KEYWORDS

Traceability, length metrology, line scales, interferometer, nanometrology

Nanomagnetism Imaging NV Center in Diamond Using a Quantum Diamond Atomic Force Microscope

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INTRODUCTION

The technique of high magnetic field sensitivity combined with nanoscale spatial resolution is extremely important for diverse areas such as nanomagnetism [1], spintronics [2], life sciences [3], and even axion-like particles [4]. The Nitrogen-Vacancy (NV) center in diamond is a photostable defect and can be used as an atomic-sized magnetic field sensor owing to its efficient optical initialization and readout as well as long coherence time. A quantum precision measurement instrument called quantum diamond atomic force microscope (QDAFM) based on NV center and atomic force microscopy scanning technology (AFM) allows for sensor-sample distance as small as a few nanometers and scanning, achieving quantitative measurement of stray magnetic field emitted from the sample surface with non-invasive, real-space and nanoscale spatial resolution (up to 10 nm).

SINGLE-SPIN MAGNETOMETER

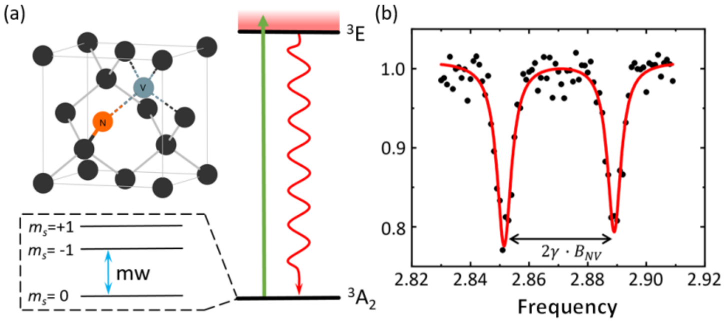

FIGURE 1. (a) Schematic of the NV center and spin levels of NV center. (b) Typical NV ESR spectrum obtained from a single NV center when the external magnetic field is applied.

The core of this technique, NV center in diamond, consists of a substituted nitrogen atom and an adjacent vacancy. The NV center is a spin-1 system with long coherence times even at room temperature. By using a green laser (λ=532 nm), this phenomena is optically initialized with a readout with spin-dependent photoluminescence (PL), and manipulated with a microwave (MW) field. Therefore, the QDAFM employs the NV center as a quantum magnetometer, combined with an atomic force microscope, leading to a non-invasive, real-space, and quantitative measurement of a stray magnetic field near the sample surface with nanoscale spatial resolution. This technique operates well over a large temperature range--from cryogenic to ambient and above—and with a wide range of external magnetic fields.

PRINCIPLE OF MAGNETIC IMAGING

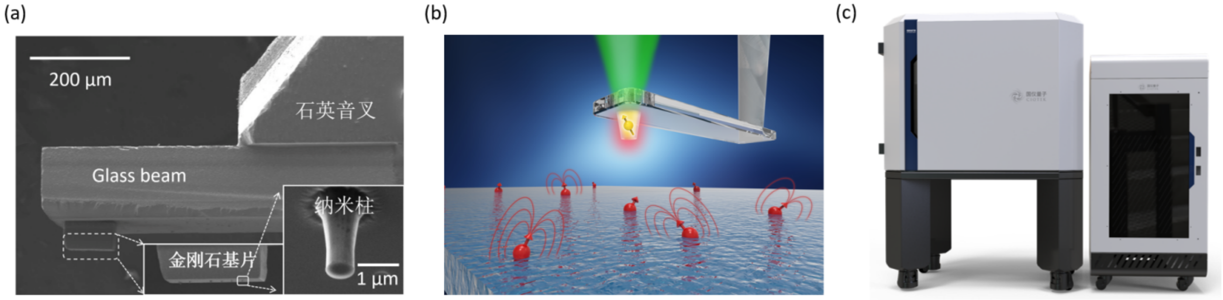

FIGURE 2. (a) Scanning electron microscopy (SEM) image of the diamond probe with arrays of nanopillars. (b) Schematic view of scanning NV microcopy using single nanopillar diamond probe. (c) The QSAFM instrument.

For this technique, a new type of probe with an array of pillars on a (100 μm)^2 × 50 μm diamond chip was fabricated [5]. The probe features high yield, convertibility to be a single pillar, and is reusible. The relatively large area of the diamond chip allows for measurements at a tilt angle using a leveling platform based on the principle of equal thickness interference. The QDAFM is also compatible with Akiyama probes or single nanopillar diamond probe (Figure 2b).

APPLICATIONS

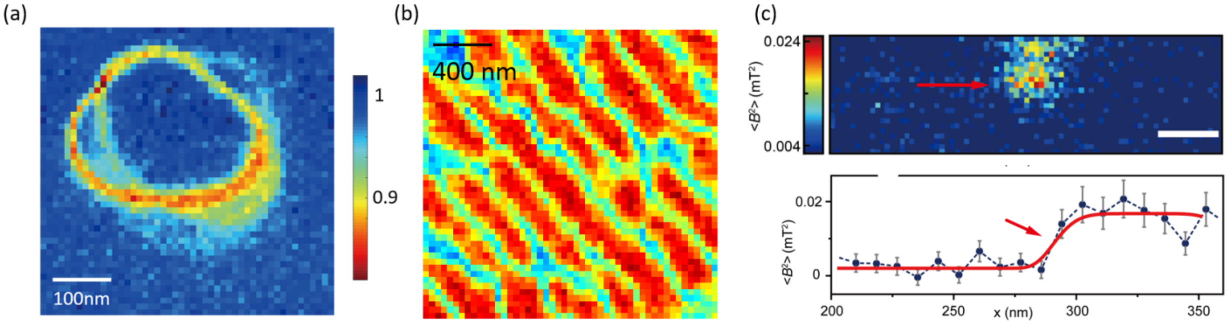

FIGURE 3. (a) Field contour image of a single magnetic skyrmion. The pixel is 10 nm. The QDAFM can also be used to measure magnetic moment density and nature of domain wall in ultrathin ferromagnetic. (b) Magnetic field image recorded above the ferrimagnetic oxides by QDAFM in iso-B imaging mode. (c) High resolution image of ferritins in a single cell. With the scanning, intracellular ferritins are imaged with a spatial resolution of ca. 10nm.

Based on high spatial resolution, details of magnetic textures can be acquired. These phenomena can be explained by the local pinning environment and the hopping between multiple pinning sites during our measurement. Figure 3b shows typical QDAFM results and allows the technique to investigate strain control of magnetic materials in future spintronic devices. In the areas of life sciences [3], nanoscale magnetic imaging of ferritins is obtained (figure 3c). With this technology, we can further study the regulatory mechanism of iron metabolism disorders related to iron at nanoscale, such as hemochromatosis, anemia, liver cirrhosis, and Alzheimer's disease.

OUTLOOK

Magnetic domain walls can be imaged through a variety of techniques including magneto-optical Kerr effect microscopy (MOKE), Lorentz transmission electron microscopy (LTEM), transmission X-ray microscopy, scanning superconducting quantum interference devices (SQUIDs), spin-polarized scanning tunneling microscopy (SP-STM), scanning electron microscopy with polarization analysis (SEMPA), spin-polarized low-energy electron microscopy (SP-LEEM), small-angle neutron scattering (SANS) and magnetic force microscopy (MFM). Each of these techniques has its own limitations. For nanoscale magnetic imaging, MOKE is obviously not suitable because the capacity of spatial resolution is micron-scale. The other approaches can reach nanoscale resolution, but have additional requirements: (i) sample size. LTEM requires thin sample＜100nm while SANS requires sample dimension of mesoscopic scale; (ii) sample surface. SP-LEEM, X-ray microscopy and SEMPA, all these techniques based on reflective particles, require dedicated sample preparation, partly electrical conductivity and highly complicated experimental equipment with ultra-high vacuum, which are limited to model samples and impede special demands for studying its mechanisms; (iii) sample conditions. SQUIDs and SP-STM only operate under cryogenic conditions. And MFM could disturb the studied spin textures severely owing to the magnetic field intensity of intrinsic magnetic nature of the probe that can be comparable to the external field. Therefore, the QDAFM promises significant advances in magnetic domain wall imaging, providing non-perturbing and quantitative measurements of the stray magnetic field.

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KEYWORDS

NV center in diamond, Spintronics, Scanning NV microscopy, Magnetic domain wall, Quantum magnetometer

Cathodoluminescence Spectroscopy Probe of Semiconductor Defects and Carrier Dynamics

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INTRODUCTION

High spatial resolution spectroscopic information may be acquired by using an electron beam in a modern scanning electron microscope (SEM), exploiting a phenomenon called cathodoluminescence (CL) where electrons are promoted from the conduction band to the valence band upon impingement of the high energy electron beam onto a semiconductor. This approach offers several advantages over usual optical spectroscopy techniques. The multimode imaging capabilities of the SEM enable the correlation of optical properties (via CL) with surface morphology (secondary electron mode) at the nanometer scale and the large energy of the electrons allows the excitation of wide-bandgap materials[1,2]. In addition, CL sensitivity to material composition, as well as the presence of defects, makes it a technique of choice for device characterization.

DEFECT DETECTION AND COMPOSITIONAL ANALYSIS

Quantitative CL has extensively been used to study aging effects and reliability issues in advanced III-V semiconductor devices such as nitride-based power devices[3] (Figure 1), light emitting diodes[4] (Figure 2) or vertical surface emitting laser (VCSEL) devices. Here, we will present recent advances in instrumental developments as well as recent examples of materials studies.

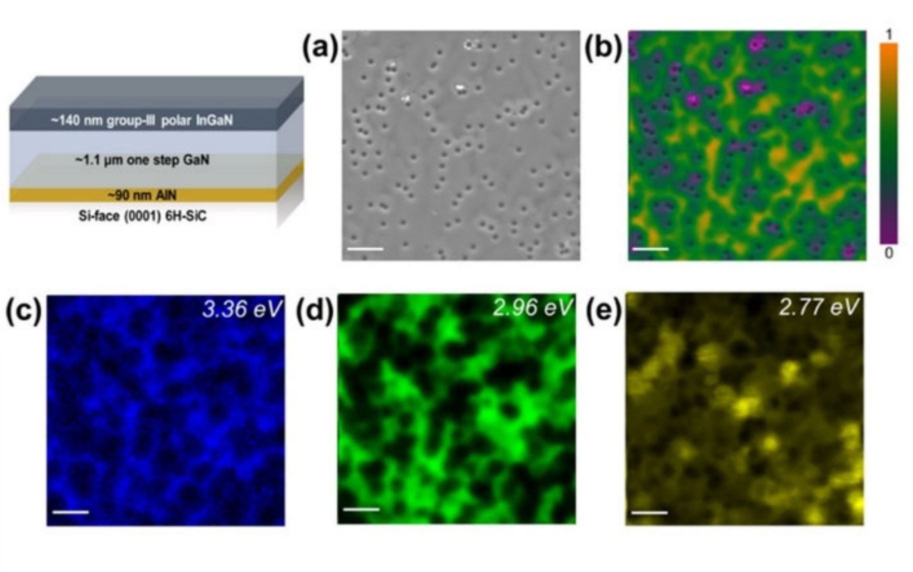

FIGURE 1: Spatially resolved CL measurements of group-III polar InGaN at RT: (a) SEM image of the surface and (b) superimposed SEM + panchromatic CL image [(c) – (e)] are monochromatic CL maps extracted from the collected hyperspectral map at (c) 3.36 eV, (d) 2.96 eV, and (e) 2.77 eV. The scale bars on the SEM and CL maps are 1 µm

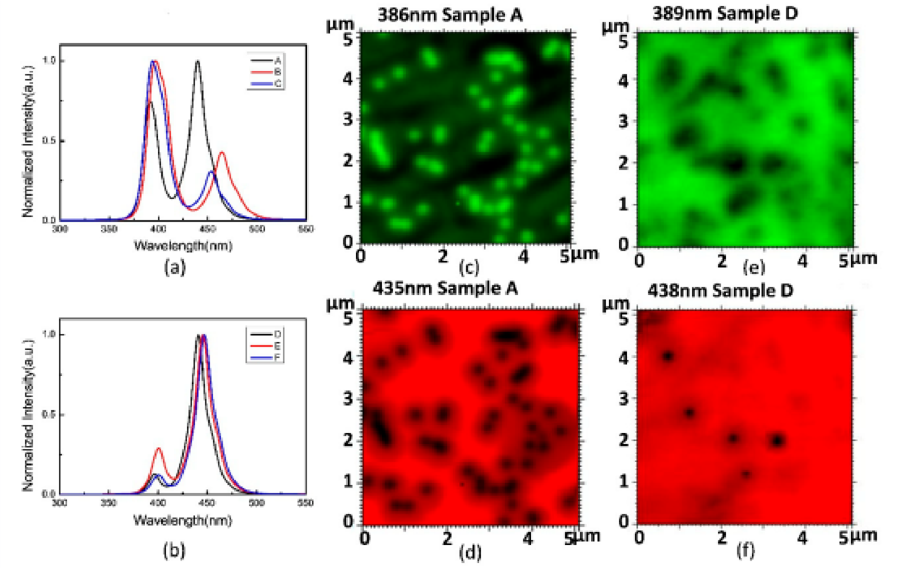

FIGURE 2: CL spectra of samples (a) A/B/C and (b) D/E/F measured at 10 K. Spatial distribution of CL spectral bands of sample A at (c) 386 and (d) 435 nm. Spatial distribution of CL spectral bands of sample D at (e) 389 and (f) 438 nm.

CARRIER DYNAMICS ANALYSIS IN NANOSTRUCTURES

Cathodoluminescence can measured in time-resolved mode (femtosecond electron pulses) with space resolution of 10 nm. Picosecond and femtosecond spectroscopy allow for a detailed study of carrier dynamics in nanostructured materials[5] as illustrated in Figure 3.

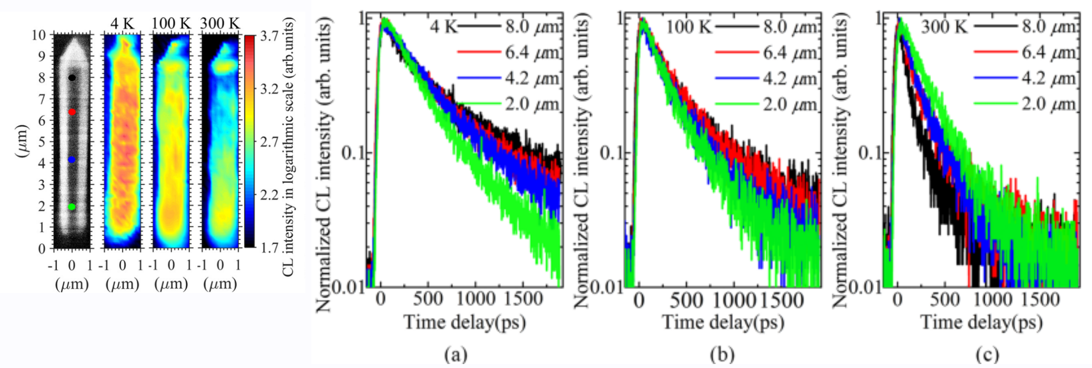

FIGURE 3: CL decays of QW emissions at different positions along the rod at a) 4, b) 100, and c) 300 K, respectively.

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KEYWORDS

Cathodoluminescence, Semiconductor, Nanoelectronics, Materials, LED, Carrier Dynamics, Solar cell, GaN, SiC

Ultra-wide bandgap semiconductor materials studied with extreme ultraviolet atom probe tomography

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INTRODUCTION

Ultra-wide bandgap semiconductors are attractive materials due to their applications in optoelectronics and high-power devices [1]. Accurate measurements of the composition, dopants, and impurities in Ga_2O_3-based devices is of critical importance. Atom probe tomography (APT) is one of the analytical tools used to measure the composition of materials; however, recent APT measurements of III-nitride semiconductor materials have revealed compositional biases on such systems [2,3].

In this work we perform compositional APT studies on oxides and unintentionally doped β-Ga_2O_3 using a commercial APT instrument and a custom-built extreme ultraviolet (EUV) APT. While commercial near-UV (NUV) APT systems utilize a 355-nm laser to induce field ion evaporation, in the custom system we replaced the near-ultraviolet laser in a straight flight-path atom probe tomograph with a coherent EUV light source and a vacuum beamline. With these modifications, we were able to illuminate the specimen's tip with 30-45 eV energy photons [4].

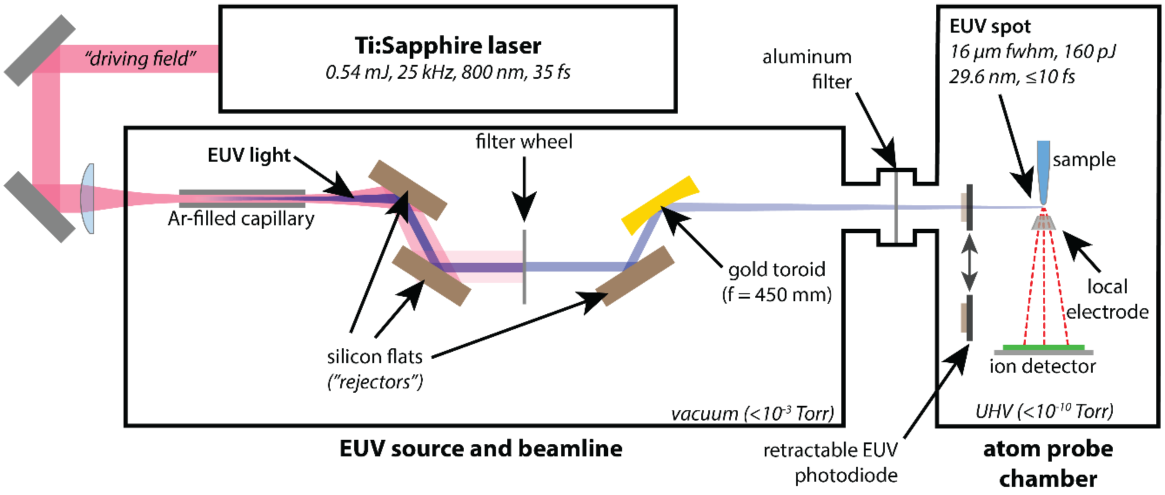

FIGURE 1. Schematic representation of EUV pulsed Atom Probe Tomograph.

EUV-ASSISTED ATOM PROBE TOMOGRAPHY

In our EUV APT measurements we maintain a constant ion detection rate while varying the EUV pulse energy by approximately two orders of magnitude (x120) and sample standing voltage. Our results show an underestimation of the oxygen composition when performing APT experiments under high EUV pulse energy or low E-field conditions. Compositional values closer to stoichiometric are obtained when performing experiments under high E-field conditions. These results are similar to recently published results with a NUV APT instrument [5]. These NUV experiments were performed at 100 kHz laser repetition rate, for this reason we performed additional studies with a commercial NUV APT instrument at 25 kHz. A careful compositional analysis comparison between the NUV and EUV systems will be discussed.

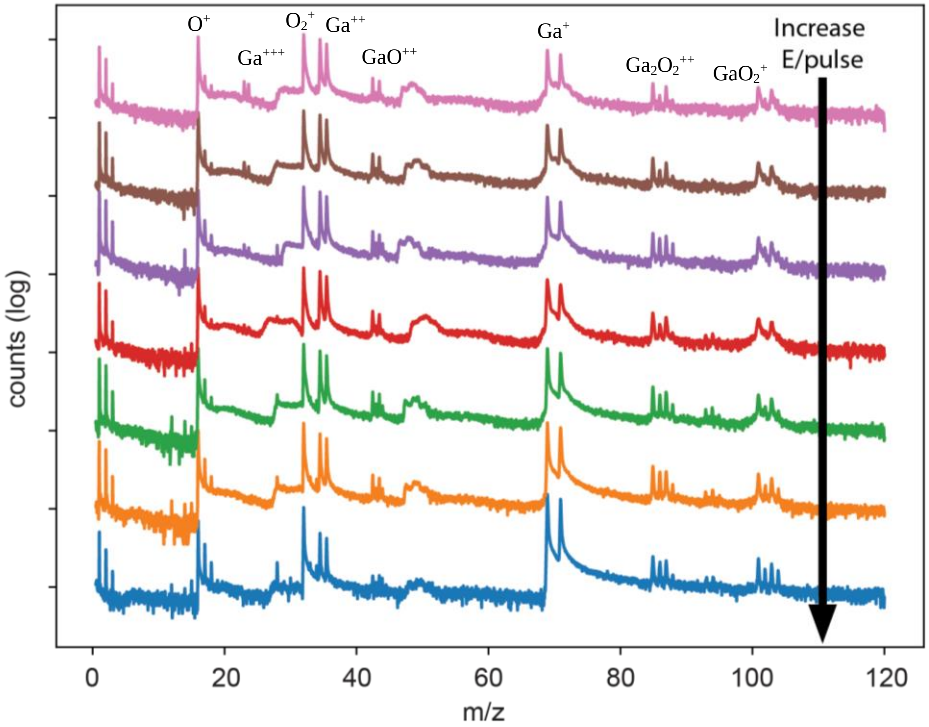

FIGURE 2. EUV APT mass spectra of Ga_2O_3 specimen as a function of EUV energy per pulse.

Our EUV APT data also shows the existence of unintentionally doped Si in the β-Ga_2O_3 sample. This is of importance as technologically-relevant devices with Si implantation are under development [6]. Further studies will focus on EUV APT reconstructions of Si-implanted β-Ga2O3.

CONCLUSION

We have adapted an atom probe tomograph with an ultrafast, EUV source in place of a pulsed, visible-UV laser. We present a Ga_2O_3 mass spectra comparison between a commercial NUV APT instrument and our EUV APT. In both instruments the correct composition is obtained when performing measurements under high field conditions.

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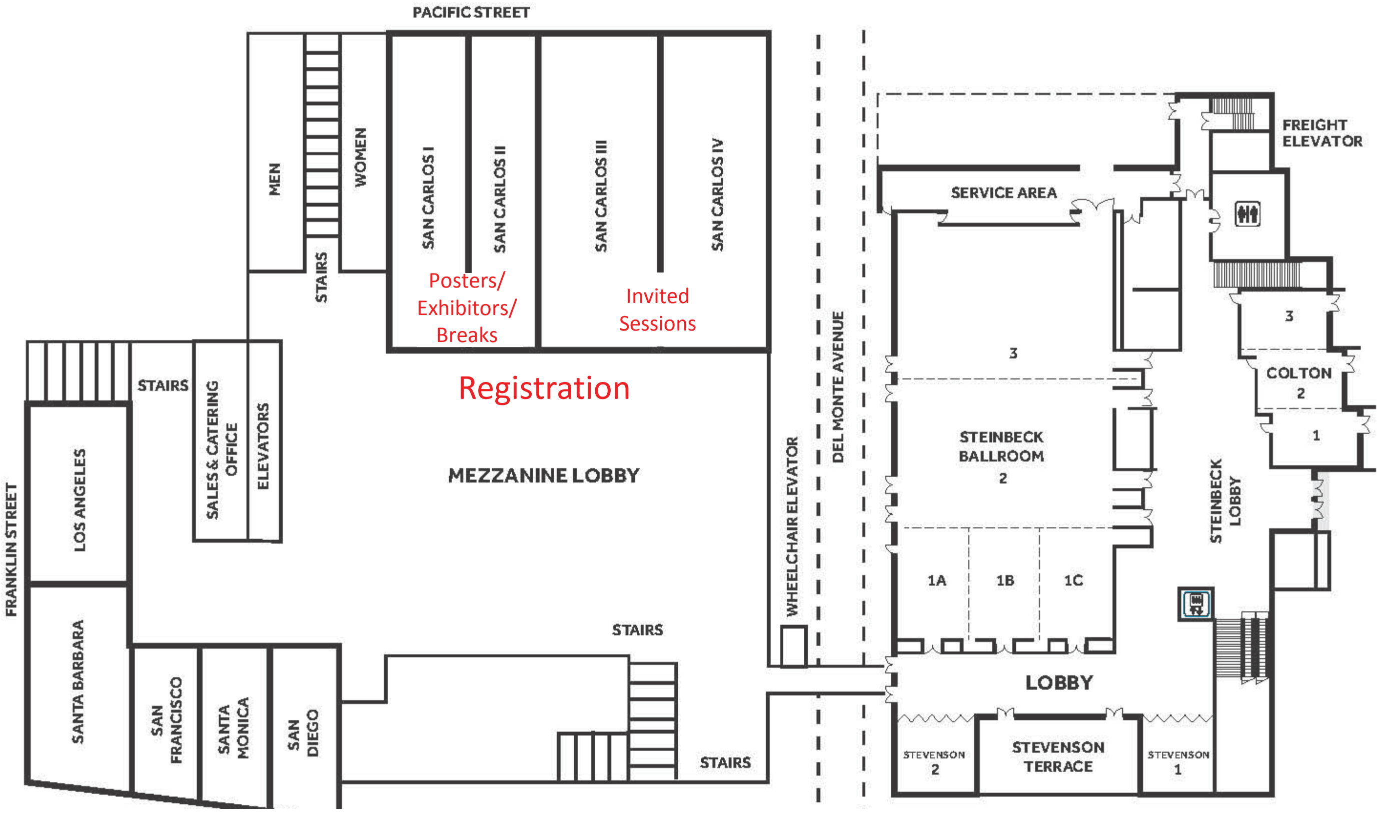
KEYWORDS

Atom Probe Tomography, Oxides, Wide-bandgap semiconductor, Extreme-Ultraviolet Light

MEZZANINE FLOOR



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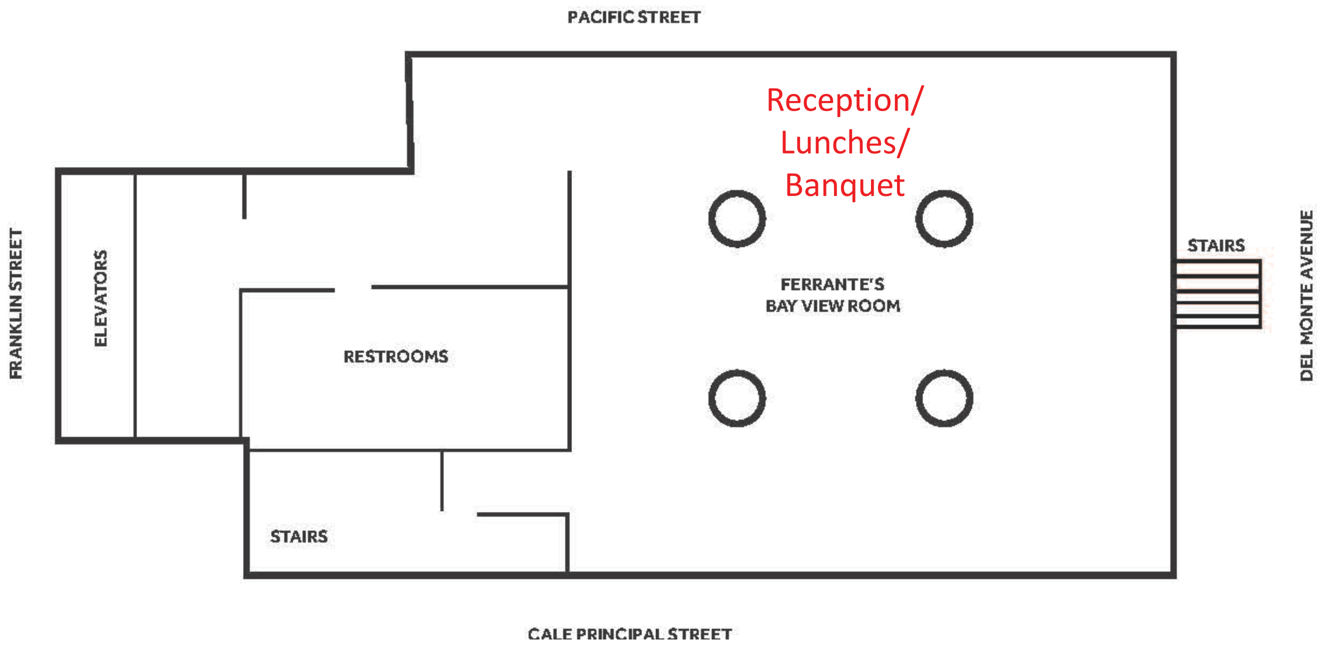

Program at a Glance

	Morning	AM Sessions	PM Sessions	Evening
Tuesday Jun. 21st	**7:00** Registration / Attendee Check-in	**9:00** Conference Opening **9:15** Plenary	**1:30** Industry Trends **3:30** Microscopies I	**5:00** Poster Session **6:45** Banquet
Wednesday Jun. 22nd	**7:45** Registration / Attendee Check-in	**8:30** Tomographies **10:30** New Developments in Chemical / Electrical Characterization	**1:30** Microscopies II **3:00** New Techniques for Emerging Devices / Beyond CMOS **3:30** Advanced Manufacturing Metrology	**5:00** Poster Session
Thursday Jun. 23rd	**8:00** Registration / Attendee Check-in	**8:30** EUV and Advanced Patterning **10:30** Advanced Packaging	**1:30** Emerging Materials and Devices **3:30** Spintronics-Based Devices	