Quantitative Atom Probe Tomography of Complex Systems

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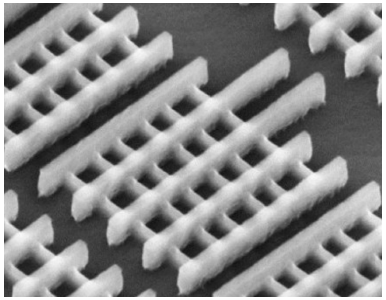
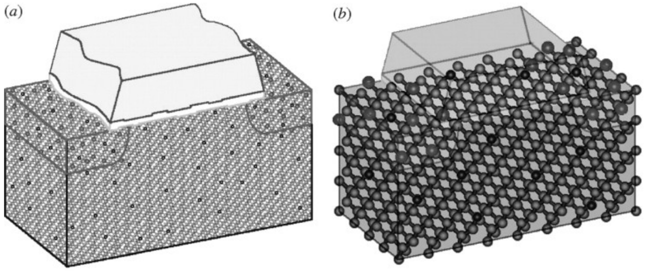
Motivation

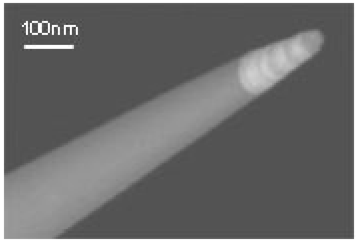
3D

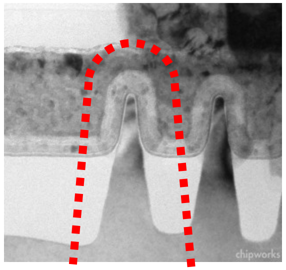


Atom



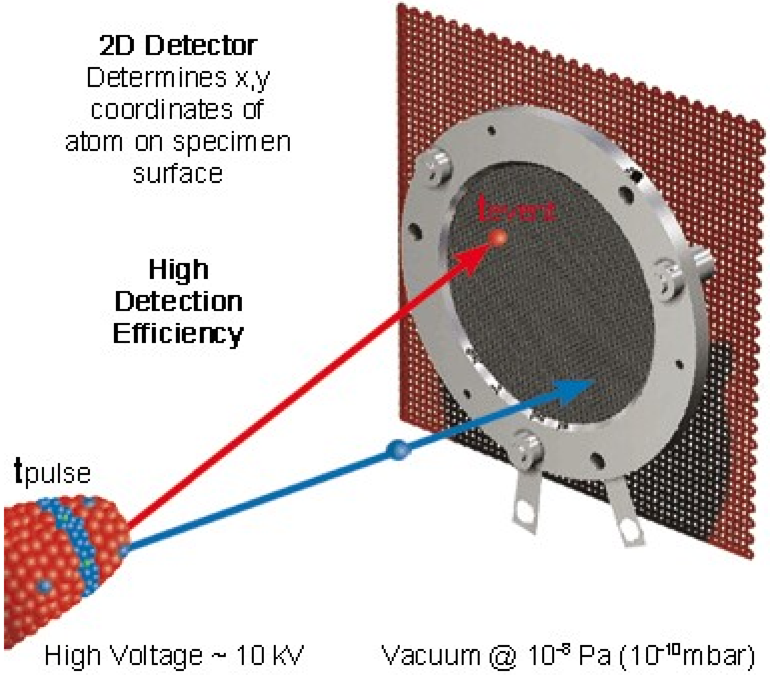
Probe





1. Intel 22 nm channel and gate publicity image (Intel)
2. Walker *et al.*, *Phil. Trans. R. Soc. A* **368**, 3967 (2010)
3a. Atom probe tip (CAMECA Instruments)
3b. Intel 22 nm finFET TEM (Chipworks)

Atom probe basics



Schematic showing the principles of atom probe tomography.

Labelled in the diagram are the Specimen and the 2D position sensitive detector,

t(pulse) is a laser or voltage pulse acting on the tip of the specimen that triggers evaporation of ions and t(event) is the time the ion reaches the detector.

$$F = V / (k_f\, r)$$

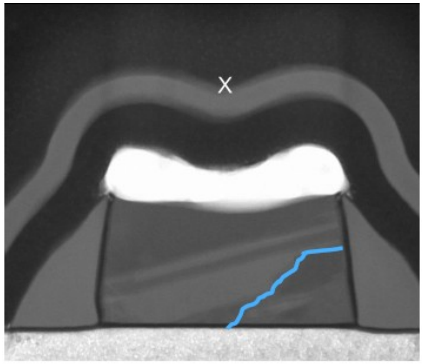
Measured

x
y
z
} Compute 3D position

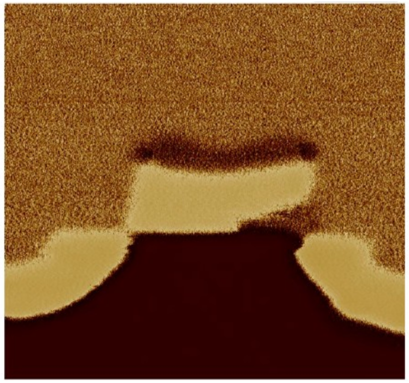
t — Determine ionic weight

Detector image from CAMECA Instruments
http://www.cameca.com/instruments-for-research/atom-probe.aspx

Planar device poly-Si gate analysis



TEM:
structure



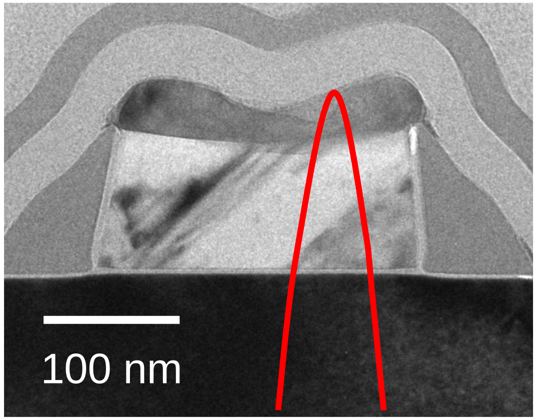
SSCM:
carriers

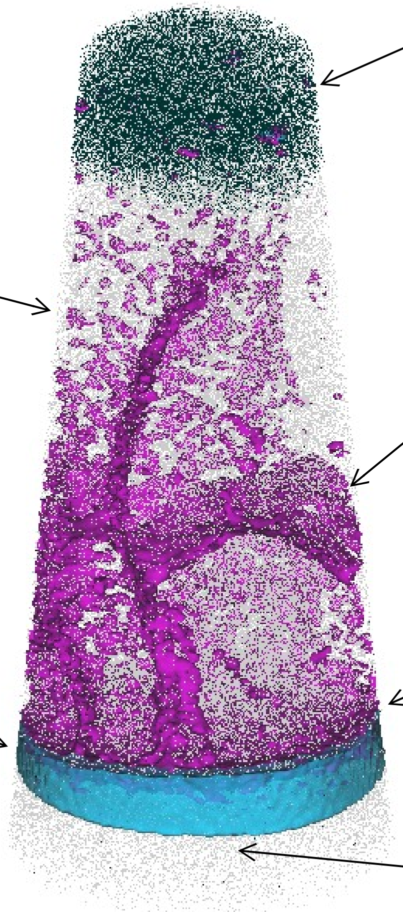
SSRM:
carriers

?

APT:
dopants

nMOS poly-gate





Silicide composition

Dopants composition in grains

Dopant segregation into grain boundaries

Dopant pile up at gate oxide

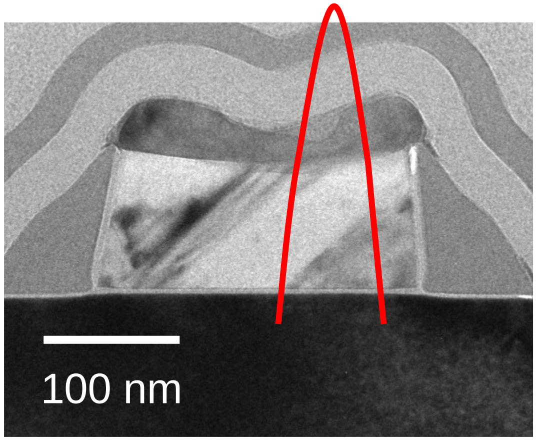
Gate oxide

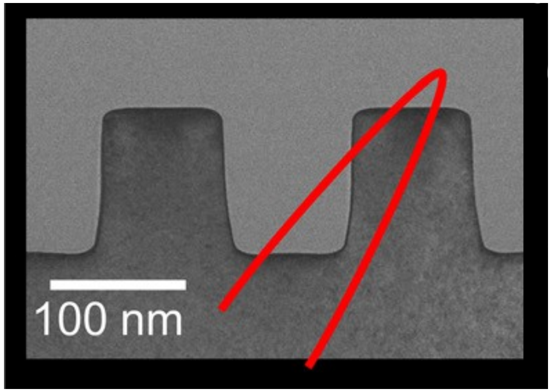
APT doping

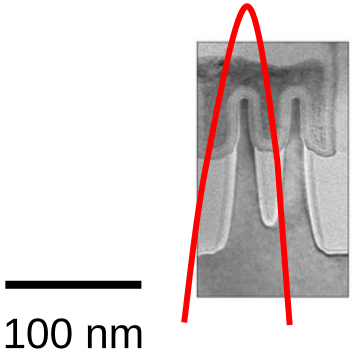
Dopant penetration into channel

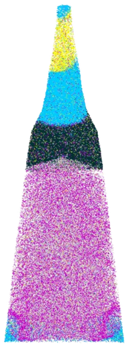
Field-of-view

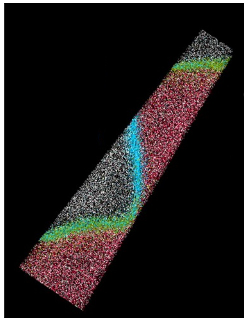
$$F = V / (k_f\, r)$$











^{28}Si

^{30}Si

O

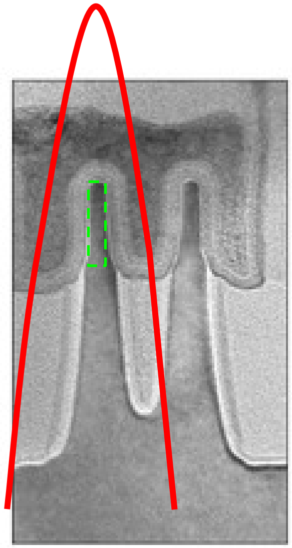
Ti

As

B

1. 250 nm planar device
2. 100 nm test structure, Takamizawa *et al.*, *Appl. Phys. Lett.* **100**, 093502 (2012)
3. Intel 14 nm finFET, *IEDM 2014*

Sensitivity for a single atom

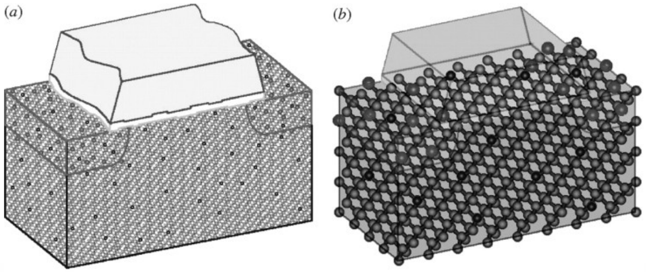


Intel 14 nm finFET,
IEDM 2014

Feature	Size
Fin width, y	8 nm
Fin height, z	42 nm
Gate length, x	24 nm

Volume, v ~ 8000 nm^3

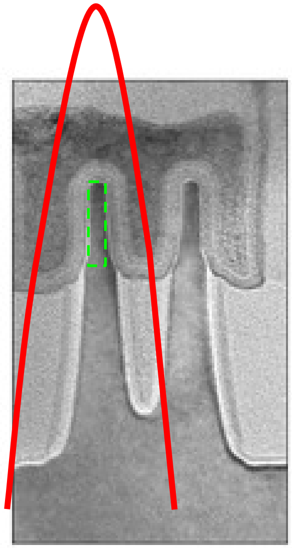
Atom count, N ~ 400,000 atoms



Walker *et al.*, *Phil. Trans. R. Soc. A* **368**, 3967 (2010)

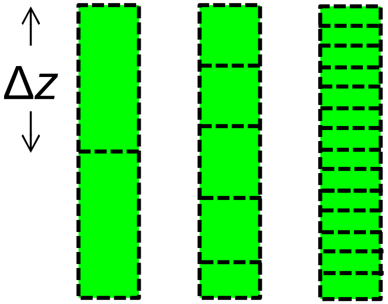
Universal sensitivity limit
1 / 400,000
0.00025 at.%
2.5 ppm
1.2E17 cm^{-3}

APT effective sensitivity limit



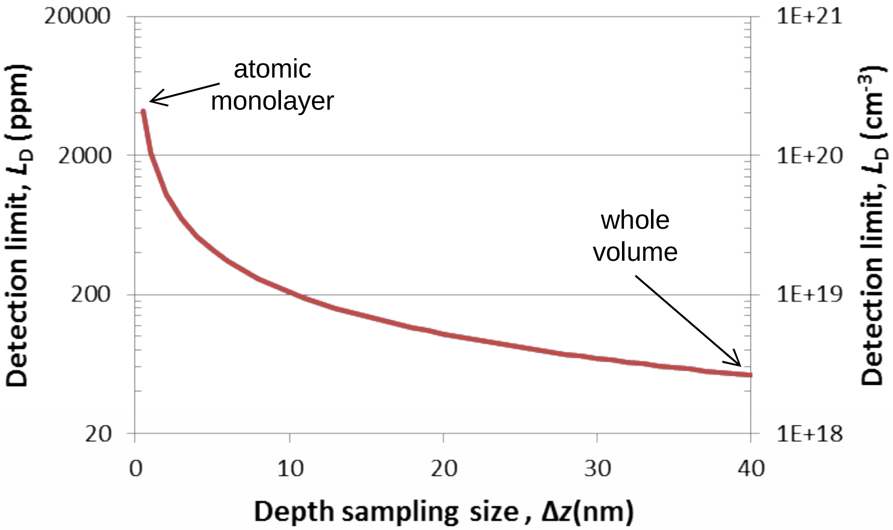
Intel 14 nm finFET, *IEDM 2014*

- **Sampling size (Δ*z*)**
- **Detector efficiency**
- **Background noise, N_B**



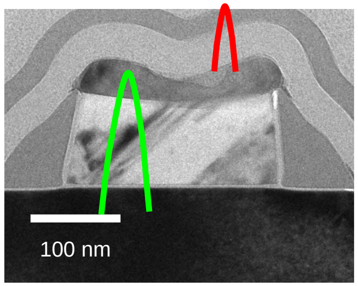
Detection limit $L_D = k^2 + k(2N_B)^{0.5}$

At 2σ precision, if $N_B = 2$ then $L_D = 10$ counts



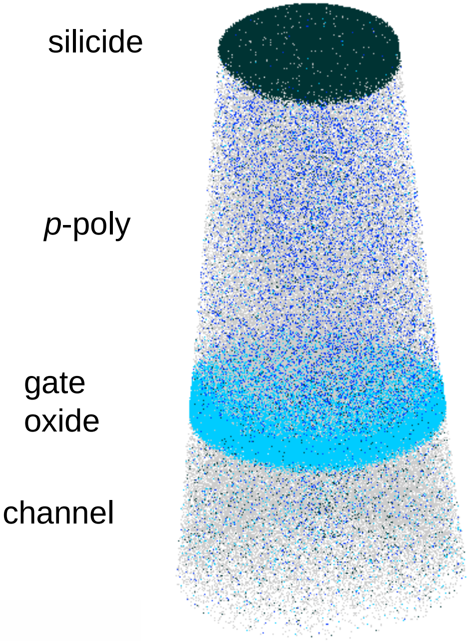
pMOS

Poly-gate issue is in pMOS device

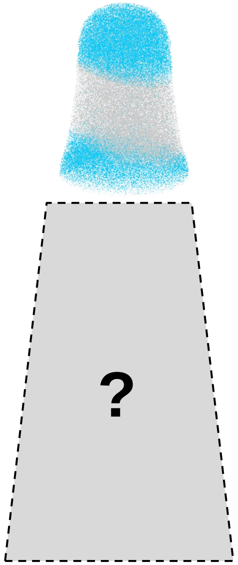


Good location

Bad location

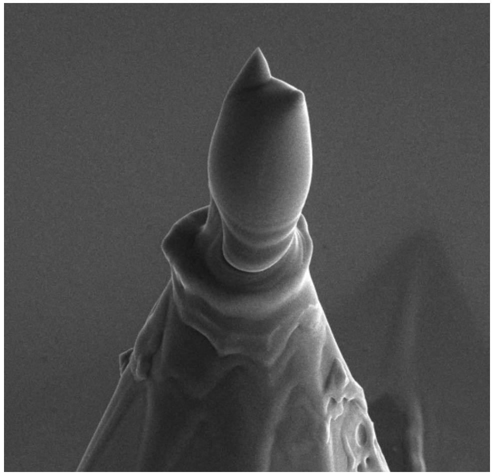


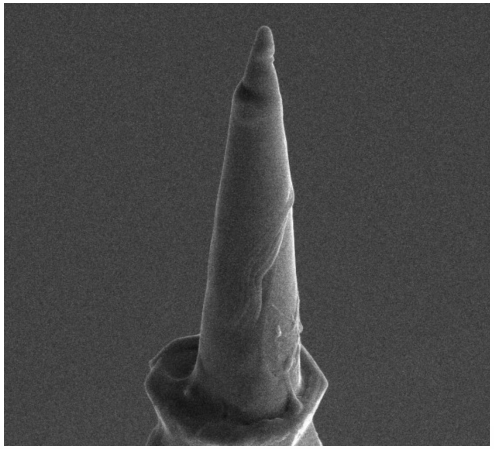
Si
Ti
O
B



Atom probe in practice

	Fab in-line quality verification	Failure and reliability analysis	R&D support
Data quality requirement	Consistently high reproducibility and accuracy (<1%)	Enough to spot defects and anomalies	Ability to offer unique insight
Time to knowledge requirement	Every minute counts	Every hour counts	Every day counts
Successful measurement probability	Sufficient to get data quickly	100%, able to work on unique specimen	Sufficient to get data in high volumes





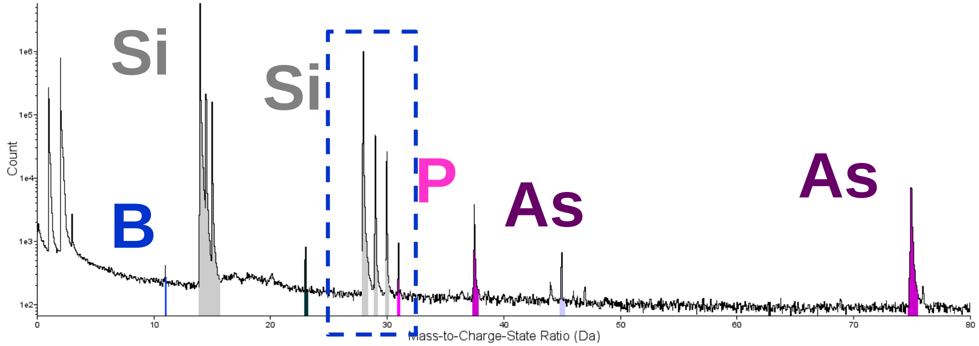
Compositional accuracy issues

- Multiple hit/detector (B quantification)
- Mass-overlaps/complex ion formation (Si^{++} and N^{+})
- Mass-overlaps/multiply charged ions (O and O_2^{+})
- Non-stoichiometric measurements (SiO_2, TiN)
- Out-of-time evaporation
- Dependency of composition on measurement conditions (field, laser)
- Variation of measurement conditions inside specimen, over time and between measurements

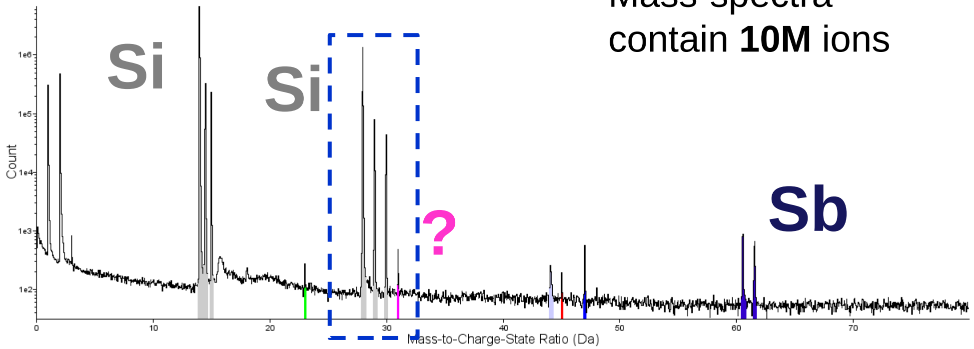
Compositional precision: mass-overlaps

P (31 amu) is a common *n*-type dopant.

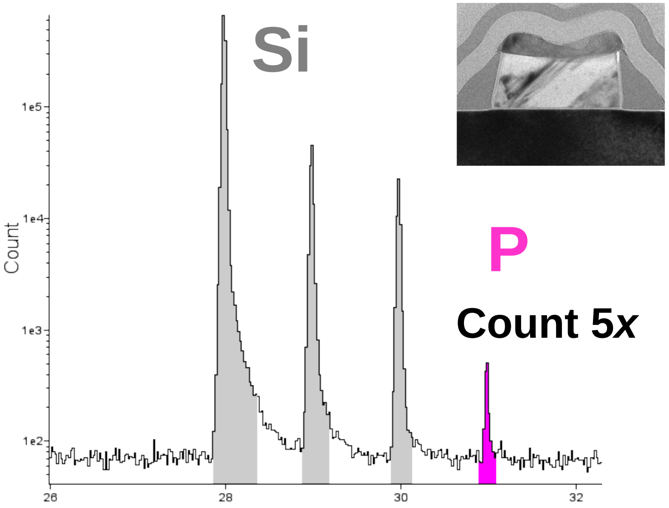
0.25 µm
***n*MOS**
poly

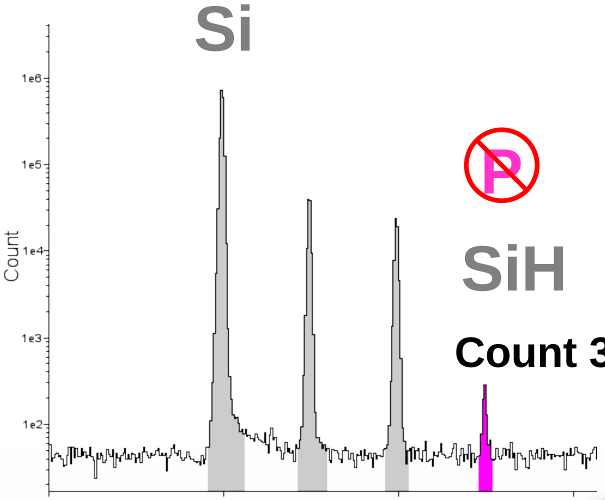


Si microtip
(no P)



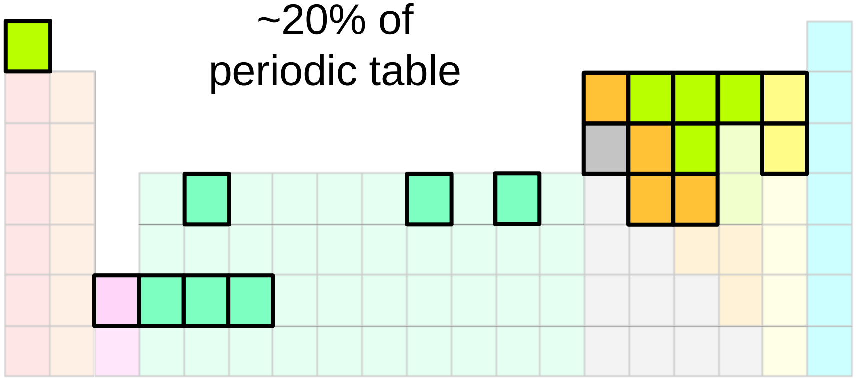
Mass-spectra
contain **10M** ions





Mass-interference between ^{31}P and ^{30}SiH prevent reliable quantification of dilute P in Si.

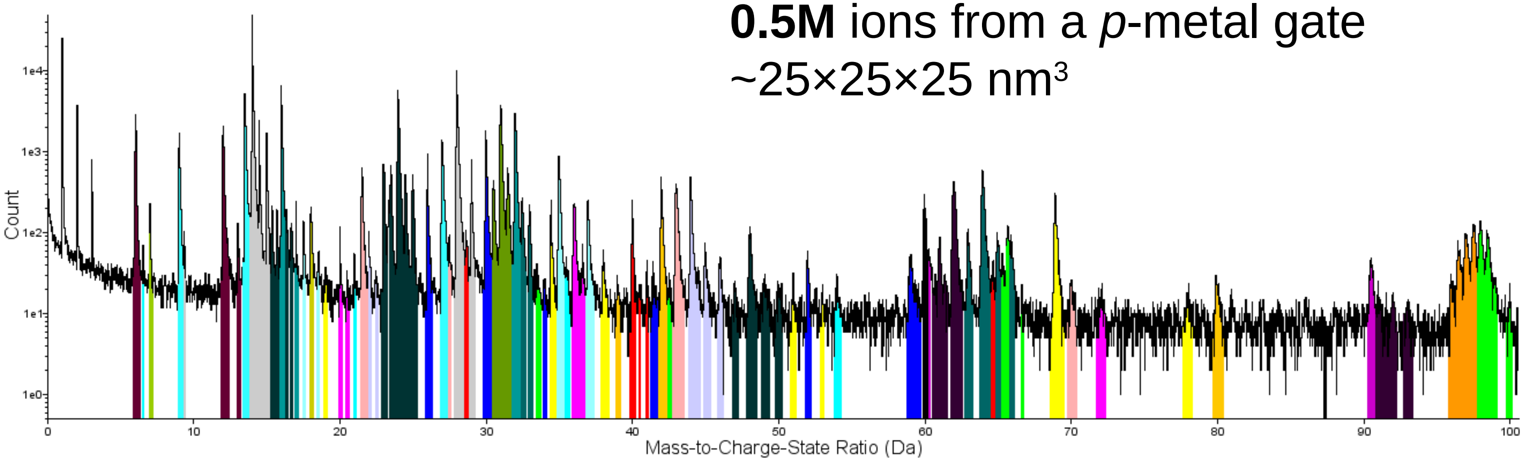
Composition of advanced devices



~20% of periodic table

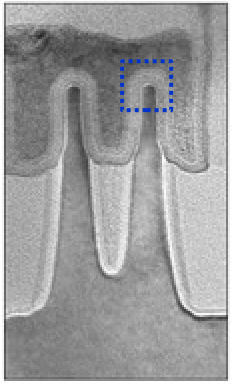
Tradition devices have poly-Si gates and SiO gate dielectric.

High-*k* gate oxide and replacement metal gate in sub-45 nm devices increases compositional complexity

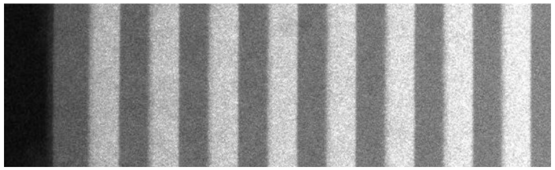


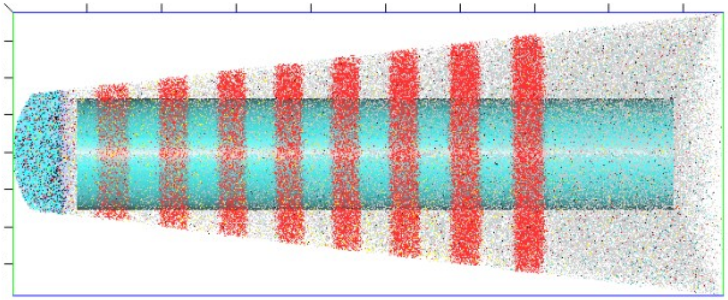
0.5M ions from a *p*-metal gate
~25×25×25 nm^3

Intel 14 nm finFET,
IEDM 2014



Spatial accuracy: atomic density

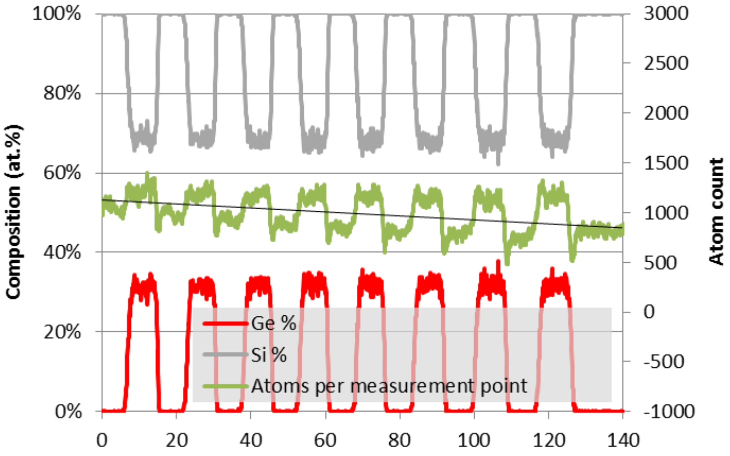




Reconstruction of a Si/SiGe test structure.

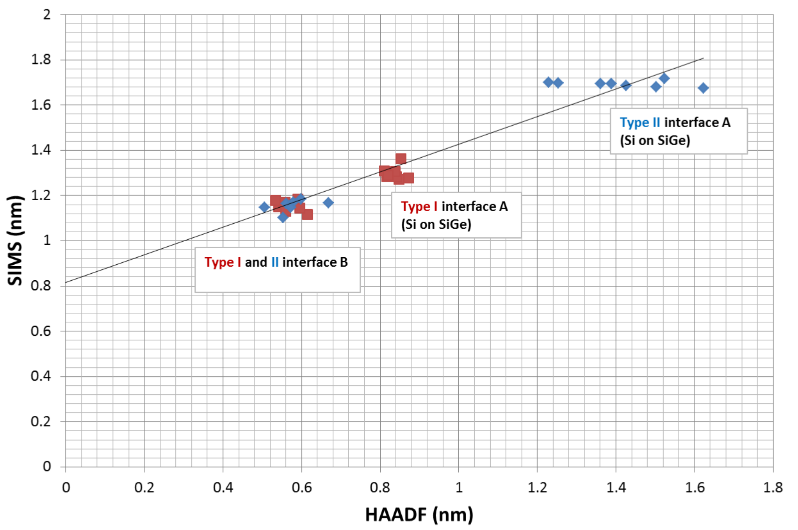
Layers are

- Flat
- Evenly spaced
- Dimensions calibrated against TEM



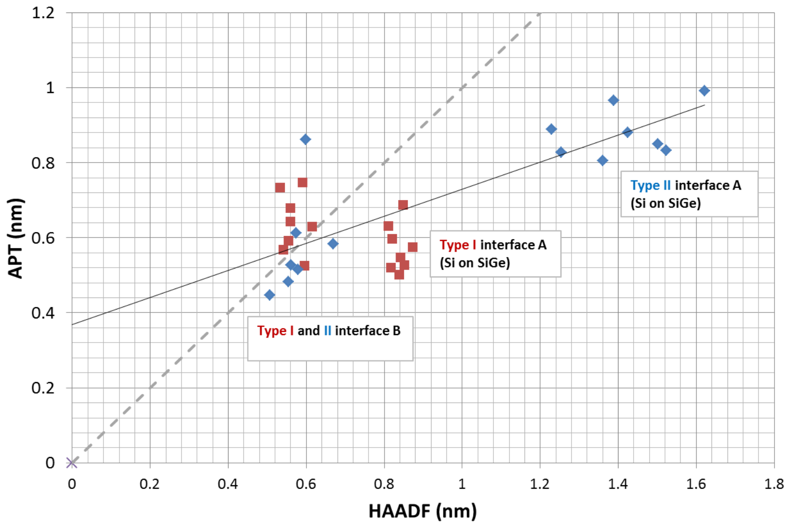
Atomic density fluctuates throughout the reconstruction because of tip shape change from different evaporation field/laser interaction (local magnification)

Spatial accuracy: interface profiles



SiGe interface profiles measured for two different growth conditions.

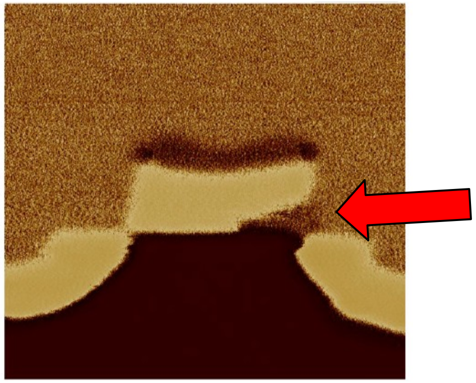
SIMS and HAADF show consistent results with tight groupings. There is a linear relationship between the measured interface widths.



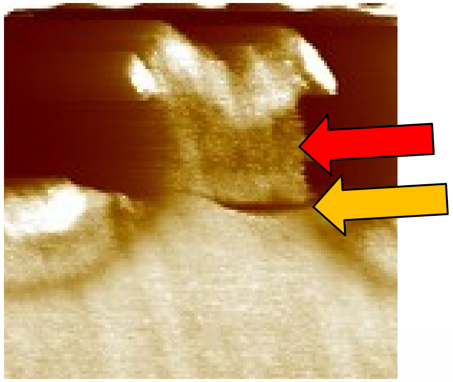
In comparison, APT has a large spread in measured interface widths due to dependency on specimen geometry/layer depth and atomic density.

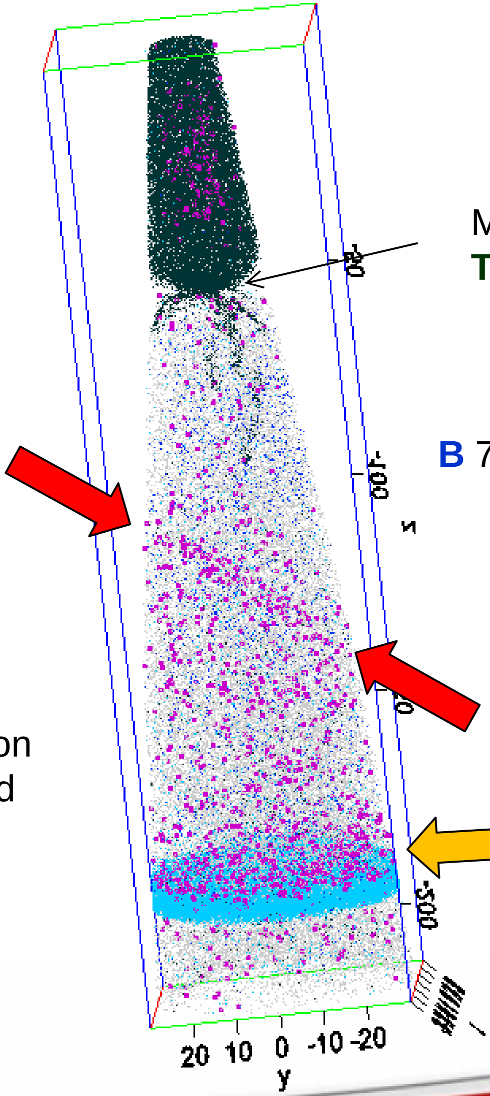
pMOS failed device

SSCM



SSRM





Microfracture at
Ti rich layer

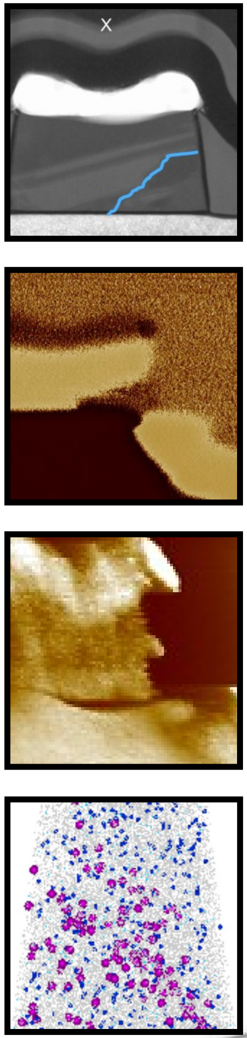
B 75% good location

As in grain
boundary

As >300%
good location
B 50% good
location

As pile up at
gate oxide

Summary



- APT was used to determine the **dopant composition in a poly-Si gate** of failed planar transistor devices.
- For older technology nodes, APT **field-of-view** can only image part of the device. For recent finFET geometries, single device analysis is possible.
- **Sensitivity** is limited by small volume, low atom count of finFET devices. High sensitivity can be achieved for large volume devices.
- **Data reproducibility**, **time-to-knowledge** and **measurement success rate** are important criteria for various fab applications. Prematurely failed specimens prevented useful failure analysis data being obtained in a timely manner.
- A number of **compositional issues** exist and are well known in APT. In the case of poly-Si gate measurement, possible P issue can not be checked due to mass overlaps. This is a particular issue in modern devices with diverse compositions
- For planar devices **spatial accuracy** is not a huge issue. For small volumes in finFETs trajectory aberrations limit compositional and dimensional fidelity.
- Using APT, it was demonstrated that As rich grain and lower B doping was cause of failure in pMOS poly-Si gate.